DATA CONVERTERS

& Voltage References IC Handbook

PLESSEY
Semiconductors

Foreword

The collective description of Data Conversion covers a vast range of applications which is limited only by the imagination of today's system designers. Traditionally the name of Plessey Semiconductors has been associated with data conversion products offering the ultimate in high speed performance. 1987 saw the introduction of several more modest speed ADCs and DACs aimed at both commercial and professional video applications. Now, with the addition of a comprehensive range of microprocessor compatible ADCs and DACs and also the faster triple DACs for graphics applications we can really claim "we've got something for everyone".

The line up of 'Flash' analog to digital converters now includes ECL and TTL output versions of a 30MHz 8-bit design. The SP97504 benefits from recent technology improvements and has been brought in to replace the older 100MHz 4-bit SP9754. At the other end of the spectrum the ZN437 introduces an 8-bit 8 channel data acquisition system which will satisfy the demands of industrial process monitoring and similar instrumentation applications. And for applications where the ability to transmit data serially is important our ZN509/ZN510 parts provide a serial output and come in small 8 pin DIL packages ideal for co-siting with remote transducers.

On the digital to analog converter side the latest ultra high speed product is our 450MHz 8-bit SP98608. This design has applied a wealth of experience in DAC design techniques to our 7GHz f_T WS process. In addition to the ZN454 triple 4-bit video DAC we now have the ZN455 triple 4-bit DAC with palette memory, and for systems requiring higher resolution, the ZN515 8-bit video DAC. In the microprocessor compatible area we have five new 8-bit designs, but perhaps more significantly maximum resolution is now extended to 12-bits with the ZN6012.

Plessey Semiconductors also offers a comprehensive range of voltage reference sources: there are basically four series within the range. The 'REF' series of micropower devices have operating currents down to 40μA. In TO-92 package, these parts are pin compatible to National Semiconductor LM385Z/285Z ranges.

For ultra stable performance over current and temperature the ZN458/423 series have slope resistance of as low as 0.2 and temperature coefficients as low as 29ppm/°C guaranteed. The 'ZNREF' range of low current precision references offer five choices of nominal voltage between 2.5 and 10V and feature a trim facility such that system errors, etc., can be trimmed out.

The fourth addition to the range is the SR series, the world's first SOT-23 bandgap reference ICs, giving the ultimate in miniaturisation.

So now Plessey Semiconductors can offer you 'one-stop shopping' for all your data conversion needs; but if you can't find the product to solve your particular design problem, then we would like to hear from you!

Contents

Product index - Data conversion

High Speed DACs

Type	Function	Guaranteed Min Clock Rate	DAC Max Rise Time (10% to 90%)	Process	Page
MV95308	8-bit video DAC	30MHz	6.0ns	CMOS	13
MV95408	8-bit video DAC	50MHz	5.5ns	CMOS	17
SP9768	8-bit multiplying DAC	100MHz	2.0ns	Bipolar	47
SP9770	10-bit multiplying DAC	50MHz	3.0ns	Bipolar	51
SP98608	8-bit latched multiplying DAC	450MHz	800ps	Bipolar	116
SP97618	8-bit graphics DAC	200MHz	1.1ns	Bipolar	110
ZN454	Triple 4-bit video DAC	100MHz	5.0ns	Bipolar	329
ZN455	Triple 4-bit video MEMDAC	100MHz	5.0ns	Bipolar	336
ZN515	8-bit video DAC	100MHz	5.0ns	Bipolar	383

Advanced Function DACs

Type	Function	Linearity Error (LSB)	Settling Time (μs)	Output Type	On-chip Reference	Special Features	Page
ZN425	8-bit DAC/ADC	±0.5	1.0	Voltage	YES	8-bit counter	121
ZN426	8-bit DAC	±0.5	1.0	Voltage	YES	Low cost	128
ZN428	8-bit microprocessor compatible DAC	±0.5	0.8	Voltage	YES	Data latch	149
ZN429	8-bit DAC	±0.5	1.0	Voltage	NO	Low cost	158
ZN434	4-bit DAC	±0.25	0.2	Voltage	YES	Low cost	182
ZN435	8-bit multifunction DAC/ADC	±0.5	0.8	Voltage	YES	Up/down counter	185
ZN436	6-bit DAC	±0.5	1.0	Voltage	NO	Low cost	198
ZN438	8-bit microprocessor compatible DAC	±0.5	1.25	Voltage	YES	High speed output buffer amplifier	229
ZN508	8-bit dual micro-processor compatible DAC	±0.5, ±1.0	0.8	Voltage	YES	Separate Vref inputs and data latches for each DAC	363
ZN525	8-bit multifunction DAC/ADC	±0.5	0.8	Voltage	YES	Up/down counter Enhanced control circuitry	384
ZN527	8-bit dual micro-processor compatible DAC	±1.0	0.8	Voltage	NO	Separate Vref inputs and data latches for each DAC	392
ZN528	8-bit dual micro-processor compatible DAC	±0.5	0.8	Voltage	NO	Separate Vref inputs and data latches for each DAC	392
ZN558	8-bit microprocessor compatible DAC	±0.5	0.8	Voltage	YES	Data latch	408
ZN559	8-bit microprocessor compatible DAC	±1.0	0.8	Voltage	YES	Low cost, monotonic	419
ZN6012	12-bit DAC	±1.0, ±2.0	0.6	Current	NO	Low cost	432

Advanced Function ADCs

ZN427	8-bit microprocessor compatible ADC	±0.5	10	NO	YES	Three-state data outputs	133
ZN432	10-bit ADC	±0.5,±1.0	20	NO	YES	Serial and Parallel data outputs	166
ZN433	10-bit tracking ADC	±0.5	1*	NO	YES	Serial and Parallel data outputs	174
ZN437	8-bit, 8 channel data acquisition system	±0.5, ±1.0	16	NO	NO	Programmable clock prescaler, 8 x 8 bit RAM, four conversion modes	203
ZN439	8-bit microprocessor compatible ADC	±0.25, ±0.5, ±1.0	5	YES	YES	Advanced micro-processor interface with double buffered latches	242
ZN447	8-bit microprocessor compatible ADC	±0.3	9	YES	YES	Three-state data outputs	268
ZN448	8-bit microprocessor compatible ADC	±0.5	9	YES	YES	Three-state data outputs	268
ZN449	8-bit microprocessor compatible ADC	±1.0	9	YES	YES	Three-state data outputs low cost	268
ZN501	10-bit microprocessor compatible ADC	±0.5	20	NO	YES	Three-state data outputs	337
ZN502	10-bit microprocessor compatible ADC	±1.0	20	NO	YES	Three-state data outputs	337
ZN503	10-bit microprocessor compatible ADC	±0.5	20	NO	YES	Parallel and Serial three-state outputs, programmable input ranges	351
ZN504	10-bit microprocessor compatible ADC	±1.0	20	NO	YES	Parallel and Serial three-state outputs, programmable input ranges	351
ZN509	8-bit ADC with serial output	±0.5	8	YES	YES	Single supply operation low cost	372
ZN510	8-bit ADC with serial output	±1.0	8	YES	YES	Single supply operation low cost	372
ZN538	8-bit microprocessor compatible 8 channel data acquisition system	±0.5	16	NO	NO	Clock prescaler, 8 x 8 bit RAM	401
ZN539	8-bit microprocessor compatible 8 channel data acquisition system	±1.0	16	NO	NO	Clock prescaler, 8 x 8 bit RAM	401

* Assumes continuous tracking.

Product index - Data conversion (contd.)

High Speed ADCs

Type	Function	Guaranteed Min. Clock Rate	Process	Page
SP9756 [1]	6-bit wide input bandwidth ADC (250MHz - 3dB)	110MHz	Bipolar	41
SP94308	8-bit video system ADC	20MHz	Bipolar	87
SP973E8	8-bit flash ADC (ECL outputs)	30MHz	Bipolar	93
SP973T8	8-bit flash ADC (TTL/CMOS outputs)	30MHz	Bipolar	96
SP97504	4-bit expandable ADC (replaces SP9754)	110MHz	Bipolar	100
SP97508	8-bit flash ADC	110MHz	Bipolar	104

1. 6 and 8-bit accurate versions available.

ADC-DAC Combinations

Type	Function	Linearity Options (LSB)	Conversion Time ADC (μs)	Settling Time DAC (μs)	On-Chip Reference	Special Features	Page
ZN540	8-bit microprocessor compatible ADC with dual DAC	±0.5	5	1	YES	Programmable clock pre-divide. Double buffered latches	405
ZN541	8-bit microprocessor compatible ADC with dual DAC	±1.0	5	1	YES	Programmable clock pre-divide. Double buffered latches	405

ADC Support

Type	Function	Supply Voltage	Process	Page
SL9999	400MHz ADC driver/operational amplifier	+9V to -15V/ -5V to -15V	Bipolar	21
SP92701	Single subnanosecond ECL line receiver and driver	-5.2V	Bipolar	55

Digital Voltmeters

Type	Function	Conversion Time (sec)	Clock	Reference	Voltage Range	Special Features	Page
ZN450	3½ digit charge-balancing DVM	0.25	YES	YES	±199.9mV	Direct drive of LCDs, auto-zero	285
ZN451	3½ digit charge-balancing DVM	0.25	YES	YES	±1.999mV	Direct drive of LCDs, external auto-zero	307
ZNA216	3¾ digital dual-slope DVM	0.16	YES	NO	*	Direct drive of LED display, auto-zero	435

* Determined by user's analog circuits

High Speed Comparators

SP9680	Single comparator	+5V, -5.2V	±2.5V	6mV	4ns	-	Bipolar	29
SP9685	Single comparator	+5V, -5.2V	±2.5V	5mV	3ns	1ns (min)	Bipolar	31
SP9687	Dual comparator	+5V, -5.2V	±2.5V	5mV	3ns	1ns (min)	Bipolar	36
SP93802[1]	Dual comparator	+5V, -5.2V	±4V	±5mV	950ps	150ps (typ)	Bipolar	58
SP93804[1]	Quad comparator	+5V, -5.2V	±4V	±5mV	950ps	150ps (typ)	Bipolar	69
SP93808[1]	Octal comparator	+5V, -5.2V	±4V	±5mV	950ps	150ps (typ)	Bipolar	78

1. Includes Glitch capture.

Product index - Voltage references

Micropower Fixed Voltage References

REF12	1.26	90	4.0	Military	56	451
REF12Z	1.26	90	4.0	Industrial	56	451
REF25	2.50	60	1.5	Military	55	457
REF25Z	2.50	60	2.5	Industrial	70	457
REF25D	2.5	60	1.2	Industrial	70	464
REF50	5.00	60	3.5	Military	60	467
REF50Z	5.00	60	3.5	Industrial	70	467

SOT-23 Micropower Bandgap Voltage References

SR12D	1.2	90	2.5	40	474
SR25D	2.5	80	2.0	35	475

Product index - Voltage references

Fixed Voltage References (contd.)

		Operating Current (mA)		Slope Resistance (Ω)	Maximum Temperature Coefficient (ppm/°C)	Page
		Min.	Max.			
ZN404	2.45	2	120	0.4	145	476
ZN423	1.26	1.5	12	1.0	101	480
ZN458	2.45	2	120	0.2	99	485
ZN458A	2.45	2	120	0.2	49	485
ZN458B	2.45	2	120	0.2	29	485

Low Power Trimmable Voltage References

	Accuracy Options	Nominal Voltage (V)	Tolerance (%)	Trim Range (%)	Operating Current (mA) Min.	Operating Current (mA) Max.	Temp. Coef.	Slope Res. (Ω)	Temp. Range	Page
ZNREF 025	A1	2.50	1	±5	0.15	10.0	50.0	2	M	489
	C1		1						C	
	C2		2						C	
ZNREF 040	A1	4.01	1	±5	0.15	75.0	50.0	3	M	493
	C1		1						C	
	C2		2						C	
ZNREF 050	A1	4.90	1	±5	0.15	60.0	50.0	2	M	497
	C1		1						C	
	C2		2						C	
ZNREF 062	AB1	6.17	1	±5	0.15	50.0	50.0	3	*	501
	C1		1						C	
	C2		2						C	
ZNREF 100	A1	9.80	1	±2.5	0.15	50.0	50.0	4	M	505
	C1		1						C	
	C2		2						C	

M - Military C - Commerical * - 50°C to +110°C

Product List – alpha numeric

Data converters

Voltage references

Technical Data

1. Data converters

PLESSEY
Semiconductors

MV95308

8-BIT 30MHz DIGITAL TO ANALOG CONVERTER

The Plessey CMOS MV95308 has been designed for use in both video graphics and general digital television applications.

A very low external component count has been achieved by including the reference amplifier and reference voltage source on chip.

The device also contains an input register and registered video controls (Blank, Ref. White, Over Bright and Sync.). These control inputs and associated internal circuitry allow the MV95308 to be used in video graphics systems.

A control on/off input also allows the video pedestals to be overridden for conventional DAC applications.

This device is capable of directly driving 75Ω lines with standard (RS343) video levels.

Pullup resistors have been added to tie all unused inputs into their inactive states.

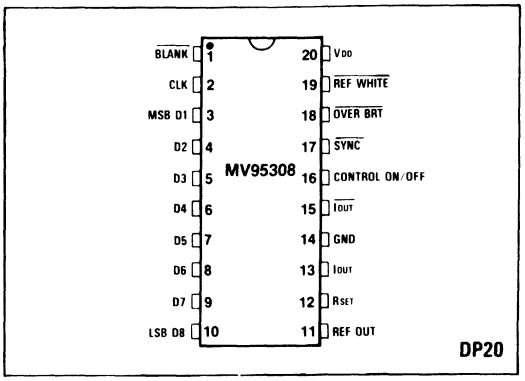


Fig.1 Pin connections - top view

ORDERING INFORMATION

MV95308 C DP (Industrial - Plastic DIL package)

FEATURES

- Low Power
- RS 343 Compatible Levels
- 20ns Settling to ±1 LSB
- On Chip Reference Voltage Source
- Graphics Ready
- Registered CMOS Inputs
- Guaranteed Monotonic
- Drives 75 Ohm Loads Directly
- Single 5V Power Supply
- 0°C to +70°C Temperature Range
- 7ns Output Rise Time (10% to 90%)

APPLICATIONS

- Data Conversion (General)
- Commercial TV
- Computer Graphics
- Instrumentation
- Test Equipment
- Waveform Synthesis

RECOMMENDED OPERATING CONDITIONS

R_{Load} (both outputs)	75Ω
V_{DD}	5.0V ± 0.5V
R_{SET} (graphics applications)	1.8k
R_{SET} (other DAC applications)	1.2k

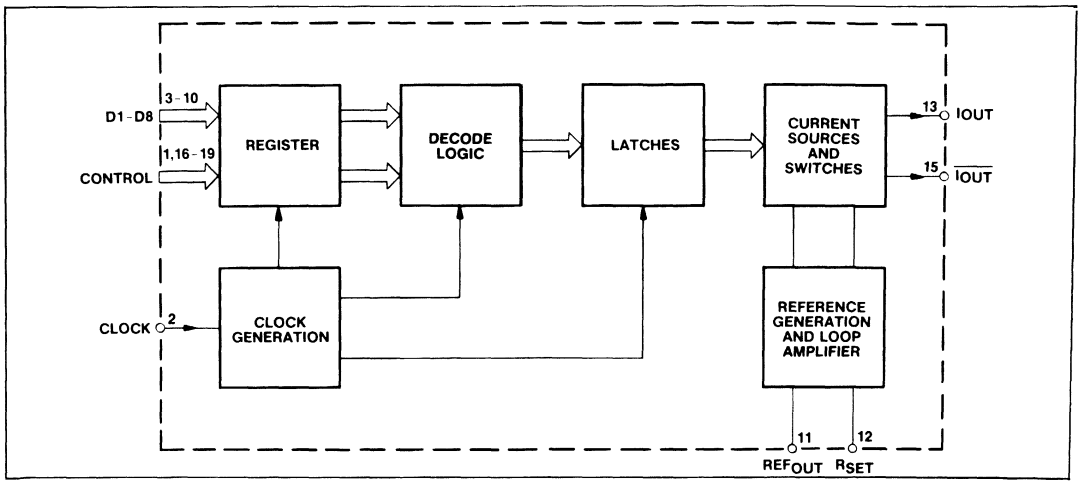


Fig.2 Block diagram of MV95308

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to 70°C, V_{DD} = +5V ± 0.5V

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	I_{DD}		58	70	mA	
Resolution		8			Bits	
Differential linearity				±1	LSB	R_{SET} = 1.8k
Integral linearity				±1	LSB	R_{SET} = 1.8k
Internal reference voltage	V_{ref}		1.0		V	Pin 11
Update rate	f_C	30	50		MHz	
Maximum output current	I_{out}	16			mA	
Clock minimum high	t_H	7			ns	
Clock minimum low	t_L	7			ns	
Input voltage high	V_{INH}	3			V	
Input voltage low	V_{INL}			1.2	V	
Data input current				20	μA	V_{IN} = 5.0V (At f_{max})
Output rise time	t_r			6	ns	10% to 90%
Settling time	t_{st}			20	ns	To ±1 LSB (75Ω load)
Clock to output delay	t_i		6		ns	Output at 10% full scale
Glitch energy			<100		ps V	

ABSOLUTE MAXIMUM RATINGS

Supply voltage	+7V
Storage temperature	-55°C to 125°C
Chip temperature	150°C

THERMAL CHARACTERISTICS

Chip to case θ_{JC}	30°C/W
Chip to ambient θ_{JA}	86°C/W

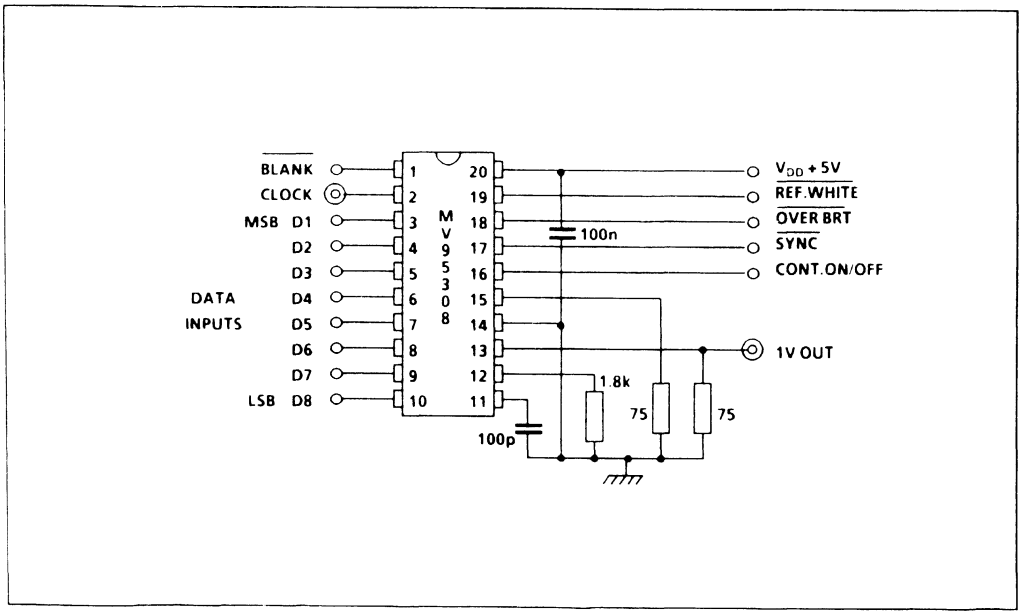


Fig.3 Applications test circuit

OPERATING NOTES

For optimum performance the device should be used in a low profile socket located over a solid ground plane. It is also important that the decoupling capacitor on pin 20 (V_{DD}) is located close to the device pin.

The outputs from this D to A converter are open drain current sources and hence require pulldown load resistors. The value of the load resistors will therefore determine the peak to peak output voltage from the DAC. This should not exceed 1.2V.

With all the data inputs high and a load of 75Ω on each output, a full scale output of 1V will be seen, (Fig.3). Fine adjustment of the output voltage can be achieved by varying the value of R_{SET}. Increasing R_{SET} will decrease the output amplitude.

For optimum slew rate and settling time, the unused output should be connected to ground via the same resistance as on the used output. This will balance the currents within the output stage of the DAC and hence provide cleaner switching.

Table 1 shows the output currents from the MV95308 with combinations of input data and control settings.

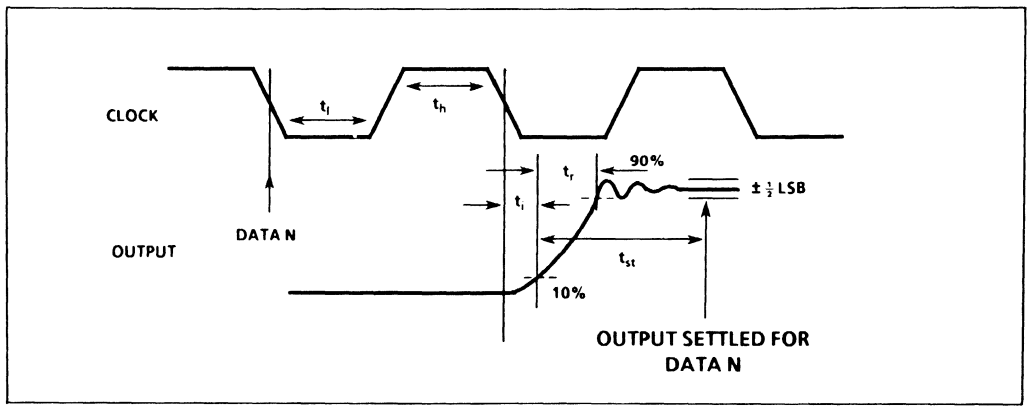


Fig.4 Timing diagram

Over Bright (Pin 18)

This control input has been introduced specially for graphics applications. It can be used to illuminate areas of graphics displays for borders, headings or cursors etc. When held low this input will cause a 10% of blank to full white level increase in the output current. Unlike the other control inputs the over bright input does not override the data. See Table 1.

Control On/Off (Pin 16)

This feature allows the MV95308 to be used in conventional DAC applications. When held low this pin will remove the sync pedestal and disable the Over Bright input. This allows the full 1V output range of the DAC to be used, 0 to 13mA into 75Ω. To gain this extra active output range, it is necessary to decrease the value of R_{SET} to 1.2kΩ.

With the control on/off pin low and all the data inputs high, the output current can be calculated from:

$$I_{out} = \frac{16 \times V_{ref}}{R_{SET}}$$

V_{ref} = 1.0V typ.

With the control on/off input open circuit the device will be configured for video graphics. In this mode and with all the data inputs high, the output current can be calculated from:

$$I_{out} = \frac{16 \times V_{ref}}{R_{SET}} + 4.533\text{mA}$$

V_{ref} = 1.0V typ.

Description	Control On/Off	Sync Bar	Blank Bar	Ref. White Bar	10 % Over.BRT Bar	Input Data	I_{OUT} (mA) R_{SET} = 1.8k
Ref. White +10 %	1	1	1	0	0	X	14.285
Ref. White	1	1	1	0	1	X	13.333
Full White	1	1	1	1	1	FF	13.333
Over Bright	1	1	1	1	0	Data	I_{CODE} +0.952
Full Black	1	1	1	1	1	00	4.533
Blank	1	1	0	X	X	X	3.183
Data-Sync	1	0	1	1	1	Data	I_{CODE} -3.813
Sync	1	0	0	X	X	X	0.000
Control On/Off	0	X	1	1	X	Data	I_{CODE} (0 to 13mA) R_{SET} = 1.2k

Table 1

X = Don't Care '1' = +5V, '0' = 0V, FF = All '1's

PLESSEY
Semiconductors

MV95408

8-BIT 50MHz DIGITAL TO ANALOG CONVERTER

The Plessey CMOS MV95408 has been designed for use in both video graphics and general high speed DAC applications.

Very low external component count is achieved as the device contains both an on chip reference amplifier and reference voltage source.

The device also contains an input register and registered video controls (Blank, Ref. White, Over Bright and Sync.). These control inputs and associated internal circuitry allow the MV95408 to be used in video graphics systems.

A control on/off input also allows the video pedestals to be overridden for conventional DAC applications.

This device is capable of directly driving 75Ω lines with standard (RS343) video levels.

Pullup resistors have been added to tie all unused inputs into their inactive states.

ORDERING INFORMATION

MV95408 B DP (Industrial - Plastic DIL package)

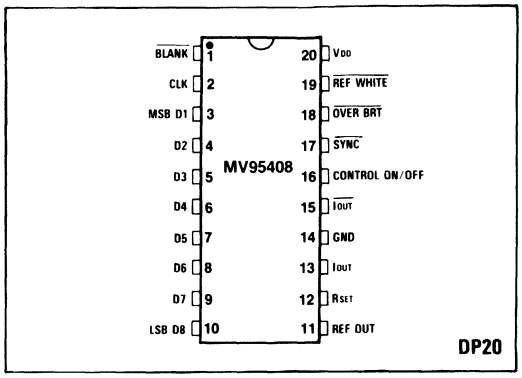


Fig.1 Pin connections - top view

FEATURES

- Low Power
- RS 343 Compatible Levels
- Differential Linearity < ±½ LSB
- 20ns Settling to ±½ LSB
- On Chip Reference Voltage Source
- Graphics Ready
- Registered CMOS Inputs
- Guaranteed Monotonic
- Drives 75 Ohm Loads Directly
- Single 5V Power Supply
- -40°C to +85°C Temperature Range
- ≤ 6ns Output Rise Time (10% to 90%)

APPLICATIONS

- Data Conversion (General)
- Commercial TV
- Computer Graphics
- Instrumentation
- Test Equipment
- Waveform Synthesis

RECOMMENDED OPERATING CONDITIONS

R_{Load} (both outputs)	75Ω
V_{DD}	5.0V ± 0.5V
R_{SET} (graphics applications)	1.8k
R_{SET} (other DAC applications)	1.2k

ABSOLUTE MAXIMUM RATINGS

Supply voltage	+7V
Storage temperature	-55°C to 125°C
Chip temperature	<150°C

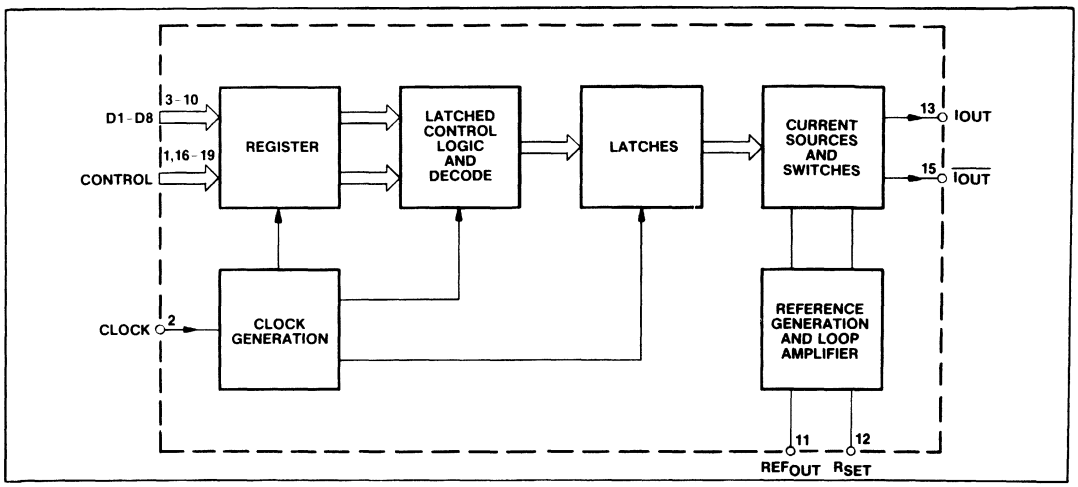


Fig.2 Block diagram of MV95408

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} -40°C to +85°C, V_{DD} +5V ± 0.5V

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	I_{DD}		58	70	mA	
Resolution		8			Bits	
Differential linearity				±½	LSB	R_{SET} = 1.8k
Integral linearity				±½	LSB	R_{SET} = 1.8k
Internal reference voltage	V_{ref}		1.0		V	Pin 11
Update rate	f_C	50	75		MHz	
Maximum output current	I_{out}	16			mA	
Clock minimum high	t_H	6			ns	
Clock minimum low	t_L	6			ns	
Input voltage high	V_{INH}	3			V	
Input voltage low	V_{INL}			1.2	V	
Data input current				20	μA	V_{IN} = 5.0V (At f_{max})
Output rise time	t_r			5.5	ns	10% to 90%
Settling time	t_{st}			20	ns	To ±½ LSB (75Ω load)
Clock to output delay	t_l		6		ns	Output at 10% full scale
Glitch energy			<100		ps V	

THERMAL CHARACTERISTICS

Chip to case θ_{JC}	30°C/W
Chip to ambient θ_{JA}	86°C/W

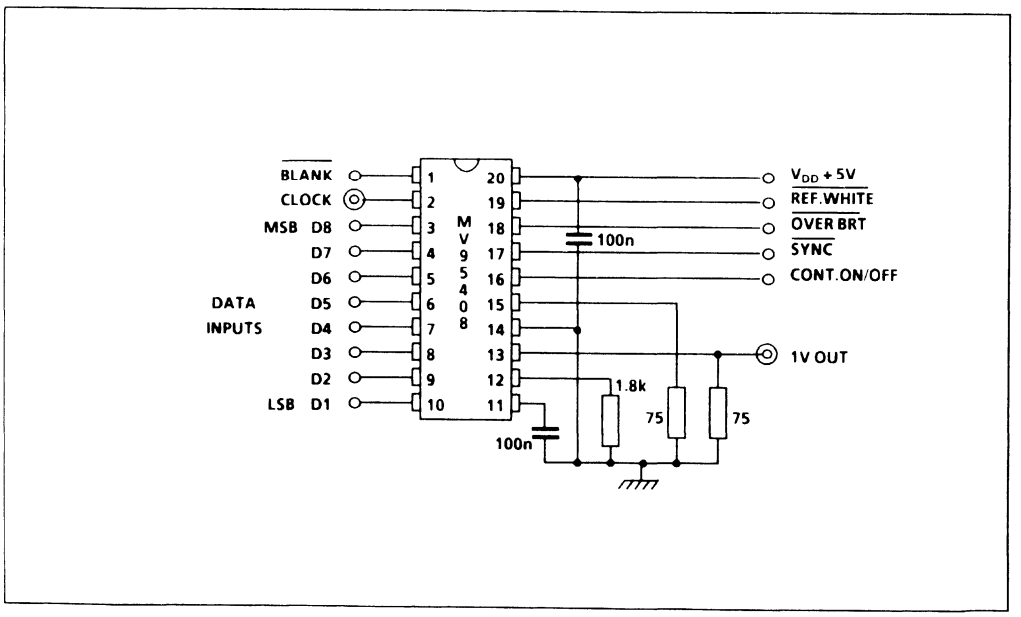


Fig.3 Applications test circuit

OPERATING NOTES

For optimum performance the device should be used in a low profile socket located over a solid ground plane. It is also important that the decoupling capacitor on pin 20 (V_{DD}) is located close to the device pin. For good stability the capacitance on pin 12 (R_{SET}) should be kept to a minimum (<10pF).

The outputs from this D to A converter are open drain, current sources and hence require pulldown load resistors. The value of the load resistors will therefore determine the peak to peak output voltage from the DAC. This should not exceed 1.2V.

With all the data inputs high and a load of 75Ω on each output, a full scale output of 1V will be seen, (Fig.3). Fine adjustment of the output voltage can be achieved by varying the value of R_{SET}. Increasing R_{SET} will decrease the output amplitude.

For optimum slew rate and settling time, the unused output should be connected to ground via the same resistance as on the used output. This will balance the currents within the output stage of the DAC and hence provide cleaner switching.

Table 1 shows the output currents from the MV95408 with combinations of input data and control settings.

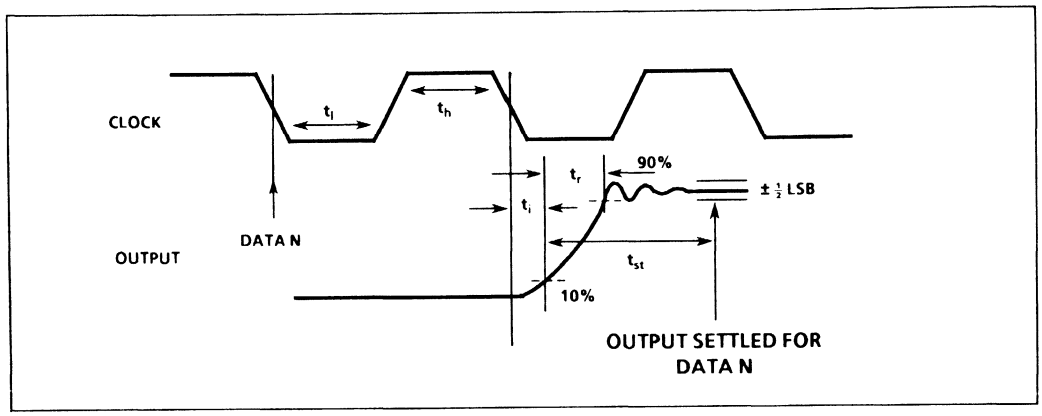


Fig.4 Timing diagram

Over Bright (Pin 18)

This control input has been introduced specially for graphics applications. It can be used to illuminate areas of graphics displays for borders, headings or cursors etc. When held low this input will cause a 10% of blank to full white level increase in the output current. Unlike the other control inputs the over bright input does not override the data. See Table 1.

Control On/Off (Pin 16)

This feature allows the MV95408 to be used in conventional DAC applications. When held low this pin will remove the sync pedestal and disable the Over Bright input. This allows the full 1V output range of the DAC to be used, 0 to 13mA into 75Ω. To gain this extra active output range, it is necessary to decrease the value of R_{SET} to 1.2kΩ.

With the control on/off pin low and all the data inputs high, the output current can be calculated from:

$$I_{out} = \frac{16 \times V_{ref}}{R_{SET}}$$

$$V_{ref} = 1.0V \text{ typ.}$$

With the control on/off input open circuit the device will be configured for video graphics. In this mode and with all the data inputs high, the output current can be calculated from:

$$I_{out} = \frac{16 \times V_{ref}}{R_{SET}} + 4.533mA$$

$$V_{ref} = 1.0V \text{ typ.}$$

Description	Control On/Off	Sync Bar	Blank Bar	Ref. White Bar	10 % Over.BRT Bar	Input Data	I_{OUT} (mA) R_{SET} = 1.8k
Ref. White +10 %	1	1	1	0	0	X	14.285
Ref. White	1	1	1	0	1	X	13.333
Full White	1	1	1	1	1	FF	13.333
Over Bright	1	1	1	1	0	Data	I_{CODE} +0.952
Full Black	1	1	1	1	1	00	4.533
Blank	1	1	0	X	X	X	3.183
Data-Sync	1	0	1	1	1	Data	I_{CODE} -3.813
Sync	1	0	0	X	X	X	0.000
Control On/Off	0	X	1	1	X	Data	I_{CODE} (0 to 13mA) R_{SET} = 1.2k

Table 1 Control inputs

X Don't Care '1' = +5V, '0' = 0V, FF = All '1's

PLESSEY
Semiconductors

SL9999

400MHz ADC DRIVER-AMPLIFIER

The Plessey SL9999 is a monolithic high speed high performance operational amplifier. Although primarily intended to drive the inputs of analog to digital converters, the device is capable of driving any other circuit including those that present a low impedance and high capacitive load. Many other internal features such as programmable open loop gain, programmable output current, internal band gap voltage reference, DC buffer and output DC offset circuitry give the device the flexibility for use in a wide range of applications.

ORDERING INFORMATION

SL9999C DP (Commercial Plastic DIL 0° to 70°C)
SL9999B DG (Commercial Ceramic DIL -40° to +85°C)
SL9999B LC (Commercial LCC -40° to +85°C)
SL9999NA IC (Naked Chip)

FEATURES

- Gain-Bandwidth Product 2GHz at 20dB
- Unity Gain-Bandwidth 400MHz
- Slew Rate 1300V/ μs Rising (typ)
- Slew Rate 630/V μs Falling (typ)
- ±50mA Output Current (Programmable)
- Non-saturating
- High Output Drive
- On-chip LF Buffer for Applying DC Offset
- Flexible Supply Range:
  V_{CC} = +8V to +12V
  V_{EE} = -4.5V to -5.5V
- Output Signal Handling (V_{CC} = +12V, V_{EE} = -5.2V)
  V_{out} = 6V p-p (max.)
- Input Signal Handling (V_{CC} = +12V, V_{EE} = -5.2V)
  V_{in} = +2.8V to -2.5V (max.)

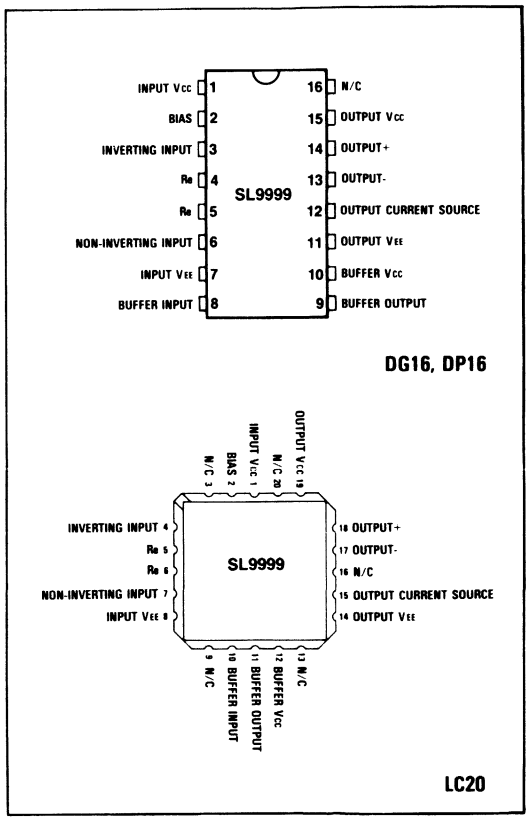


Fig.1 Pin connections - top view

APPLICATIONS

- High Speed Flash ADC Driver
- Wideband, Buffer/Level Shifter
- Wideband IF Amplification
- Video Amplifier/Line Driver
- Fast Settling Pulse Amplifier
- High Speed Op-Amp Applications

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE})	20V
Input Voltage (Inv I/P to Non-Inv I/P)	±5V
Storage Temperature	-65°C to +175°C
Chip Operating Temperature	+175°C
Operating Temperature: DIL	-40°C to +85°C
Thermal Resistances:	
DG Chip-to-Ambient: DIL	120°C/W
DG Chip-to-Case: DIL	40°C/W
DP Chip-to-Ambient: DIL	100°C/W
DP Chip-to-Case: DIL	40°C/W

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} 25° C, V_{CC} + 12V, V_{EE} -5V, Test circuit Fig.3.

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Equivalent input noise		33		nV/√Hz	50Ω source impedance, BW = 100MHz
Supply current (no load)		35	43	mA	V_{CC} = +12V, V_{EE} = -5V
Gain-bandwidth product		2		GHz	×10 gain
Unity gain bandwidth (small sig)		400		MHz	R_e = 820Ω, R_L = 50Ω
Slew rate RISING	800	1300		V/μs	R_L = 50Ω
Slew rate FALLING	500	630		V/μs	R_L = 50Ω
Settling time		24		ns	To 1% (×10 gain)
Open loop gain		65		dB	50Ω load
Maximum I_{out}			±50	mA	Programmable See Application Notes
Output bias current	15	17	20	mA	Pin 12 O/C
Supply line rejection		40		dB	Referred to input
Supply voltage V_{EE} to V_{CC}	12.5		18	V	
Common mode rejection	55			dB	50Ω load
Input offset (Note 1)		±5	±15	mV	R_e = 100Ω
Input bias current		4.5	18	μA	
Buffer bandwidth		60		MHz	-3dB R_L = 1kΩ (Pulldown resistor)
Buffer output current			15	mA	

NOTE
Input offset is dependent on R_e. For lowest offset R_e = 0 ohms.

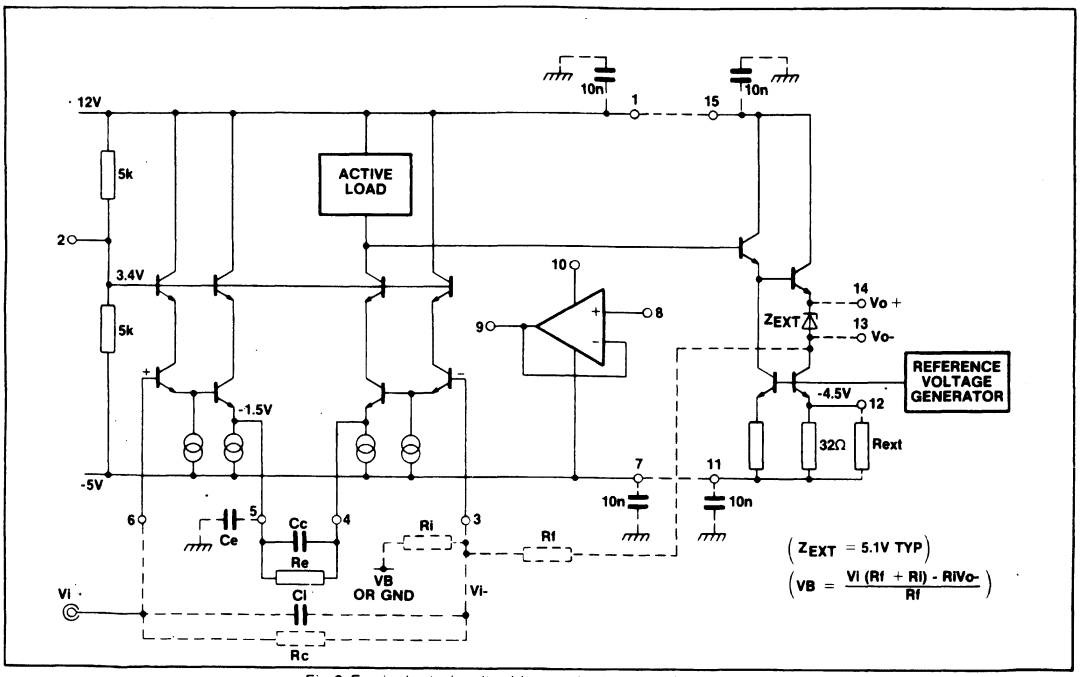


Fig.2 Equivalent circuit with standard external components

APPLICATION NOTES

The SL9999 may be used as a high frequency amplifier in any of the usual op-amp configurations (amplifiers, integrators, etc.).

In most applications, the output of the SL9999 is taken from pin 13 (V_{out-}), DC level shifting can be obtained by applying feedback from pin 13 to pin 3 and taking the output from pin 14 (V_{out+}, see Fig.2). Alternatively, a DC offset can be applied through the low-drift on-chip buffer (pins 8 and 9) to V_B.

The Zener diode between pins 13 and 14 can also be divided into smaller value Zeners or resistors to give a range of DC levels at the output.

Biasing Conditions (25° C)

For undistorted outputs the peak signal voltages on Vo +, Vo- and the inputs should comply with the following conditions:

A. $Vo+_{(MIN)} \geqslant \frac{V_{CC} + V_{EE}}{2} - 1.4V$

B. $Vo+_{(MAX)} \leqslant V_{CC} - 4.0V$

C. $Vo-_{(MIN)} \geqslant V_{EE} + 1.4V$

D. $Vi+ \text{ and } Vi- \leqslant \frac{V_{CC} + V_{EE}}{2} - 0.9V$

E. $Vi+ \text{ and } Vi- \geqslant V_{EE} + 3.2V$

Bias voltage values at several nodes are indicated on Fig.2.

R_{ext} is connected from pin 12 to pin 11 (V_{EE}) to increase output bias current I_{out}. This current should not exceed 50mA. The value of R_{ext} is calculated as follows:

$$R_{ext} \equiv \left[\frac{500}{I_{out} - 16}\right] \Omega$$

where I_{out} is in mA.

The on-chip LF buffer has a small-signal bandwidth of 60MHz with 1kΩ load, and has an input/output signal handling capability of 8V. The output can deliver 15mA; an external pull-down resistor is required.

High Frequency Stability

All component leads should be kept as short as possible, particularly at the summing junction. Also it is important to keep stray capacitance at the summing junction to an absolute minimum.

A ground plane should be used to minimise any earth induced currents between the input and output circuits.

The use of good power supply bypass capacitors (10nF Ceramic) will improve the overall performance. They should be close to the device supply pins. We also recommend electrolytic capacitors in parallel with Ceramic for supply decoupling.

Locate the signal source and load close to the circuit with proper termination - for 50Ω source use a 50Ω bead resistor. Other resistors should be carbon composition.

Voltage Gain

Stable closed loop operation is ensured by changing the value of the degeneration resistor (R_e) between pins 4 and 5 according to the selected closed loop gain. As closed loop gain decreases the value of R_e should be increased.

A graph of recommended R_e with gain is given in Fig.4.

Power Dissipation

A Zener diode is used between pins 13 and 14 to dissipate power externally and to provide DC offset of the output.

For -5V, +12V range a 4.7V to 5.1V Zener may be used.

For lower cost applications a bypassed resistor can conveniently replace the Zener diode. Its value may be calculated from the voltage drop and current through the output stage. For example, for 15mA output current a 330Ω resistor could be used.

Although some power is dissipated in the external Zener, a heatsink on the SL9999 will be necessary if power >800mW is to be dissipated.

Bandwidth Compensation

Bandwidth at higher gains can be improved by a capacitor (C_c) across the degeneration resistor R_e. For example, a non-inverting closed loop gain of 10, 10pF will increase the bandwidth to 280MHz at 50Ω load condition.

A decoupling capacitor (C_e) from pin 5 will compensate the first pole roll-off and hence reduce the noise bandwidth. For a 200MHz bandwidth an 18pF capacitor may be used with the suggested PCB layout on page 6.

A capacitor (C_i) and resistor (R_c) of suitable value between the two inputs will reduce high frequency peaking.

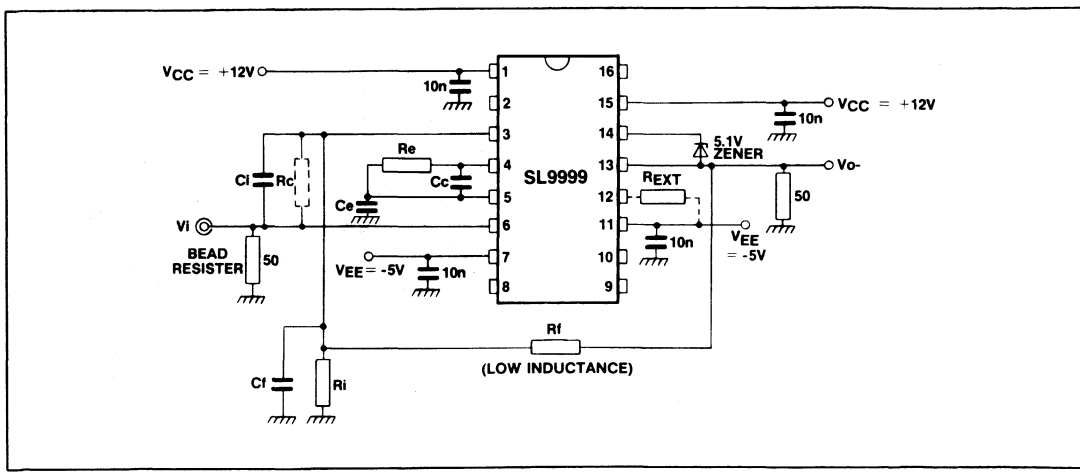


Fig.3 Test/applications circuit for 50Ω load, 10nF ceramic decoupling capacitors

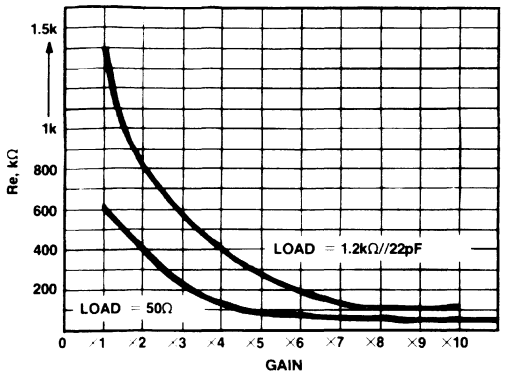


Fig.4 Typical closed loop gain v. minimum value of degeneration resistor R_e

NOTE: Input offset is proportional to R_e value

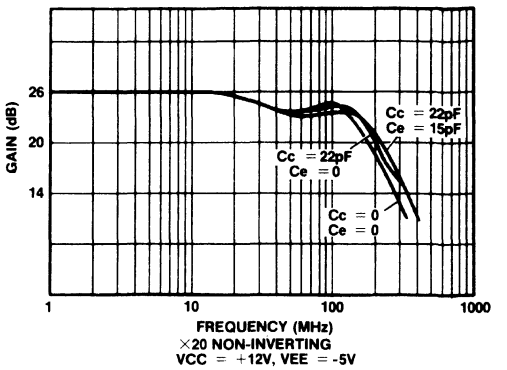


Fig.5 Typical frequency response for the test circuit of Fig.3, ×20 gain, non-inverting, 50Ω load, R_f = 10.6kΩ, R_1 = 560Ω, R_e = 22Ω.

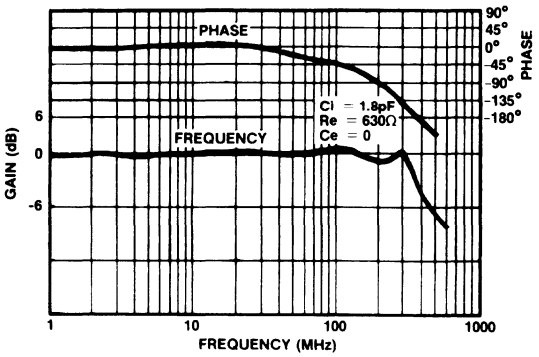


Fig.6 Typical frequency/phase performance graphs for the circuit of Fig.3, ×1 gain, non-inverting, 50Ω load, R_f = 560Ω, R_1 = ∞.

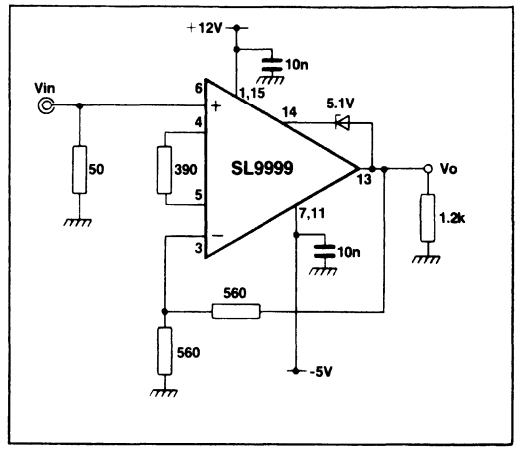


Fig.7 Test circuit for large and small signal response, and slew rate (see Figs. 8 to 11). V_{CC} = +12V, V_{EE} = -5V.

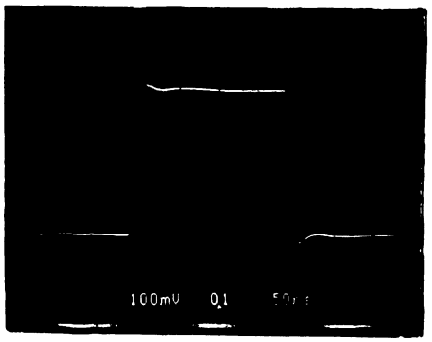


Fig.8 Small signal response

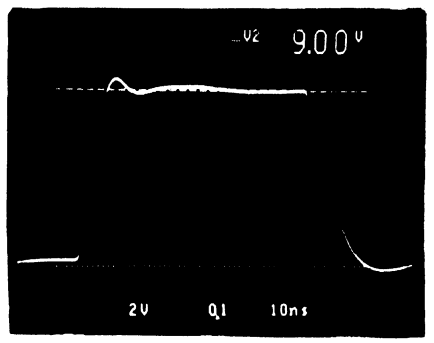


Fig.9 Large signal response

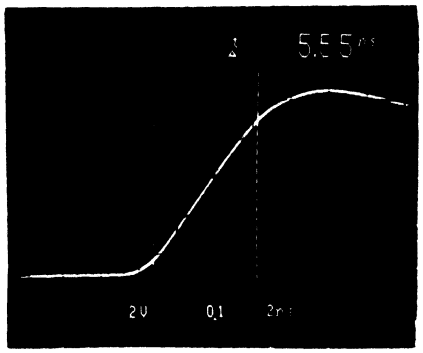


Fig.10 Rising edge 10% to 90% points 1300V/μs

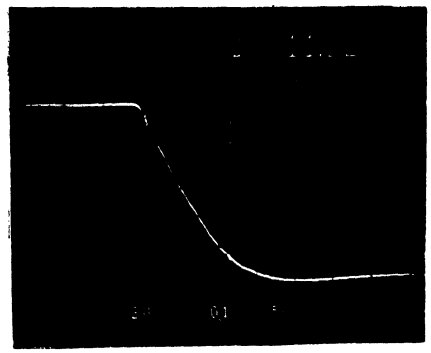


Fig.11 Falling edge 10% to 90% points 630V/μs

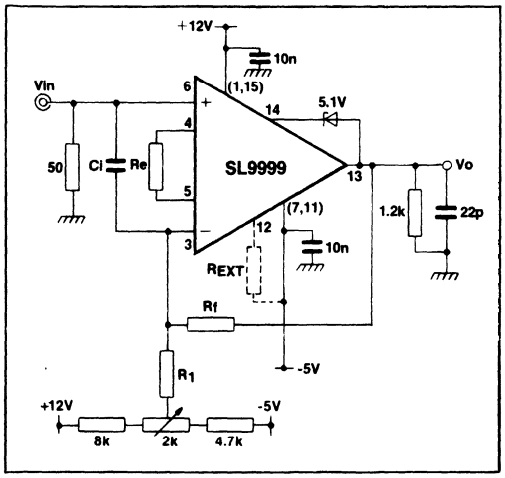


Fig.12 Application circuit for capacitor load e.g. high speed flash ADC input

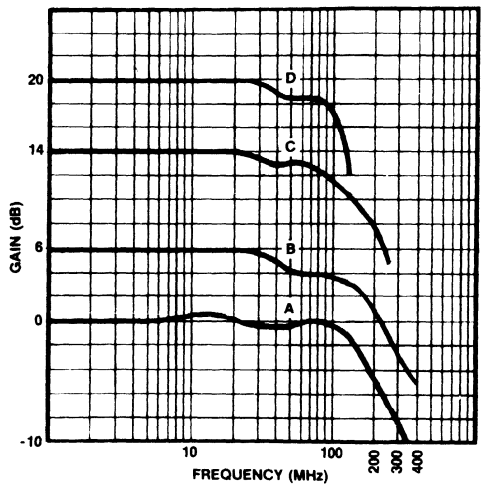


Fig.13 Typical frequency response plots for the circuit of Fig.12 (Load 22pF//1.2kΩ).

TYPICAL APPLICATION

Response (see Fig.13)	Gain	R_f (Ω)	R_i (Ω)	R_e (Ω)	C_f (Pf)	R_{ext} (Ω)	VO/P (p-p)	V_{CC} (V)	V_{EE} (V)
A	×1	2.2k	∞	1.8k	0	∞	1	+12	-5
B	×2	560	560	1.2k	18	50	2	+12	-5
C	×5	2.2k	560	270	10	∞	1	+12	-5
D	×10	5.6k	560	68	0	10	1	+12	-5

Table 1 Recommended components values for the test circuit of Fig.12

NOTE
C_f and C_i are dependent on layout and used to compensate the effects of strays.

For applications that require accurate gain flatness over the full frequency range, the inverting mode of operation is recommended. See Fig.14.

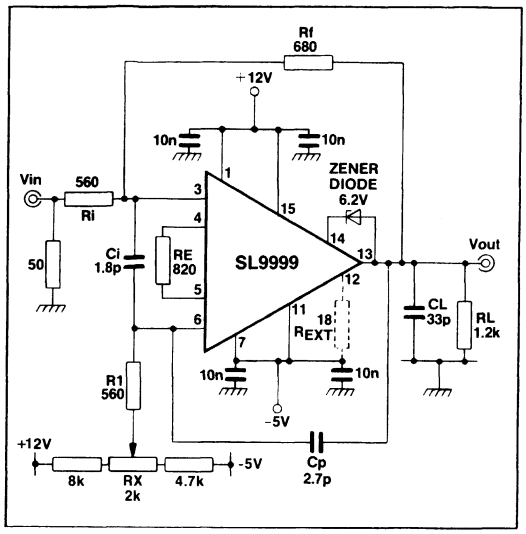


Fig.15 Typical test/applications circuit for inverting mode. Load 33pF/1.2kΩ.

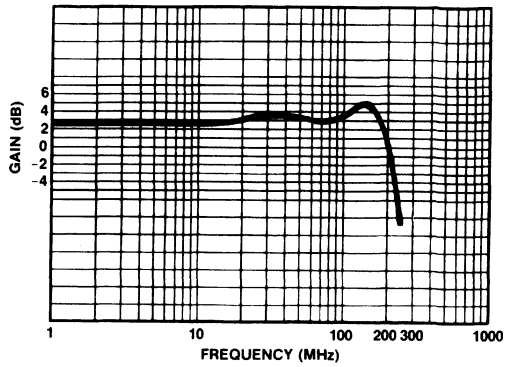
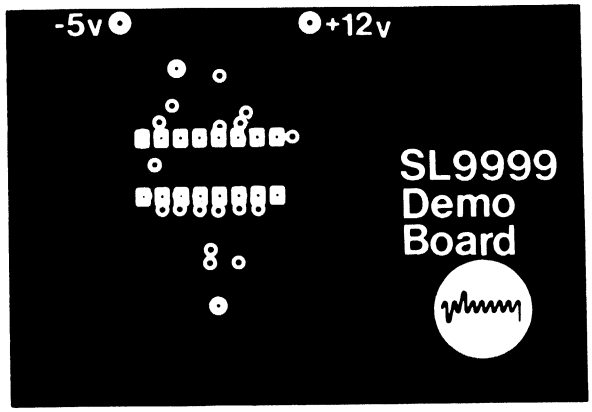
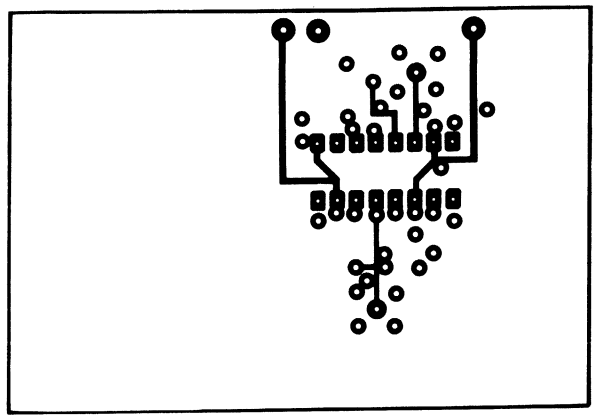


Fig.16 Frequency response of SL9999 with C_L = 33pF, C_p = 2.7pF, R_f = 680, R_L = 1.2k, C_i = 1.8pF, R_1 = 560, V_O = 1V p-p (See Test Circuit of Fig.15)

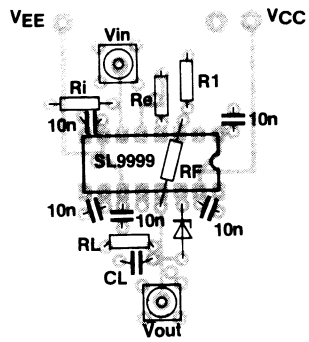
CONSTRUCTION



(a) SL9999 ground plane, component side

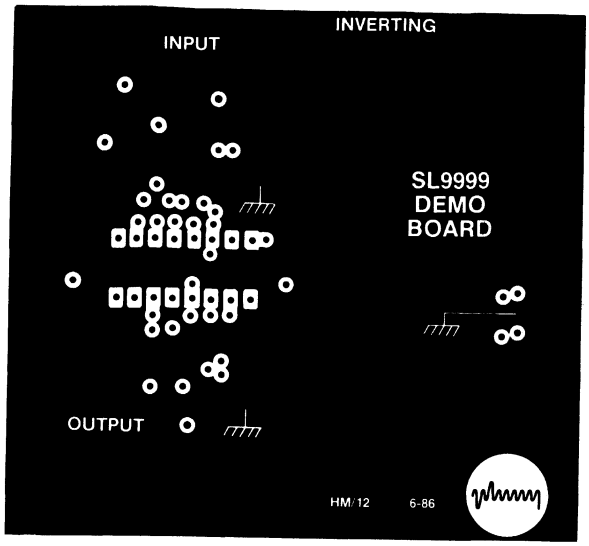


(b) SL9999 board, track side

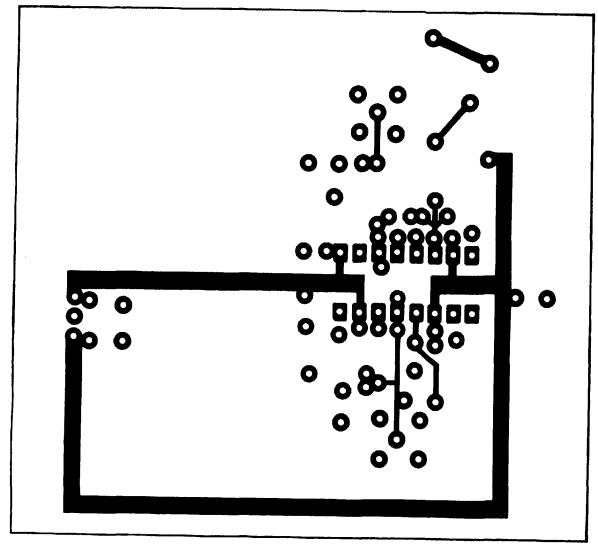


(c) Component location. NOTE: I/P and O/P are sub-vis type 50Ω connectors.

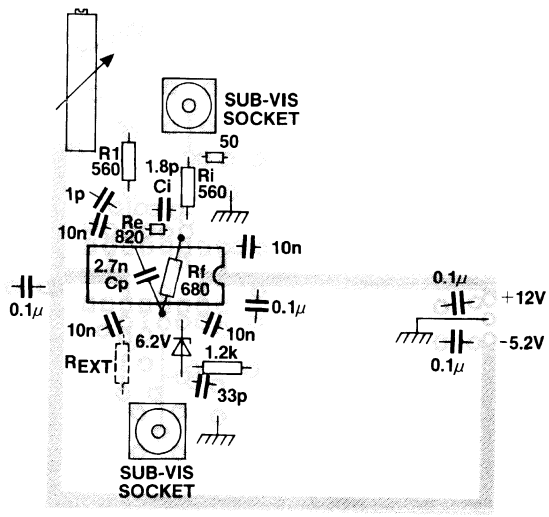
Fig.16 PCB layout for SL9999 demonstration board (Fig.12) viewed from component side and underside



(a) SL9999 ground plane, component side



(b) SL9999 board, track side



(c) Component location (1:1 scale)

Fig.17 PCB layout for SL9999 demonstration board. NOTE: I/P and O/P are sub-vis type 50Ω connectors. Rf and C f are on the track side. Gold socket pins to mount SL9999 for test circuit

PLESSEY
Semiconductors

SP9680

ULTRA FAST COMPARATOR

The SP9680 is an ultra fast comparator manufactured using a high performance bipolar process which makes possible very short propagation delays (2.4ns typ.).

The circuit has differential inputs and complementary ECL outputs, capable of driving 50 Ω lines.

The device is manufactured in a low cost mini-dip package and is intended as an alternative to the faster SP9685 in applications where performance premium and the latch facility are not required.

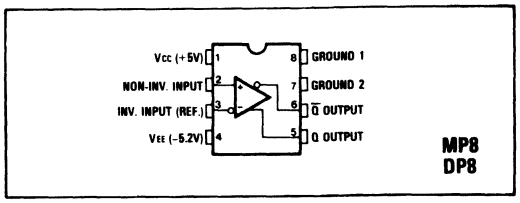
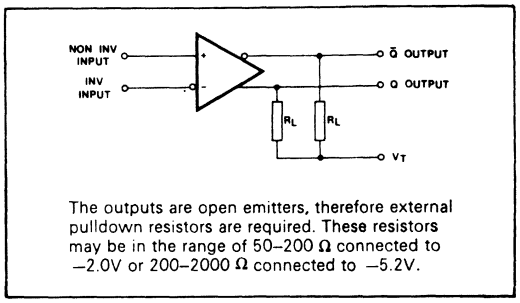


Fig. 1 Pin connections

FEATURES

- Propagation Delay 2.4ns Typ.
- Complementary ECL Outputs
- 50 Ω Line Driving Capability
- Excellent Common Mode Rejection
- 8-Lead Plastic Package
- Supply Voltages +5, −5.2V
- Operating Temperature Range −30°C to +70°C



The outputs are open emitters, therefore external pulldown resistors are required. These resistors may be in the range of 50–200 Ω connected to −2.0V or 200–2000 Ω connected to −5.2V.

Fig. 2 Functional diagram

ORDERING INFORMATION

SP9680DP (Industrial - Plastic DIL package)
SP9680MP (Industrial - Miniature Plastic package)

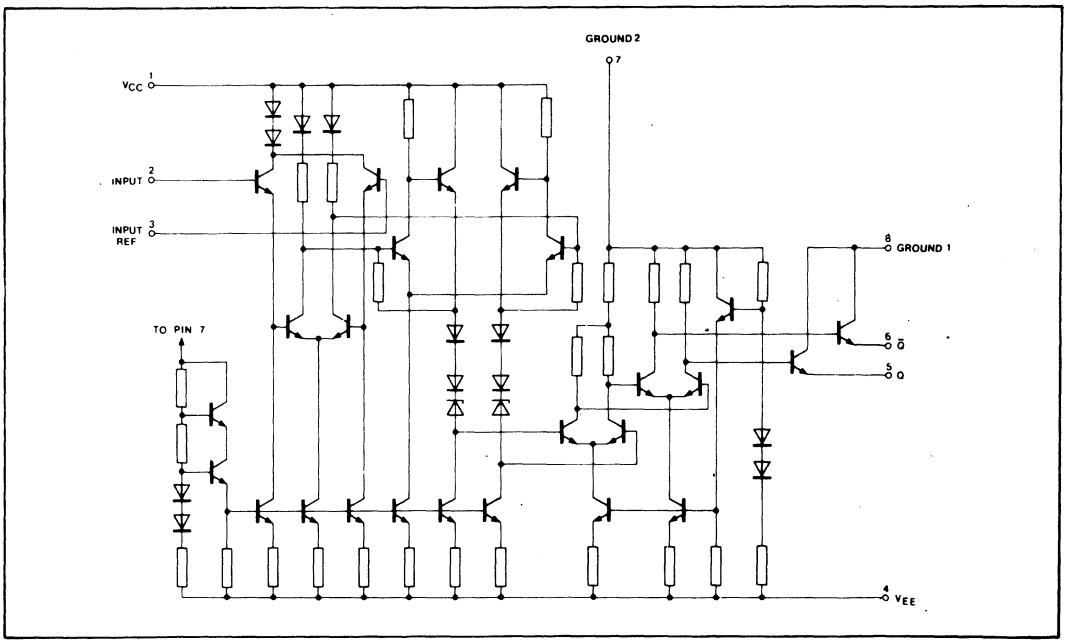


Fig. 3 SP9680 circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 25 C
V_{CC} = 5.00V 0.25V
V_{EE} = −5.2V 0.25V
R_L = 50 Ω
V_T = −2.0V (See Fig. 2)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input offset voltage	−6		+6	mV	Rs <100 Ω
Input bias current		20	40	μA	
Input offset current			10	μA	
Supply current I_{CC}		18	25	mA	
I_{EE}		22	35	mA	
Total power dissipation		200	300	mW	
Input to Q output delay		2.4	4	ns	} 100mV pulse,10mV overdrive
Input to $\overline{Q}$ output delay		2.4	4	ns	
Common mode range	−2		+2	V	
Common mode rejection ratio		80		dB	
Output logic levels					
Output HIGH	−0.96		−0.81	V	
Output LOW	−1.85		−1.65	V	
Input capacitance		3.5		pF	
Input resistance	50			kΩ	
Operating temperature range	−30		+70	°C	

Thermal characteristics θ_{JA} = 111°C/W
θ_{JC} = 71°C/W

ABSOLUTE MAXIMUM RATINGS

Positive supply voltage V_{CC} +6V
Negative supply voltage V_{EE} −6V
Output current 30mA
Input voltage ±3V
Differential input voltage 3.5V
Storage temperature range -55°C to +150°C
Operating junction temperature <150°C

PLESSEY
Semiconductors

SP9685

ULTRA FAST COMPARATOR

The SP9685 is an ultra-fast comparator manufactured with a high performance bipolar process which makes possible very short propagation delays (2.2ns typ.). The circuit has differential inputs and complementary outputs fully compatible with ECL logic levels. The output current capability is adequate for driving 50Ω terminated transmission lines. The high resolution available makes the device ideally suited to analog-to-digital signal processing applications.

A latch function is provided to allow the comparator to be used in a sample-hold mode. When the latch enable input is ECL high, the comparator functions normally. When the latch enable is driven low, the outputs are forced to an unambiguous ECL logic state dependent on the input conditions at the time of the latch input transition. If the latch function is not used, the latch enable may be connected to ground.

The device is pin compatible with the AM685 but operates from conventional +5V and -5.2V rails. It is pin and voltage compatible with AD9685.

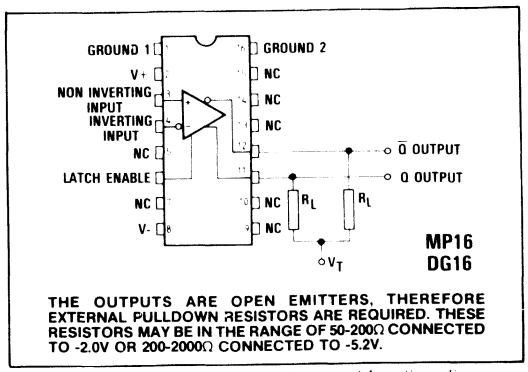


Fig.1 DIL pin connections (top view) and function diagram

FEATURES

- Propagation Delay 2.2ns Typ.
- Latch Set-up Time 1ns Max.
- Complementary ECL Outputs
- Supply +5V, -5.2V (±0.25V)
- 50 ohm Line Driving Capability
- Excellent Common Mode Rejection
- Operating Temperature Range :
  SP9685 — -30°C to +85°C
  SP9685AC — -55°C to +125°C
- Pin Compatible with AD9685
- Pin Compatible with AM685 — But Faster

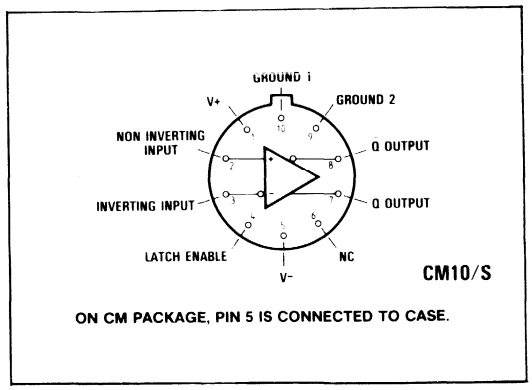


Fig.2 Metal package (CM10/S) pin connections (top view)

APPLICATIONS

- Ultra High Speed A/D Converter
- Ultra High Speed Line Receivers
- Peak Detectors
- Threshold Detectors

ORDERING INFORMATION

SP9685CM (Industrial - Cylindrical Metal package)
SP9685DG (Industrial - Ceramic DIL package)
SP9685BB DG (Plessey High Reliability Ceramic DIL package)
SP9685MP (Industrial - Miniature Plastic package)
SP9685AC DG (Military - Ceramic DIL package)

NOTE:
The AC version of this product conforms to MIL-STD-883C CLASS B screening and is covered by separate data which observes the change notification requirements of MIL-M-38510 and is published in the 'MIL-STD-883C CLASS B Integrated Circuit' Handbook. Please consult your nearest Plessey sales office.

ABSOLUTE MAXIMUM RATINGS

Postive supply voltage	6V	Storage temperature range	-55° C to +150° C
Negative supply voltage	-6V	Operating junction temperature	<175° C
Output current	30mA	Lead temperature (soldering 60 sec)	300° C
Input voltage	±3V	Vibration	196m/s²
Differential input voltage	3.5V	Shock	14700m/s² peak 0.5ms duration
Power dissipation	350mW		

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} 5.00V: V_{EE} = -5.2V: R_L 50Ω: V_T = 2.0V (see Fig.1)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input offset voltage	-5		+5	mV	R_S < 100Ω 25°C
	-7		+7	mV	R_S < 100Ω
Input bias current			20	μA	25°C
			30	μA	
Input offset current			5	μA	25°C
			8	μA	
Supply current I_{EE}			34	mA	25°C
			36	mA	
Supply current I_{CC}			23	mA	25°C
			24	mA	25°C
Total power dissipation	210		350	mW	25°C Note 3
Common mode range	-2.5		+2.5	V	
Output logic levels					
Output high	-0.96		-0.81	V	25°C
	-1.045		-0.875	V	T_{amb} = Min.
	-0.89		-0.70	V	T_{amb} = Max.
Output low	-1.85		-1.65	V	25°C
	-1.89		-1.65	V	T_{amb} = Min.
	-1.83		-1.575	V	T_{amb} = Max.
Min. latch set up time			1	ns	Notes 1, 2, 3 25°C
			2	ns	
Input to output delay			3	ns	Note 1, 3 (Q and $\overline{Q}$) 25°C
			4	ns	
Latch to output delay			3	ns	Notes 1, 2, 3 (Q and $\overline{Q}$) 25°C
			4.5	ns	
Minimum latch pulse width			3	ns	Note 3 25°C
Minimum hold time			1	ns	Note 3 25°C
Max. input capacitance		3		pF	Note 3 25°C
Input resistance	60		kΩ		Note 3 25°C
Common mode rejection ratio	70			dB	Note 3 25°C
Supply voltage rejection ratio	50			dB	Note 3 25°C

NOTES
1 -100mV pulse with 10mV overdrive
2 Switching measurements involving the latch are particularly difficult to perform and cannot be tested in production. Circuit analysis shows that at least 95% of devices will meet these specifications
3 Guaranteed but not tested

Thermal characteristics

CM10	θ_{JA}	220°C/W
	θ_{JC}	65°C/W
DG16	θ_{JA}	120°C/W
	θ_{JC}	40°C/W
LC20	θ_{JA}	73°C/W
	θ_{JC}	22°C/W

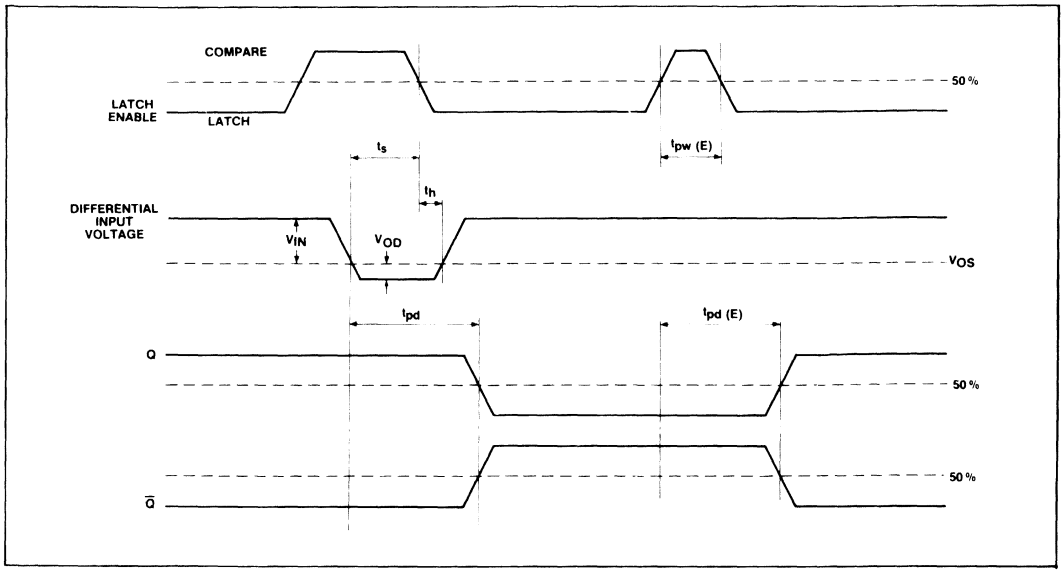


Fig.3 Timing diagram

OPERATING NOTES

Timing diagram

The timing diagram, Fig. 3, shows in graphic form a sequence of events in the SP9685. It should not be interpreted as 'typical' in that several parameters are multi-valued and the worst case conditions are illustrated. The top line shows two latch enable pulses, high for 'compare', and low for latch. The first pulse is used to highlight the 'compare' function, where part of the input action takes place in the compare mode. The leading edge of the input signal, here illustrated as a large amplitude, small overdrive pulse switches the comparator over after a time t_{pd}. Output Q and $\overline{Q}$ transitions are essentially similar in timing. The input signal must occur at a time t_s before the latch falling edge, and must be maintained for a time t_h after the latch falling edge, in order to be acquired. After t_h, the output ignores the input status until the latch is again strobed. A minimum latch pulse width $t_{pw(E)}$ is required for the strobe operation, and the output transitions occur after a time $t_{pd(E)}$.

Measurement of propagation and latch delays

A simple test circuit is shown in Fig.4. The operating sequence is:

1. Power up and apply input and latch signals. Input = 100mV square wave, latch ECL levels. Connect monitoring scope(s).
2. Select 'offset null'.
3. Adjust offset null potentiometer for an output which switches evenly between states on clock pulses.
4. Measure input/output and latch/output delays at 5mV offset, 10mV offset and 25mV offset.

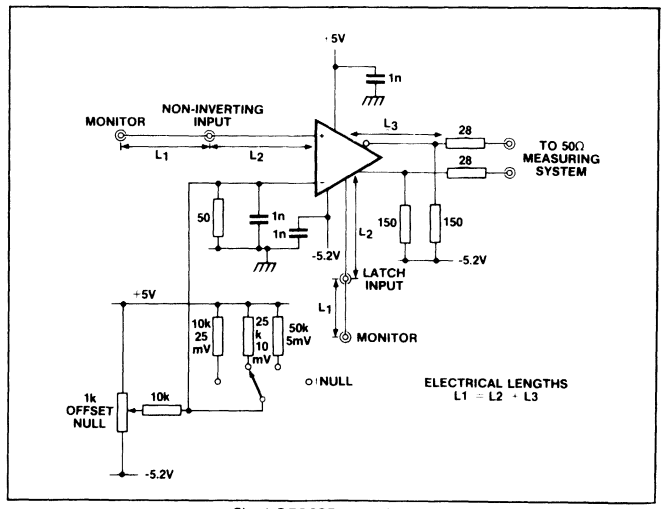


Fig.4 SP9685 test circuit

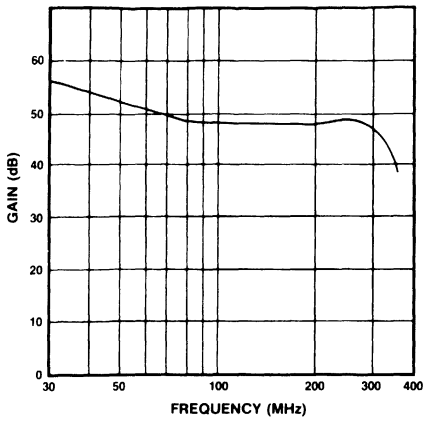


Fig.5 Open loop gain as a function of frequency

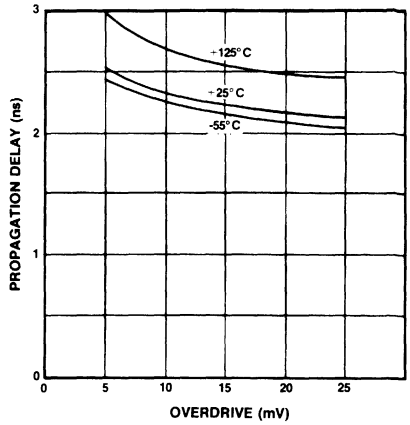


Fig.6 Propagation delay, latch to output as a function of overdrive

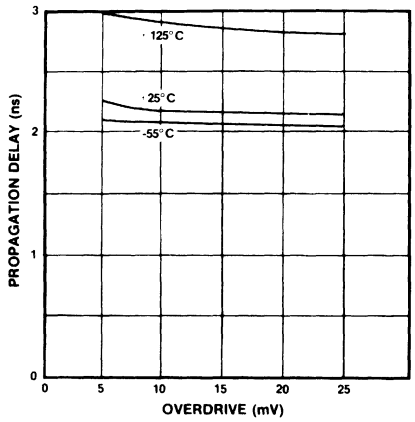


Fig.7 Propagation delay, input to output as a function of overdrive

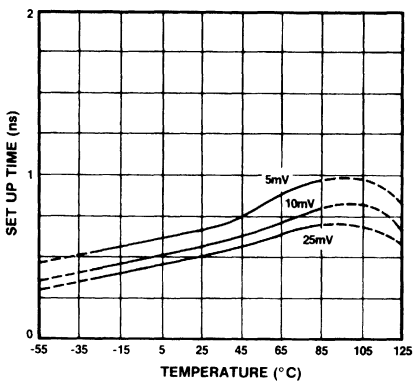


Fig.8 Set-up time as a function of temperature

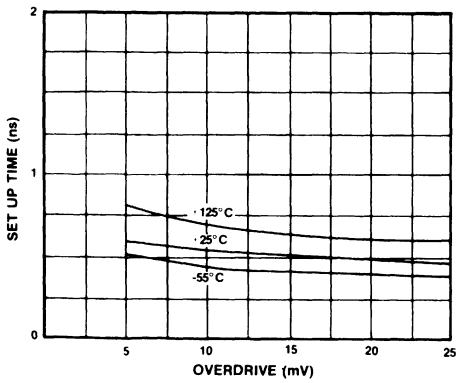


Fig.9 Set-up time as a function of input overdrive

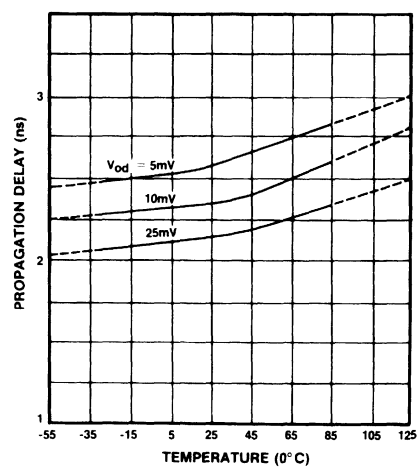


Fig.10 Propagation delay, input to output as a function of temperature

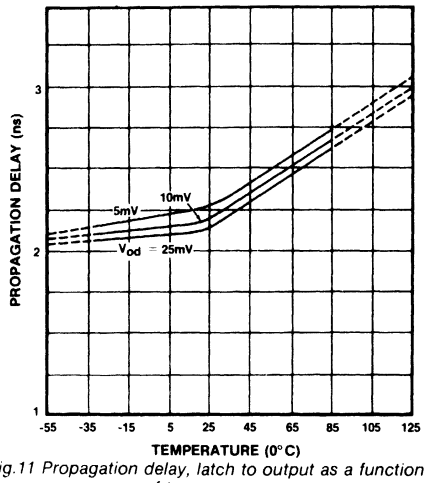


Fig.11 Propagation delay, latch to output as a function of temperature

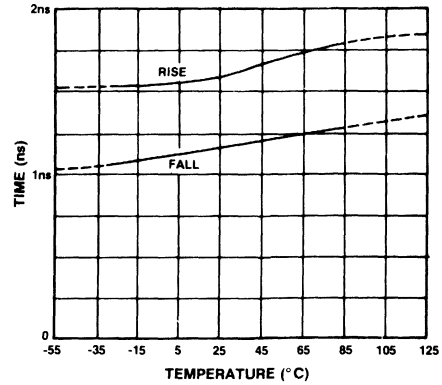


Fig.12 Output rise and fall times as a function of temperature

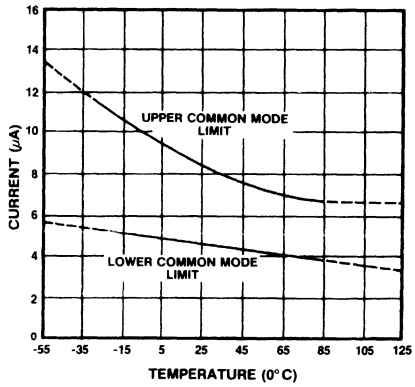


Fig.13 Input bias currents as a function of temperature

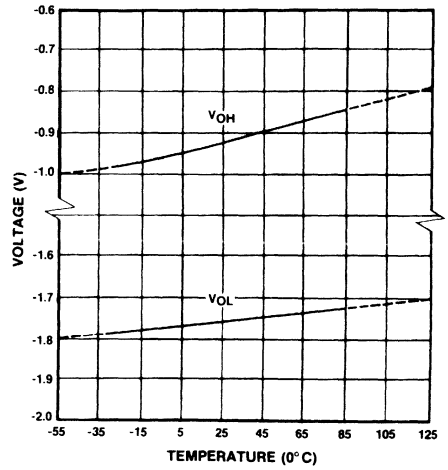


Fig.14 Output levels as a function of temperature

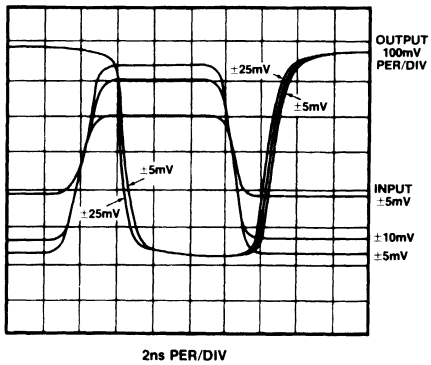


Fig.15 Response to various input signal levels

SP9687

ULTRA FAST COMPARATOR

The SP9687 is an ultra-fast dual comparator manufactured with a high performance bipolar process which makes possible very short propagation delays (2.2ns typ.). The circuit has differential inputs and complementary outputs fully compatible with ECL logic levels. The output current capability is adequate for driving 50Ω terminated transmission lines. The high resolution available makes the device ideally suited to analog-to-digital signal processing applications.

A latch function is provided to allow the comparator to be operated in the follow-hold or sample-hold mode. The latch function inputs are intended to be driven from the complementary outputs of a standard ECL gate. If LE is high, and $\overline{LE}$ is low, the comparator latch is transparent. When LE is driven low and $\overline{LE}$ high, the outputs are latched, see Fig.3. If the latch function is not used, LE must be connected to ECL HI (or ground) and LE to ECL LO.

The device is pin compatible with the AM687 and operates from conventional +5V and -5.2V rails.

FEATURES

- Propagation Delay 2.2ns Typ.
- Latch Set-up Time 1ns Max.
- Complementary ECL Outputs
- 50 ohm Line Driving Capability
- Excellent Common Mode Rejection
- Supply Voltages +5V, -5.2V
- Operating Temperature Range:
  SP9687 — -30°C to +85°C
  SP9687AC — -55°C to +125°C
- Pin Compatible with AD9687
- Pin Compatible with AM687 — But Faster
- Comparators within each SP9687 are matched as follows:
  Input to Output Delay Matching 200ps (typ)
  Latch to Output Delay Matching 200ps (typ)

ORDERING INFORMATION

SP9687DG (Industrial - Ceramic DIL package)
SP9687BB DG (Plessey High Reliability Ceramic DIL package)
SP9687MP (Industrial - Miniature Plastic package)
SP9687AC DG (Military - Ceramic DIL package)

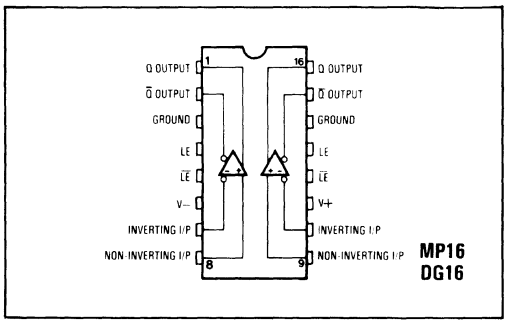


Fig.1 Pin connections

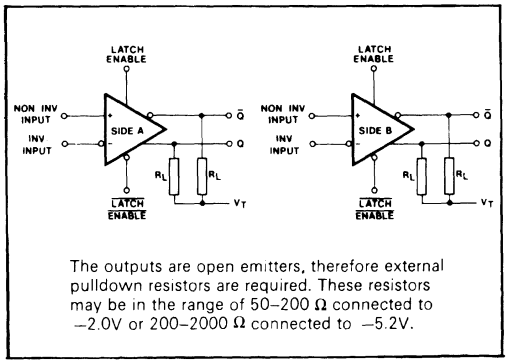


Fig.2 Functional diagram

NOTE:
The AC version of this product conforms to MIL-STD-883C CLASS B screening and is covered by separate data which observes the change notification requirements of MIL-M-38510 and is published in the 'MIL-STD-883C CLASS B Integrated Circuit' Handbook. Please consult your nearest Plessey sales office.

OPERATING NOTES

Timing diagram

The timing diagram, Fig. 3, shows in graphic form a sequence of events in the SP9687. It should not be interpreted as 'typical' in that several parameters are multi-valued and the worst case conditions are illustrated. The top line shows two latch enable pulses, high for 'compare', and low for latch. The first pulse is used to highlight the 'compare' function, where part of the input action takes place in the compare mode. The leading edge of the input signal, here illustrated as a large amplitude, small overdrive pulse switches the comparator over after a time t_{pd}. Output Q and $\overline{Q}$ transitions are essentially similar in timing. The input signal must occur at a time t_s before the latch falling edge, and must be maintained for a time t_h after the latch falling edge, in order to be acquired. After t_h, the output ignores the input status until the latch is again strobed. A minimum latch pulse width $t_{pw(E)}$ is required for the strob operation, and the output transitions occur after a time $t_{pd(E)}$. The LE input is omitted for clarity.

ABSOLUTE MAXIMUM RATINGS

Postive supply voltage	6V
Negative supply voltage	-6V
Output current	30mA
Input voltage	±3V
Differential input voltage	3.5V
Differential latch voltage	3.5V
Power dissipation	590mW
Storage temperature range	-65°C to +150°C
Junction operating temperature	<175°C
Lead temperature (soldering 60 sec)	300°C

Thermal characteristics

DG16	θ_{JA}	110°C/W
	θ_{JC}	33°C/W
LC20	θ_{JA}	73°C/W
	θ_{JC}	22°C/W

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = -30°C to +85°C: V_{CC} = 5.0V ± 0.25V: V_{EE} = -5.2V ± 0.25V:
R_L = 50Ω: V_T = -2.0V (see Fig.2)

Characteristic	Value		Units	Conditions
	Min.	Max.		
Input offset voltage	-5	+5	mV	R_S < 100Ω 25°C
	-7	+7	mV	R_S < 100Ω
Input bias current		20	μA	25°C
		30	μA	
Input offset current		5	μA	25°C
		8	μA	
Input resistance	60		kΩ	25°C
Input capacitance		3	pF	25°C
Supply current I_{EE}		68	mA	Note 2 25°C
		75	mA	
Supply current I_{CC}		46	mA	Note 2 25°C
		50	mA	
Common mode range	-2.5	+2.5	V	
Output logic levels				
Output high	-0.96	-0.81	V	25°C
	-1.045	-0.875	V	T_{amb} = Min.
	-0.89	-0.70	V	T_{amb} = Max.
Output low	-1.85	-1.65	V	25°C
	-1.89	-1.65	V	T_{amb} = Min.
	-1.83	-1.575	V	T_{amb} = Max.
Min. latch set up time		1	ns	Notes 1, 3, 4 25°C
		2	ns	
Input to output delay		3	ns	Notes 1, 3 (Q and $\overline{Q}$) 25°C
		4	ns	
Latch to output delay		3	ns	Notes 1, 3, 4 (Q and $\overline{Q}$) 25°C
		4.5	ns	
Minimum latch pulse width		3	ns	Note 1 25°C
Minimum hold time		1	ns	Note 1 25°C

NOTES

1 Guaranteed but not tested.
2 Refers to entire package. Other data in this table applies to each half.
3 ±100mV pulse with ±10mV overdrive. See Figs 6 to 8.
4 Switching measurements involving the latch are particularly difficult to perform and cannot be tested in production. Circuit analysis shows that at least 95% of devices will meet these specifications.

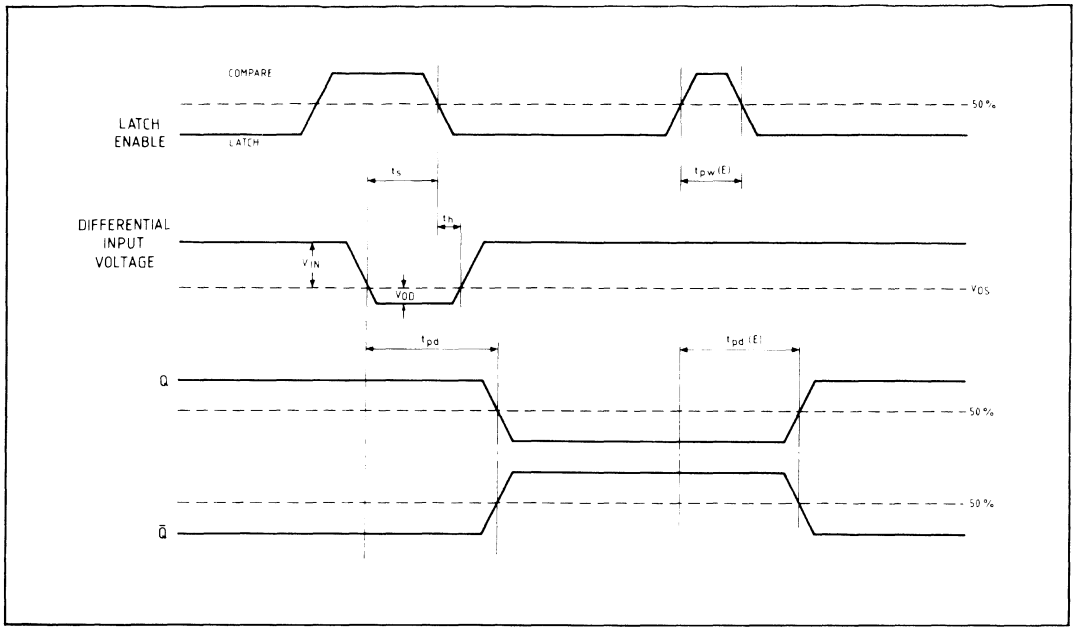


Fig.3 Timing diagram

PERFORMANCE CURVES

Unless otherwise specified, standard conditions for all curves are T_{amb} = 25°C, V_{CC} = 5.0V, V_{EE} = -5.2V

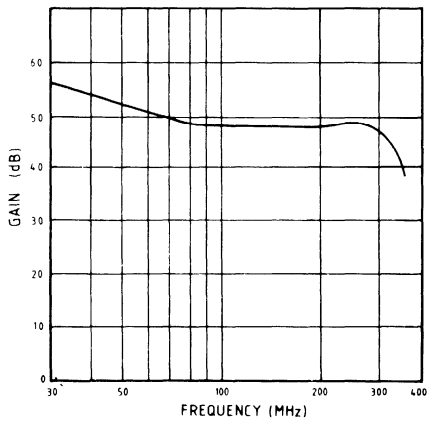


Fig.4 Open loop gain as a function of frequency

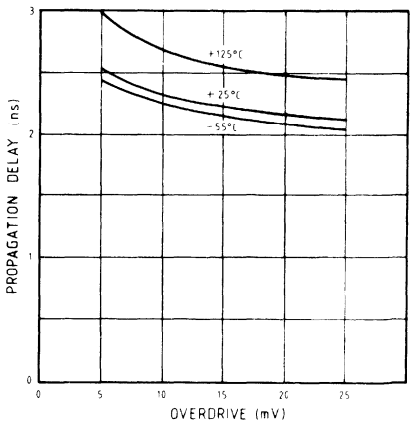


Fig.5 Propagation delay, latch to output as a function of overdrive

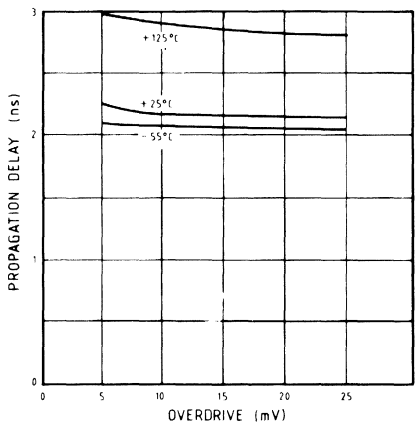


Fig.6 Propagation delay, input to output as a function of overdrive

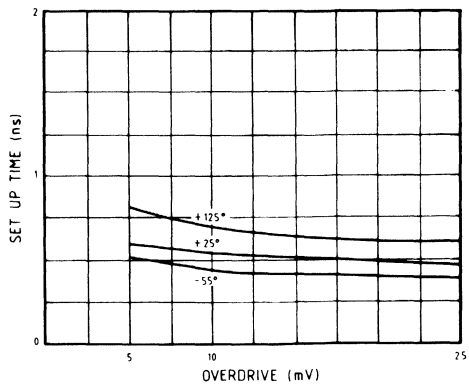


Fig.7 Set-up time as a function of temperature

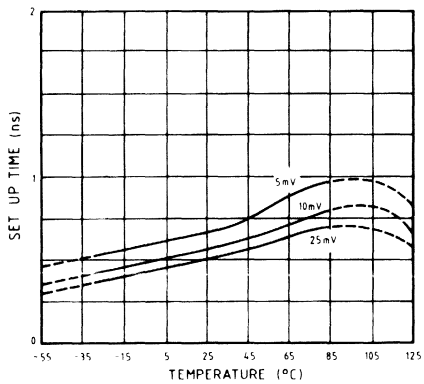


Fig.8 Set-up time as a function of input overdrive

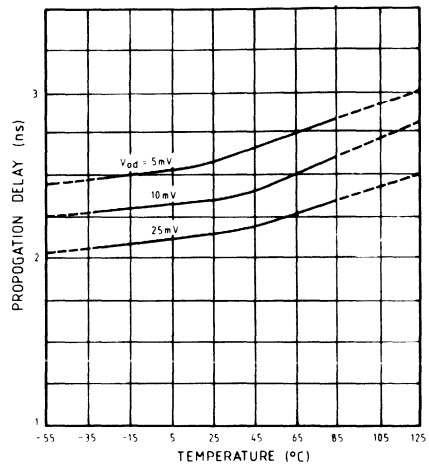


Fig.9 Propagation delay, input to output as a function of temperature

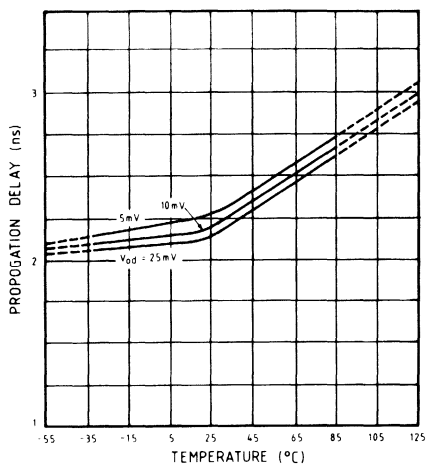


Fig.10 Propagation delay, latch to output as a function of temperature

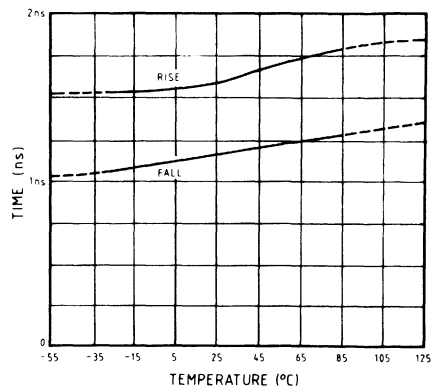


Fig.11 Output rise and fall times as a function of temperature

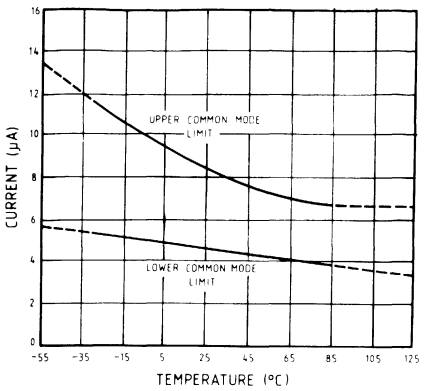


Fig.12 Input bias currents as a function of temperature

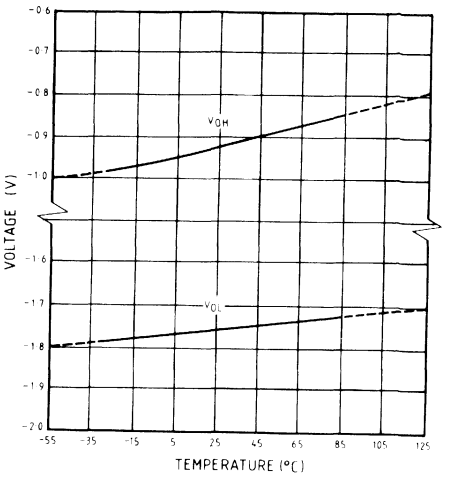


Fig.13 Output levels as a function of temperature

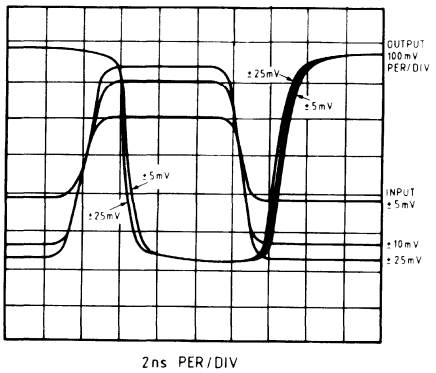


Fig.14 Response to various input signals levels

PLESSEY
Semiconductors

SP9756

6-BIT HIGH SPEED, HIGH ACCURACY ADC

The Plessey SP9756 is a 6-bit flash ECL analog-to-digital converter. It incorporates 64 individual comparators, a clock driver circuit, reference chain and a D-type output latch. This flash ADC is capable of sampling in excess of 110MHz, with a wide analog bandwidth and good dynamic performance.

A choice of accuracy is available: the accuracy of the SP9756-8 is typically ±⅛ LSB at 2V input and therefore it is ideally suited for use in systems that incorporate expansion to higher resolutions. Alternatively the SP9756-6 is guaranteed to be accurate to ±½ LSB for inputs between 1V and 2V in cost conscious designs.

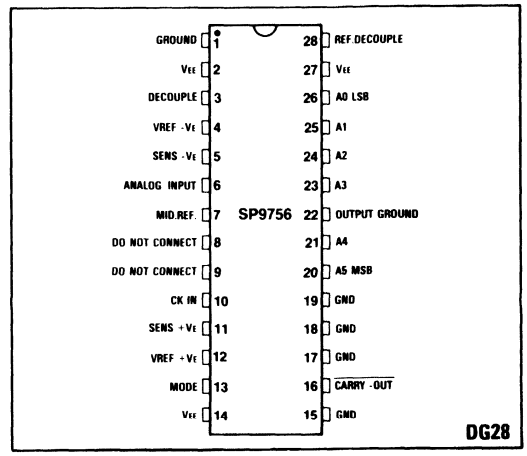


Fig.1 Pin connections - top view

FEATURES

- ±½ or ±⅛ LSB Accuracy (-6 and -8 versions)
- Monotonic over the Full Frequency Range
- 110MHz Conversion Rate (130MHz Typ.)
- 250MHz Full Power Bandwidth (To -3dB) at 1V Input
- 50MHz Bandwidth with typically ±½ LSB Accuracy
- Operates on a Single -5.2V Supply
- Internally Latched 6-Bit ECL Outputs (7ns Minimum Valid Data at 100MHz)
- Operating Temperature Range: -40°C to +85°C Industrial
- On-Chip Band-Gap Reference for Good Temperature Stability
- Internal Clock Buffer
- No External Sample and Hold Needed
- On-Chip Reference Chain
- Sense Outputs for Precise Setting of Reference Voltages
- Mode Input to Program Over-Range Condition
- Low Propagation Delay (3ns Typ.)

APPLICATIONS

- Instrumentation
- Nucleonics Research
- Video Printers
- Radar Video Digitising
- Medical Electronics

ORDERING INFORMATION

SP9756-6 DG (Industrial - Ceramic DIL package)
SP9756-8 DG (Industrial - Ceramic DIL package)

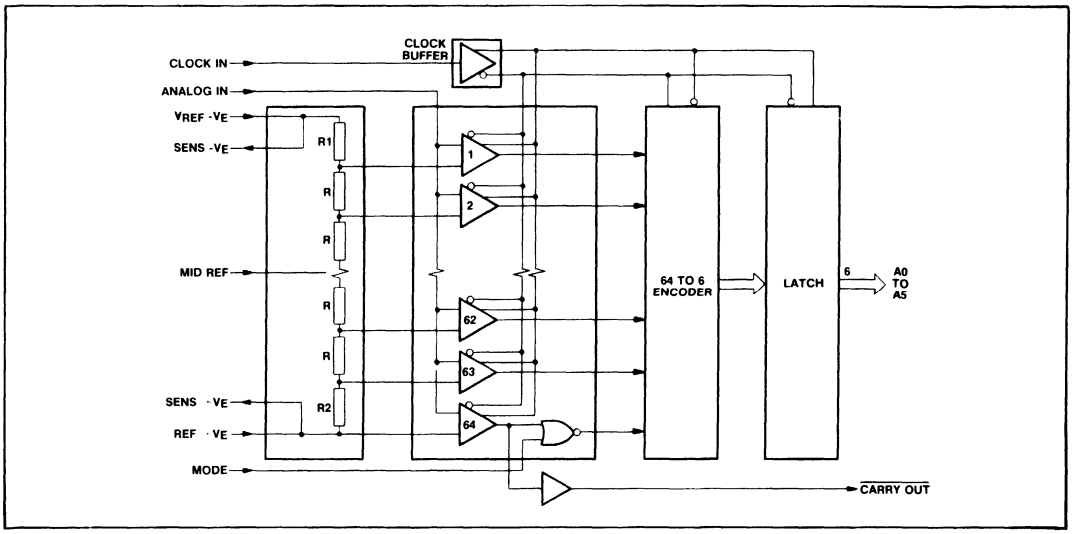


Fig.2 SP9756 functional block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{EE} = -5.2V ± 0.25V

Characteristic	Pin	Value			Unit	Conditions
		Min.	Typ.	Max.		
Supply current, I_{EE}			-170	-250	mA	Excludes ECL O/P & ref. currents
Supply voltage, V_{EE}	2	-4.5		-5.5	V	
Dynamic range				2.20	V	Degrades below -30°C (V_{EE} = -5.20V)
Analog input capacitance			22		pF	
Analog input current				2.2	mA	
Minimum reference bit size			8		mV	
Power dissipation			1.2	1.7	W	Outputs loaded
Differential linearity SP9756-8						
at 7kHz input			±0.125	±0.188	LSB	2V p-p input, 100MHz clock, measured using histogram test. See Figs.7 to 9 and reference 1 measurement techniques.
at 50MHz input			±0.5		LSB	
Integral linearity SP9756-8						
at 7kHz input				±0.25	LSB	
at 50MHz input			±0.5		LSB	
Differential linearity SP9756-6						
at 7kHz input				±0.5	LSB	1V p-p input, 100MHz clock, measured using histogram test. See Figs.10 and 11 and reference 1 measurement techniques.
at 50MHz input				±0.75	LSB	
Integral linearity SP9756-6						
at 7kHz input				±0.5	LSB	
at 50MHz input				±0.5	LSB	
Aperture jitter			25		ps	
Full power 3dB bandwidth			250		MHz	
S/N rato (RMS) at 50MHz analog, 101MHz sample rate		32			dB	
Data out A_0 to A_5	20-21, 2326					
O/P V_{HIGH}			-0.9		V	
O/P V_{LOW}			-1.8		V	
R_{Chain}	3,12		25		Ω	
V_{mode} High	13	-50		+100	mV	All zero's over-range
V_{mode} Low	13	-3.5		-0.500	V	All one's over-range
Sample rate	10	110	130		MHz	No missing codes
T_{data}		7			ns	
T_{prop}			3		ns	
t_1				1.5	ns	
t_{sto}			1.2		ns	
t_{co}			2.0		ns	

ABSOLUTE MAXIMUM RATINGS

Clock & Mode input	0V to -3.5V
Supply voltage	-7V
Maximum junction temperature	175°C
Storage temperature range	-55°C to +150°C
Thermal characteristics:-	
θ_{JA}	40 deg C/W (typ)
θ_{JC}	15 deg C/W (typ)
T_{amb}	-40°C to +70°C (still air)
T_{amb}	-55°C to +125°C (in 500LFPM of air across package)

OPERATING NOTES

Analog Input

The input voltage range is 0.0V to -2.2V. Optimum performance is achieved with an input of 2V p-p i.e. DC offset to -1.0V for symmetrical limiting. At temperatures below -30°C this input range may degrade to 1.8V p-p.

The input capacitance is of the order of 22pF therefore the source impedance should be low. The device is specified using an input drive from a 50Ω generator into a 50Ω termination resistor, i.e. 25Ω looking out of the device. This 25Ω source impedance should be considered as a maximum.

Reference Voltage

For optimum performance REF +VE (pin 12) should be connected to 0V (analog GND) and REF -VE (pin 4) to -2V supply. This supply should be decoupled with a good quality, high frequency capacitor to the analog GND. The minimum voltage across the reference is 0.5V, below this the linearity of the device will be adversely affected.

An input signal above V_{REF} +VE will give an 'all ones' output provided that pin 13 is connected to a -2V supply (see mode input).

Sense pins (SENS +VE, pin 11 and SENS -VE, pin 5) are available on both REF +VE and REF -VE. These allow Kelvin applied voltages to be used for precision setting of the reference chain.

The reference chain can be used dynamically for applications using ACG on non-linear coding (see Fig.6).

Clock Input

As the SP9756 features an internal differential clock driver, a single ended ECL clock signal is suitable.

The aperature uncertainty of the device is in the order of 25ps, therefore the clock signal should have low edge jitter to be compatible.

Clock Timing

The first sample of the analog input is taken approximately 1.2ns after the rising edge of the clock. The input comparators then latch, holding their state until the falling edge.

When the SP9756 receives the first falling edge the device commences decoding and the input comparators are released. The binary data becomes available at the outputs 3.5ns after the second rising edge of the clock.

The SP9756 incorporates an output D-type latch. The data out from this latch is valid for over 70% of the clock cycle, at 100MHz. This greatly simplifies data acquisition of the binary information, as timing is not so critical as with many other ADCs.

Mode Input

The MODE input (pin 13) selects the output code when V_{IN} is higher than REF +VE. For normal operation this pin should be connected to -2V. The SP9756 will then give an all ones output for any input greater than REF +VE. If the mode input is tied to GND the device will give all zeros when the input is higher than REF +VE.

The mode pin must not be left open circuit.

CIRCUIT BOARD LAYOUT

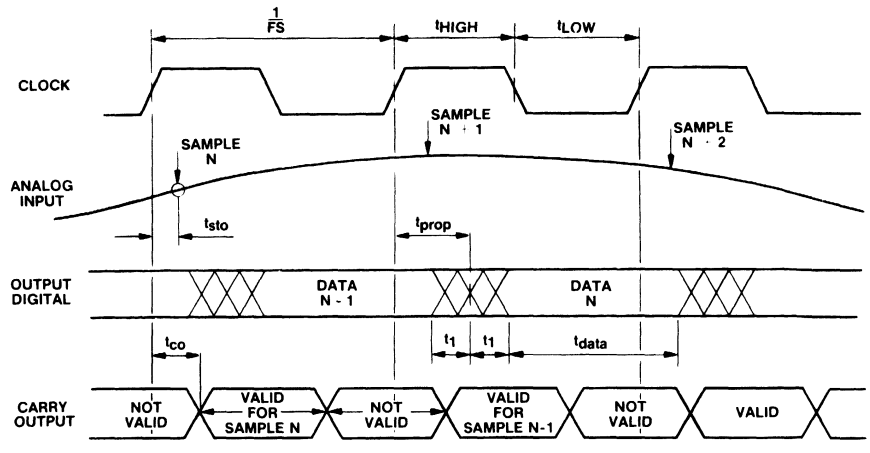
As with most PCB layouts for analog-to-digital conversion, the best performance from the SP9756 can be achieved by separating the ground plane into two sections, analog GND, and digital GND. This aids the device performance by reducing the amount of digital switching noise fed back into the analog section of the converter.

The digital noise is produced mainly by the ECL binary outputs, which ideally should be terminated through a 100Ω load to a -2V supply.

The device supplies are also a source of digital feedback, as they can be modulated by the digital output current. Therefore it is wise to decouple the SP9756 close to the device supply pins with good quality high frequency capacitors. It is also advisable to direct the current returned from the output load towards pin 22 and away from other digital grounds. One way of achieving this is by creating a second digital ground plane which should connect to the main digital ground at pin 22 of the device, the ground connection between the ADC and the device acquiring the data is then made to this second digital ground plane.

The following should be referred to the digital GND: V_{EE}, REF decouple (pin 28), -2V supply for output termination, clock termination, device GND, pins 1, 15 and 22.

The following should be referred to the analog GND: Ref +VE, REF -VE, input termination or buffer.



NOTES
1. Data is valid over complete clock cycle and appears at the O/P after one clock cycle delay.
2. The carry output is valid one clock cycle before the relevant data output.

Fig.3 Timing diagram

SUBRANGING

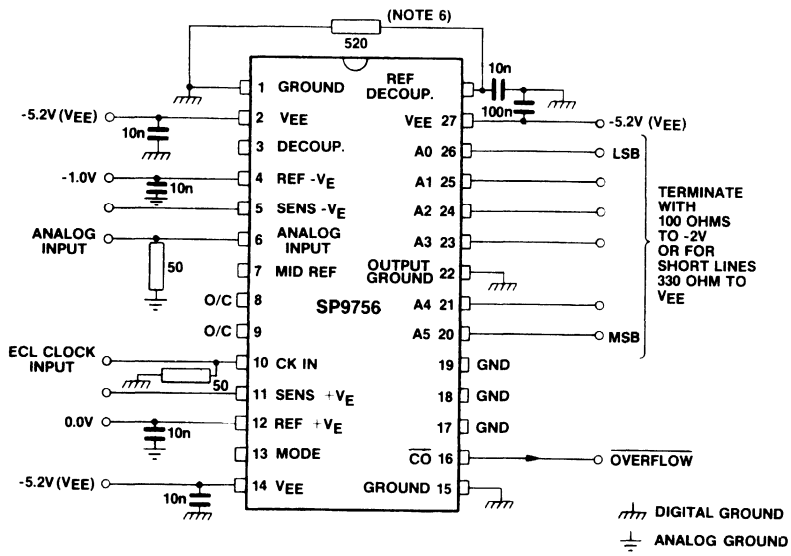
The subranging system uses a two rank method for coarse then fine digitisation of the input signal. The SP9756-8 is ideally suited for subranging systems as the accuracy of the first rank conversion defines the total system accuracy. Systems with 8 bits $\pm\frac{1}{2}$ LSB accuracy can be realised (see Fig.5).

NON LINEAR CODING (REF.3)

By simply feeding the reference with a proportion of the analog input (as shown in Fig.6) non-linear coding can be produced. The accuracy of the Plessey SP9756-8 allows expansion factors of 4:1 whilst maintaining $\frac{1}{2}$ LSB accuracy. This gives a dynamic range of 49.8 dB from a single six-bit device.

REFERENCES

1. *Dynamic Performance of A to D Converters, Hewlett Packard Product Note 5180A-2*
2. *A Complete 100MHz A/D - D/A Evaluation System, Plessey P.S.2048.*
3. *Cern-EP/79-133, B. Hallgren & H. Verweij.*



NOTES ON APPLICATIONS

1. MODE drives output either 'all zeros' or 'all ones' on over-range.
2. Kelvin connections can be made to the referenced chain via SENS (· VE) and SENS (-VE).
3. O/C leave open circuit.
4. REF DECOUPLE (Pin 28) gives access to DC bias reference for logic. This gives ability to eliminate possible crosstalk by allowing capacitor to remove edge noise.
5. Keep OUTPUT GROUND separate from GROUND.
6. Optional 520Ω from pin 1 to pin 28 reduces the number of bit errors, for sensitive applications.

Fig.4 Test and applications circuit

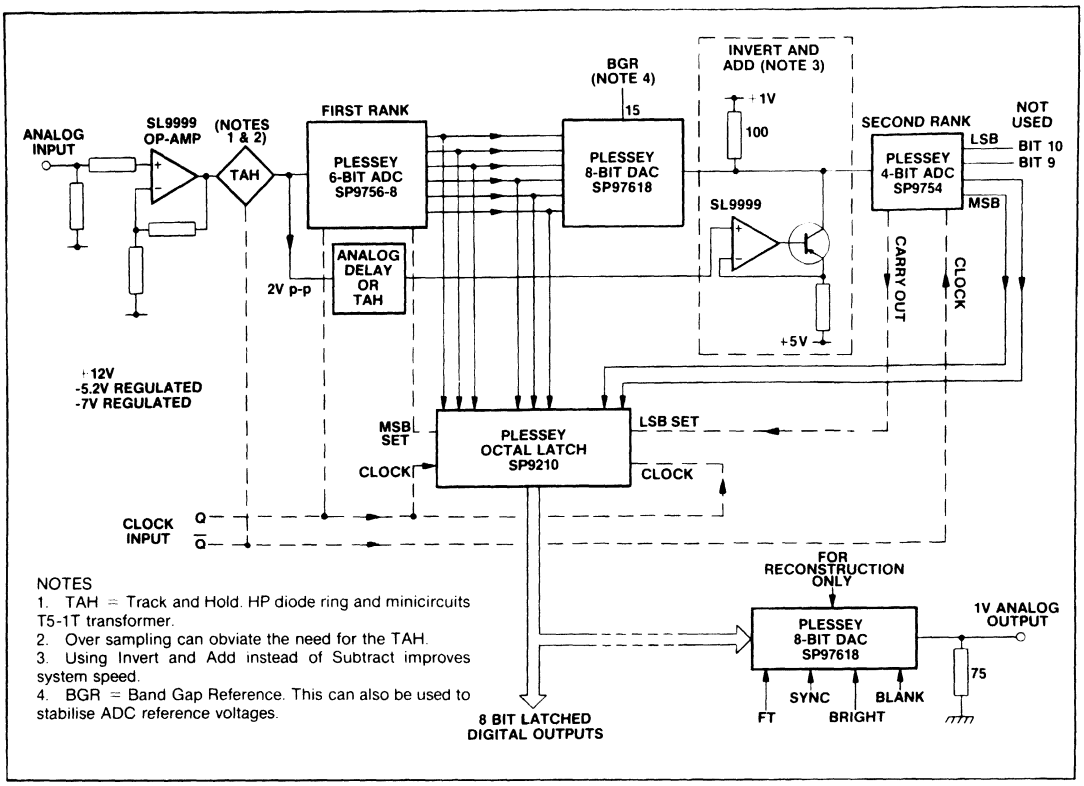


Fig.5 Block diagram of low cost high speed 8-bit A-D converter using SP9756-8

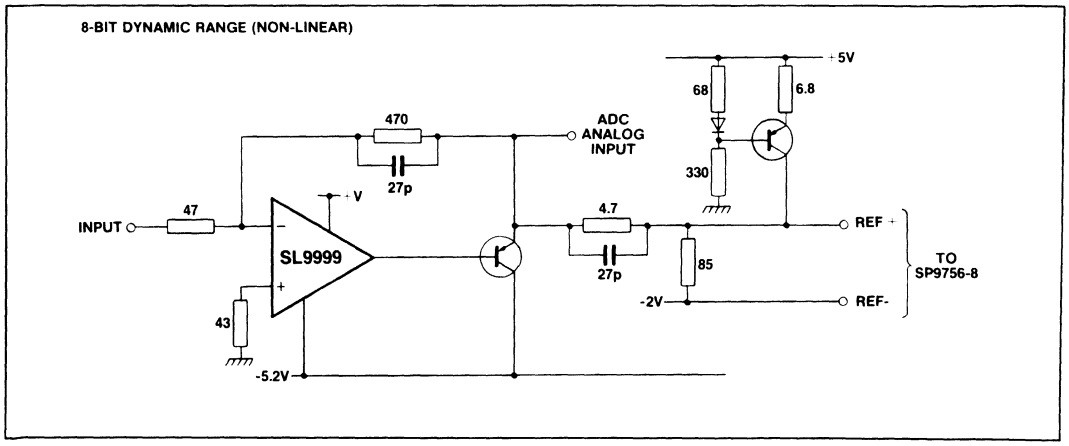


Fig.6 SP9756-8 with 4:1 expansion in dynamic range (non-linear)

TYPICAL ACCURACY DATA

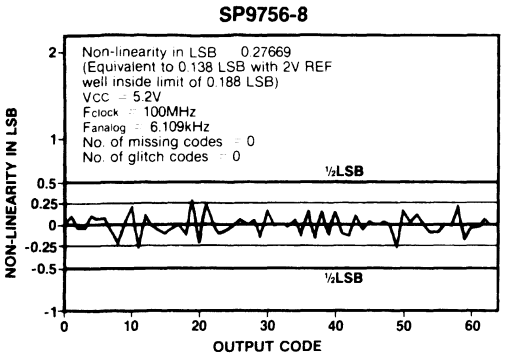


Fig.7 Device measured at 1V on REF with 6kHz analog and 100MHz clock

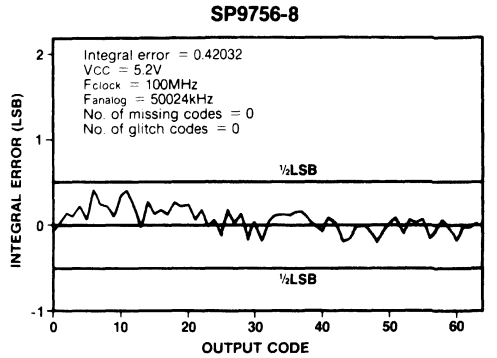


Fig.8 Measured with 2V REF at 50MHz analog and 100MHz clock proves ±0.5 LSB integral spec and ±0.5 LSB differential spec

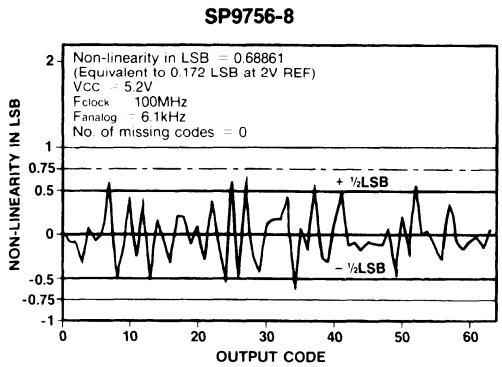


Fig.9 Measured at 0.5V REF
0.75 LSB limit at 0.5V REF ≡ 0.1875 LSB at 2V REF
0.5 LSB limit at 0.5V REF ≡ 0.125 LSB at 2V REF

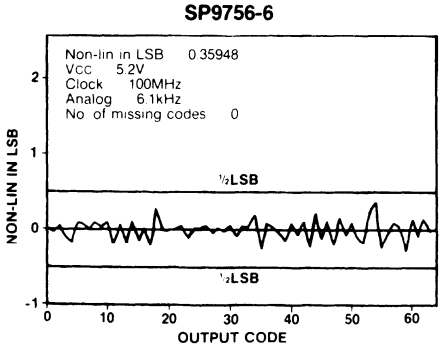


Fig.10 Differential linearity in LSB

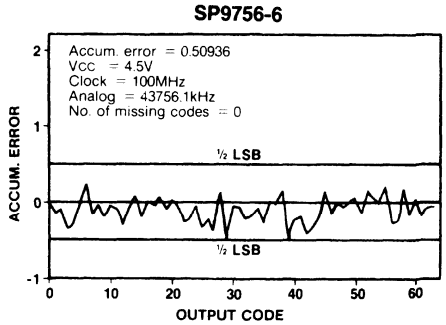


Fig.11 End point integral linearity (near Nyquist input frequency)

PLESSEY
Semiconductors

SP9768

8-BIT HIGH SPEED MULTIPLYING D-A CONVERTER

The SP9768 is an ECL 10K compatible 8-bit DAC. The 5nsec settling time allows a 150 megasample per second conversion time. An inherently low glitch design is used and the complementary current outputs are suitable for direct transmission line drive. The SP9768 design includes a high performance voltage reference and reference amplifier.

Both current and voltage multiplying modes are available.

FEATURES

- 5ns Settling Time 1 LSB Typically
- 8 Bits ±½ LSB Integral and Differential Linearity
- Current Output
- Operating Temperature Range -30°C to +85°C
- ECL 10K Standard Inputs
- Complementary Outputs, 20mA Full Scale
- Reference Temperature Coefficient Typically 40ppm/°C

ORDERING INFORMATION

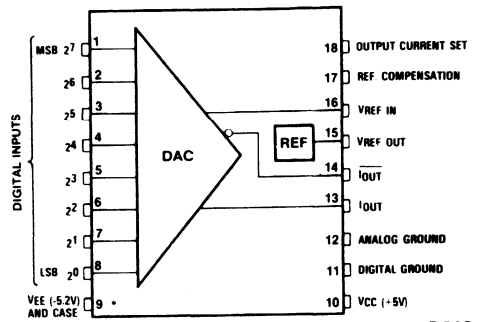
SP9768DP (Industrial - Plastic DIL package)
SP9768DC (Industrial - Sidebrazed DILMON package)
SP9768BB DC (Plessey High Reliability Ceramic DIL package)
SP9768LC (Industrial - LCC package)

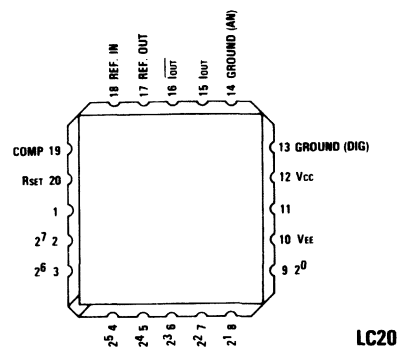
APPLICATIONS

- Data Conversion
- Video Graphic Displays
- Instrumentation
- Waveform Generators
- High Speed Modems
- ADC Evaluation

ABSOLUTE MAXIMUM RATINGS

Positive supply voltage	+5.5V
Negative supply voltage	-5.7V
Digital input voltage	0 to -4.5V
Minimum RSET (from 0V)	175Ω
Maximum RSET	2.5kΩ
Output reference supply (V_L)	0 to +3V
Reference input	±2V
Storage temperature range	-65°C to +150°C
Operating junction temperature	<175°C
Lead temperature (soldering 60 sec)	300°C





Not to scale

Fig.1 Pin connections - top view

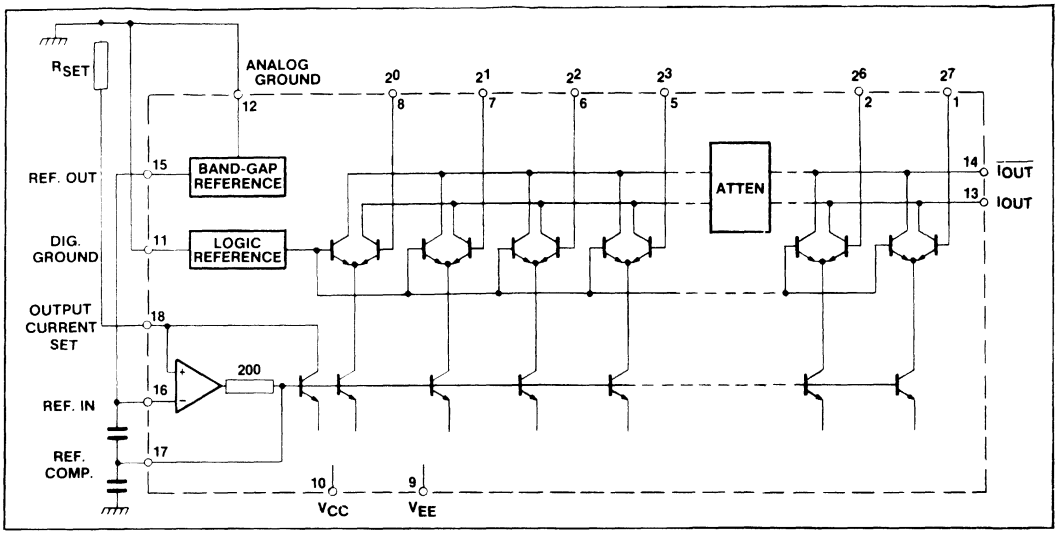


Fig.2 SP9768 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25°C; V_{CC} = +5.00V ± 5%; V_{EE} = -5.2V ± 5%; R_{SET} = 240Ω; Input voltage: High = -0.81V, Low = -1.85V

Characteristic	Value			Unit	Conditions
	Min.	Typ.	Max.		
Supply current I_{CC}	7.0	12.0	20.0	mA	All inputs at
Supply current I_{EE}	55.0	66.0	80.0	mA	-1.8V
Logic inputs:					
V_{IH}	-0.96		-0.81	V	Standard ECL
V_{IL}	-1.85		-1.65	V	10K compatible
$I_{IN(HI)}$		115	200	µA	All inputs HI
Reference voltage V_{REF}	-1.20	-1.26	-1.300	V	Nominal supplies
Reference voltage temp. coeff.		40	80	ppm/°C	-30°C to +85°C
Output current - full scale	2		30	mA	R_{SET} 2.5kΩ - 175Ω
Output current - full scale	20.2	21.3	22.4	mA	R_{SET} = 240Ω
Output compliance	-1.0		+1.0	V	T_{amb} =25°C See
	-0.7		+1.0	V	T_{amb} =85°C Note 4
Bit size (LSB)	78.9	83.2	87.5	µA	Current output
Resolution	8			Bits	
	0.391			%	
Integral non-linearity			0.5	LSB	
Differential non-linearity			0.5	LSB	
Output dynamic parameters (see Note 1)					
Rise time		1.2	2.0	ns	10 to 90%
Settling time - full scale		5	10	ns	To 1 LSB
Glitch energy		90	150	psV	Mid-point
Glitch duration			4	ns	transition
Noise output		-90	-83	dBm	See Note 2
Multiplying mode - voltage (see Fig.5) (See Note 1)					
Multiplying input voltage range	-2		0	V	
Reference input resistance		10		kΩ	
Multiplying input bandwidth		200		kHz	-3dB see Note 3
Transfer function non-linearity		0.2	1.0	%FS	DC

Characteristic	Value			Unit	Conditions
	Min.	Typ.	Max.		
Multiplying mode - current (see Fig.6) (See Note 1)					
Multiplying input current range	0.5		8.0	mA	
Set current input resistance		400		Ohms	
Multiplying input bandwidth		20		MHz	-3dB
Transfer function non-linearity		1.0	3.0	%FS	DC

NOTES
1. Dynamic parameters guaranteed but not 100% tested.
2. Noise in any 10kHz band in the range 0.1 to 500MHz, for any digital input.
3. Voltage-mode multiplying bandwidth is limited by the reference compensation capacitor on the loop amplifier output (pin 17). For the minimum recommended value of 3.9nF, the -3dB point is typically 200kHz. However, the loop amplifier output slew rate is asymmetrical at high frequencies; the maximum frequency at which no significant distortion is introduced is typically 35kHz.
4. The output positive compliance can be increased beyond +1.0V at the expense of linearity. See Fig.4 for circuit configuration.
5. Analog and digital grounds should be connected together at the device pins (pin 11 and pin 12).

THERMAL CHARACTERISTICS

DC18 θ_{JA} = 85°C/W, θ_{JC} = 16°C/W LC20 θ_{JA} = 73°C/W, θ_{JC} = 22°C/W DP18 θ_{JA} = 85°C/W, θ_{JC} = 30°C/W

APPLICATION

The pinout of the device is shown in Fig.1 External components are the current setting resistor and decoupling capacitors.

The DAC has current outputs, with a nominal full-scale of 20mA, corresponding with a 1 volt drop across a 50Ω load.

The actual output current is determined by the on-chip reference voltage and an off-chip current setting resistor. Output current, I_{OUT}, is approximately given by

$$I_{OUT} = 4 \times \frac{V_{REF}}{R_{SET}} \text{ at full scale}$$

A complementary I_{OUT} is also provided. If single output operation only is employed it must be ensured that the complementary output is terminated in an identical manner to the used output. The setting resistor, R_{SET}, is typically 240Ω, giving a full-scale output current of 21mA, and should have a temperature coefficient similar to that of the output load resistor.

The reference voltage source is nominally -1.280 volts and is of a modified bandgap type. Samples show average temperature coefficients of 50ppm/° C over the range -55° C to +125° C. This precision voltage reference can be used as an independent part.

The reference supply is internally compensated; however, to reduce the possibility of instability or noise generation, pin 15 should be decoupled as shown in Fig.4. The current loop technique has been used with a high performance loop amplifier. The current is set by an external resistor as described above. Stabilisation of the loop amplifier is achieved by a single capacitor from pin 17 to ground. Minimum value is 3900pF, although a 10nF chip ceramic is recommended.

Fig.3 shows a suggested circuit for a conventional D to A using the on-chip voltage reference.

RECOMMENDATION

For low output noise it is best to use a chip capacitor on pin 17 to the 0V (GND) plane. The use of split analog and digital ground planes for this device is not recommended. Eurocard construction is not recommended. Ringing or time skew on digital inputs should be avoided.

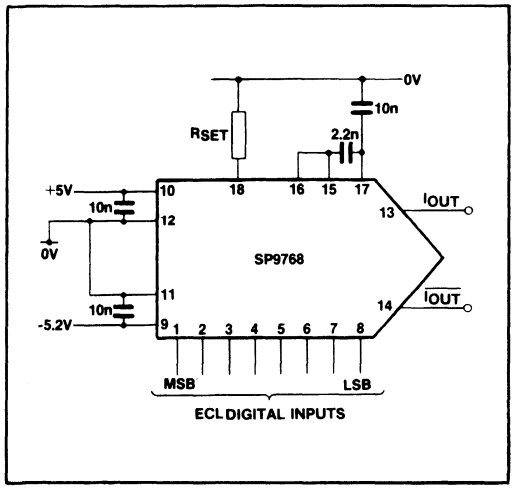


Fig.3 Conventional D/A operation using on-chip reference

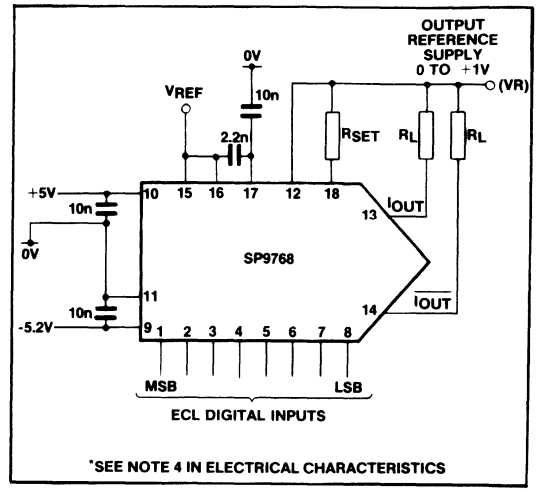


Fig.4 Voltage output referred to a positive voltage

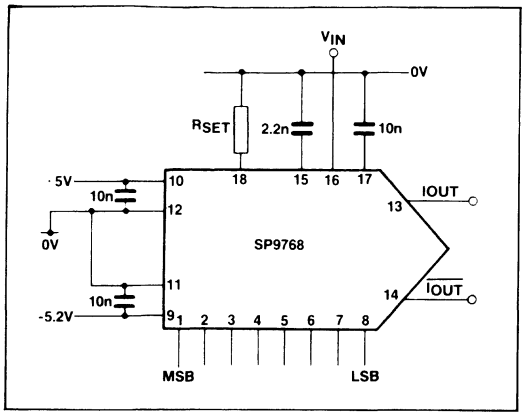


Fig.5 Multiplying mode operation (voltage mode)

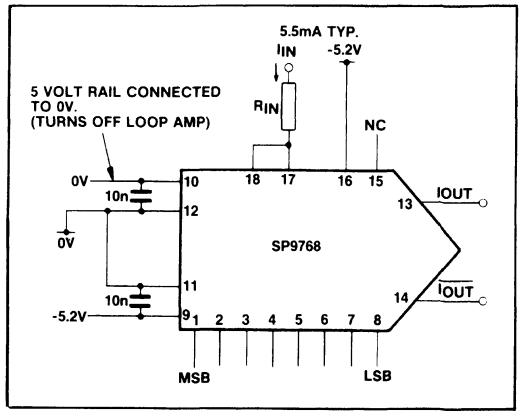


Fig.6 Multiplying mode operation (current mode)

OPERATING NOTES

Output Compliance

Fig.4 shows the method of using the SP9768 with a load resistor not referred to ground, allowing a larger output swing than the conventional connection of Fig.3. Connecting pin 12 and the current setting resistor R_{SET} to the load reference supply ensures that the scale factor of the output is independent of the load reference.

As pointed out in Note 4 of the Electrical Characteristics, extending the compliance beyond +1V may cause sight degradation of linearity.

Multiplying Mode

Multiplying operation of the DAC is available in two modes: either a voltage applied in place of the internal reference, or a current supplied via the current set pin.

Voltage A circuit for using the DAC in voltage multiplying mode is shown in Fig.5. The transfer function is approximately: I_{OUT} (Full Scale) = 4 x V_{IN}/R_{SET}. While this mode offers the best linearity of operation, the frequency response limitations outlined in Note 3 mean that the maximum useable bandwidth is limited to approximately 35kHz.

Current A circuit for using the DAC in current multiplying mode is shown in Fig.6. The transfer function is approximately: I_{OUT} (Full Scale) = 4 x I_{IN}. In this mode the current setting loop amplifier is not used, and any possibility of instability or interference can be averted by turning off the amplifier by connecting V_{CC} to 0V as shown.

The operational bandwidth of the current input to -3dB is at least 20MHz.

A 1V output is obtained into 50 ohm when a current of approximately 5.5mA is fed into pin 17/18 and the input code is selected for full output current.

PLESSEY
Semiconductors

SP9770B & C

10-BIT HIGH SPEED MULTIPLYING D-A CONVERTER

The SP9770 is an ECL 10K compatible 10-bit DAC. The 12nsec settling time allows a 75 megasample per second conversion time. An inherently low glitch design is used and the complementary current outputs are suitable for direct transmission line drive. The SP9770 design includes a high performance voltage reference and reference amplifier.

FEATURES

- Operating Temperature Range -30°C to +85°C
- 12ns Settling Time 1 LSB Typically
- **SP9770B** 10 Bits ±½ LSB Integral and ±½ LSB Differential Linearity
- **SP9770C** 10 Bits ±½ LSB Integral and ±1 LSB Differential Linearity
- Current Output
- ECL 10K Standard Inputs
- Complementary Outputs, 20mA Full Scale
- Reference Temperature Coefficient Typically 40ppm/°C

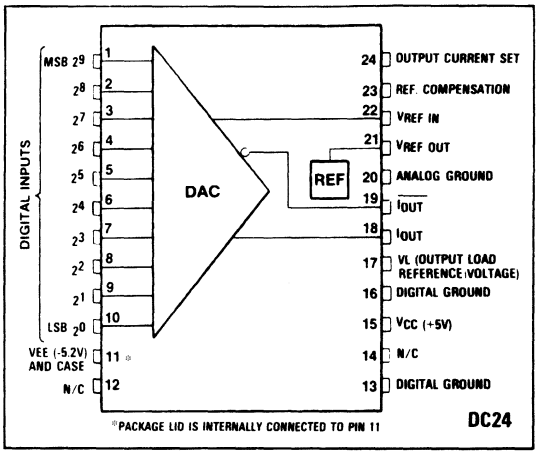


Fig.1 Pin connections - top view

ORDERING INFORMATION

SP9770B DC (Industrial - Sidebrazed DILMON package)
SP9770C DC (Industrial - Sidebrazed DILMON package)

APPLICATIONS

- Data Conversion
- Video Graphic Displays
- Instrumentation
- Waveform Generators
- High Speed Modems

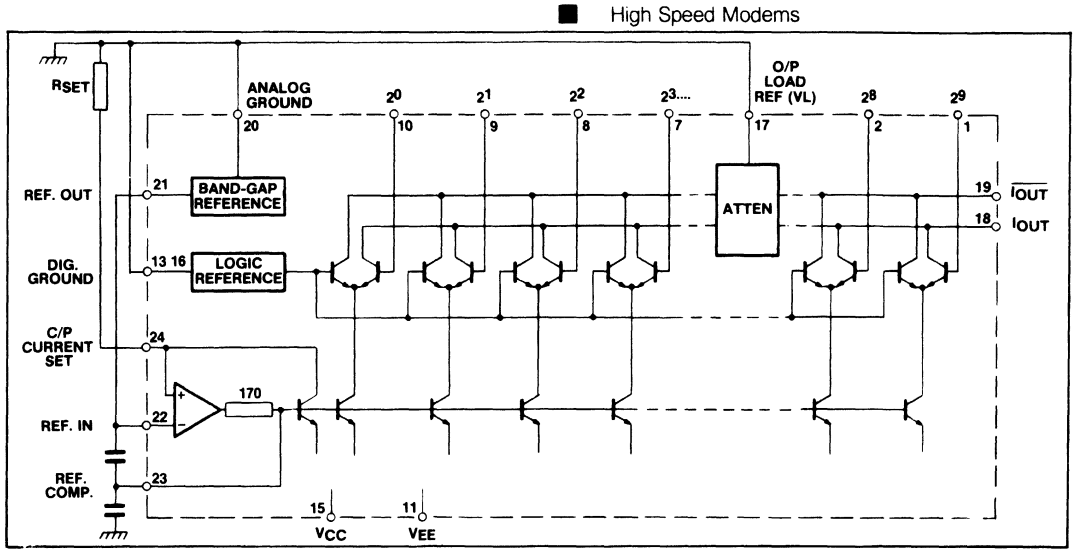


Fig.2 SP9770 block diagram

ABSOLUTE MAXIMUM RATINGS

Positive supply voltage	+5.5V	Output reference supply (V_L)	0 to +3V
Negative supply voltage	-5.7V	Reference input	±2V
Digital input voltage	0 to -4.5V	Storage temperature range	-65°C to +150°C
Minimum R_{SET} (from 0V)	175Ω	Junction operating temperature	<175°C
Maximum R_{SET}	2.5kΩ	Lead temperature (soldering 60 sec)	300°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25°C; V_{CC} = +5.00V ± 5%; V_{EE} = -5.2V ± 5%; R_{SET} = 240Ω; Input voltage: High = -0.81V, Low = -1.85V

Characteristic	Value			Unit	Conditions
	Min.	Typ.	Max.		
Supply current I_{CC}	7.0	12.0	17.0	mA	All inputs at
Supply current I_{EE}	45.0	56.0	70.0	mA	-1.8V
Logic inputs:					
V_{IH}	-0.96		-0.81	V	Standard ECL
V_{IL}	-1.85		-1.65	V	10K compatible
$I_{IN(HI)}$		115	200	μA	All inputs HI
Reference voltage V_{REF}	-1.250	-1.280	-1.300	V	
Reference voltage temp. coeff.		40	80	ppm/°C	-30°C to +85°C
Output current - full scale	2		30	mA	R_{SET} 2.5kΩ - 175Ω
Output current - full scale	20.2	21.3	22.4	mA	R_{SET} = 240Ω
Output compliance	-1.0		+1.0	V	T_{amb} =25°C See
	-0.7		+1.0	V	T_{amb} =85°C Note 4
Bit size (LSB)	19.7	20.8	21.9	μA	Current output
Resolution	10			Bits	
	0.098			%	
Differential non-linearity			0.5	LSB	
Integral non-linearity			0.5	LSB	SP9770B
			1.0	LSB	SP9770C
Output dynamic parameters (see Note 1)					
Rise time		2.0	3.0	ns	10 to 90%
Settling time - full scale		12	20	ns	To 1 LSB
Glitch energy		90	150	psV	Mid-point
Glitch duration			4	ns	transition
Noise output		-90	-83	dBm	See Note 2
Multiplying mode - voltage (see Fig.5)					
Multiplying input voltage range	-2		0	V	
Reference input resistance		10		kΩ	
Multiplying input bandwidth		200		kHz	-3dB see Note 3
Transfer function non-linearity		0.2	1.0	%FS	DC

NOTES
1. Dynamic parameters guaranteed but not 100% tested.
2. Noise in any 10kHz band in the range 0.1 to 500MHz, for any digital input.
3. Voltage-mode multiplying bandwidth is limited by the reference compensation capacitor on the loop amplifier output (pin 23). For the minimum recommended value of 3.9nF, the -3dB point is typically 200kHz. However, the loop amplifier output slew rate is asymmetrical at high frequencies; the maximum frequency at which no significant distortion is introduced is typically 35kHz.
4. The output positive compliance can be increased beyond +1.0V at the expense of linearity. See Fig.4 for circuit configuration.

Thermal characteristics
θ_{JA} = 65°C/W
θ_{JC} = 15°C/W

APPLICATION

The pinout of the device is shown in Fig.1. External components are the current setting resistor and decoupling capacitors.

The DAC has current outputs, with a nominal full-scale of 20mA, corresponding with a 1 volt drop across a 50Ω load.

The actual output current is determined by the on-chip reference voltage and an off-chip current setting resistor. Output current, I_{OUT}, is given by

$$I_{OUT} \triangleq 4 \times \frac{V_{REF}}{R_{SET}} \text{ at full scale}$$

A complementary I_{OUT} is also provided. If single output operation only is employed it must be ensured that the complementary output is terminated in an identical manner to the used output. The setting resistor, R_{SET}, is typically 240Ω, giving a full-scale output current of 21mA, and should have a temperature coefficient similar to that of the output load resistor.

The reference voltage source is nominally -1.280 volts and is of a modified bandgap type. Samples show average temperature coefficients of 50ppm/° C over the range -55° C to +125° C. This precision voltage reference can be used as an independent part.

The reference supply is internally compensated; however, to reduce the possibility of instability or noise generation, pin 21 should be decoupled as shown in Fig.4. The current loop technique has been used with a high performance loop amplifier. The current is set by an external resistor as described above. Stabilisation of the loop amplifier is achieved by a single capacitor from pin 23 to ground. Minimum value is 3900pF, although a 10nF chip ceramic is recommended.

Fig.3 shows a suggested circuit for a conventional D to A using the on-chip voltage reference.

RECOMMENDATIONS

For low output noise it is best to use a chip capacitor on pin 23 to the 0V (GND) plane. The use of split analog and digital ground planes for this device is not recommended.

For low glitch output it is essential that the input time skew and ringing is minimised. The Plessey SP9210 is a suitable high speed latch for this purpose.

Eurocard construction is not recommended.

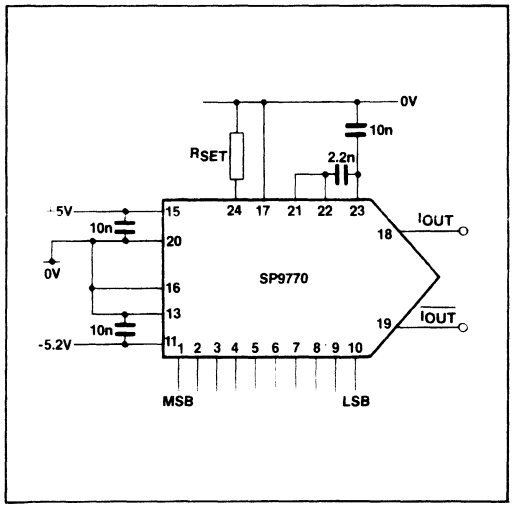


Fig.3 Conventional D/A operation using on-chip reference

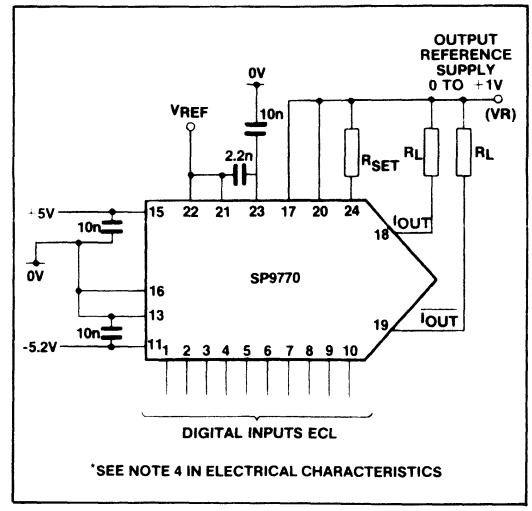


Fig.4 Voltage output referred to a positive voltage for outputs biased above ground

OPERATING NOTES

Output Compliance

Fig.4 shows the method of using the SP9770 with a load resistor not referred to ground, allowing a larger output swing than the conventional connection of Fig.3. Connecting pins 17 and 20, and the current setting resistor R_{SET} to the load reference supply ensures that the scale factor of the output is independent of the load reference.

As pointed out in Note 4 of the Electrical Characteristics, extending the compliance beyond +1V may cause slight degradation of linearity.

Voltage multiplying. A circuit for using the DAC in voltage multiplying mode is shown in Fig.5. The transfer function is approximately: I_{OUT} (Full Scale) = 4 x V_{IN}/R_{SET}. While this mode offers the best linearity of operation, the frequency response limitations outlined in Note 3 mean that the maximum useable bandwidth is limited to approximately 35kHz.

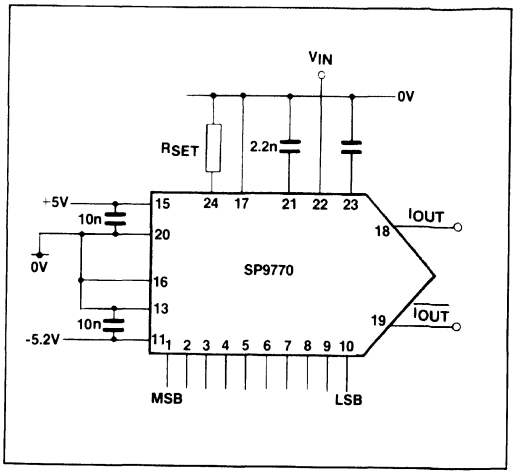


Fig.5 Multiplying mode operation (voltage mode)

PLESSEY
Semiconductors

SP92701

SUB-NANOSECOND ECL LINE RECEIVER AND DRIVER

The SP92701 is designed with an on-chip reference to allow either single ended or differential ECL signals to be received. The inverted and non-inverted outputs can drive 50Ω lines directly.

The use of a fixed current source in the tail of the differential input stage, enables the device to be used in more general applications. These include operational amplifier applications where low propagation delays are required.

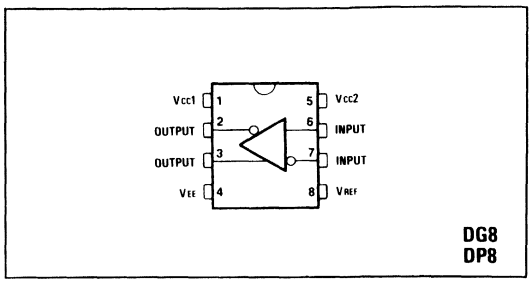


Fig.1 Pin connections - top view

FEATURES

- ECL 10K Compatible
- Single or Differential Operation
- 50 Ohm Line Driving Capability
- Sub-nanosecond Performance
- ECL Reference Output
- Operating Temperature -40°C to +85°C (DG)
- Full Static Protection on All Pins

APPLICATIONS

- Line Receiver
- Line Driver
- Clock Buffering/Distribution
- Op-amp Circuits
- Fanout Expansion
- Schmitt Trigger Circuits
- Fast Peak Detector

ORDERING INFORMATION

SP92701C DP (Industrial - Plastic DIL package)
SP92701B DG (Industrial - Ceramic DIL package)

ABSOLUTE MAXIMUM RATINGS

Power supply voltage | V_{CC}-V_{EE}|	8V
Input voltage	0V to V_{EE}
Differential input voltage	3.3V
Output source current	50mA
Storage temperature range	-55°C to 150°C
Junction operating temperature	
DG	175°C
DP	150°C

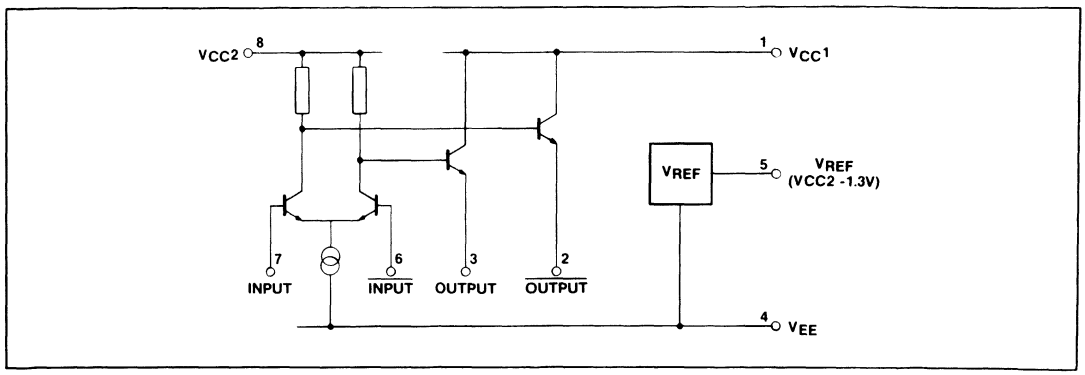


Fig.2 Internal diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} −40 °C to +85 °C (DG package), 0 °C to +70 °C (DP package); V_{EE} = −5.2V ± 0.25V

DC Characteristics

Characteristic	Symbol	Value						Units	Conditions
		−40 °c (DG)		25 °C (DP & DG)		85 °C (DG)			
		Min.	Max.	Min.	Max.	Min.	Max.		
Power supply current	I_{EE}		12		12		12	mA	No load
Input current high	I_{INH}				350			μA	Inputs ECL high
Input leakage current	I_{cbo}		50		40		40	μA	Inputs ECL low
Reference voltage	V_{REF}	−1.43	−1.29	−1.35	−1.23	−1.29	−1.15	V	
High output voltage	V_{OH}	−1.06	−0.86	−0.96	−0.81	−0.89	−0.70	V	Load = 50Ω to −2V
Low output voltage	V_{OL}	−1.90	−1.66	−1.85	−1.62	−1.83	−1.57	V	Load = 50Ω to −2V
High input voltage	V_{IH}	−1.19	−0.88	−1.09	−0.81	−1.03	−0.7	V	
Low input voltage	V_{IL}	−1.90	−1.53	−1.85	−1.48	−1.83	−1.44	V	

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Common mode range	V_{cmr}		2.85 to 0.8		V	At 25 °C
Input sensitivity (differential)	V_{pp}		150		mV	At 25 °C
Differential gain			25		dB	At 25 °C

AC Characteristics

T_{amb} = 25 °C

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Propagation delay	t_{pd}		0.8	0.96	ns	
Transition time, 20 % to 80 %	t_r, t_f		0.8	0.95	ns	

NOTE Guaranteed but not tested.

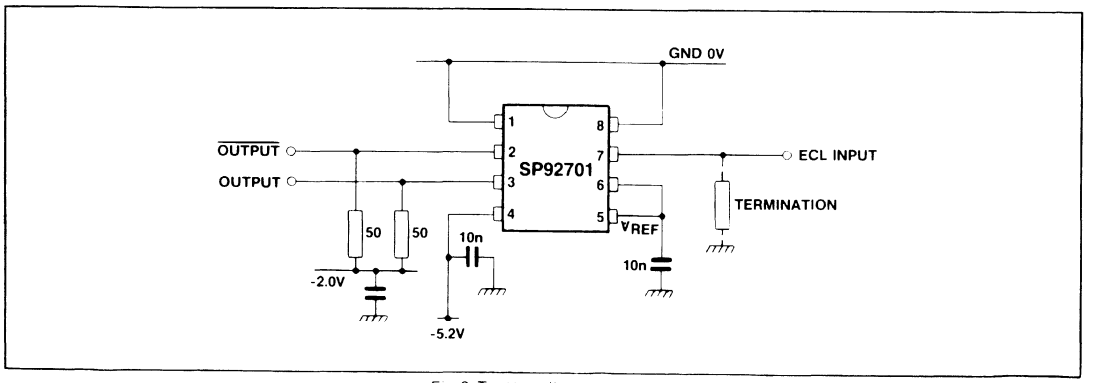


Fig.3 Test/applications circuit

OPERATING NOTES

The SP92701 has been designed primarily for enhancing the edges of ECL signals.

With most systems using ECL it is necessary to minimise the amount of edge jitter on clock signals etc. By reducing the rise times of the ECL edges it is possible to reduce the amount of voltage noise to time jitter conversion that occurs with slower edge.

The SP92701 can also be used to expand fanout and provide conversion from single ended to differential or differential to single ended ECL.

A current source located in the tail of the differential pair (Fig.2) gives the SP92701 a wide common mode range. This enables it to be used in other applications such as comparators or low cost wideband amplifiers.

Used as a line receiver in single ended non-inverting mode, the typical maximum frequency of operation is 700MHz.

Outputs

The outputs of the SP92701 are open emitter and hence require an external pulldown resistor for evaluation or test. It can also be useful to apply $V_{CC} = +2V$ and $V_{EE} = -3.2V$ for direct drive of 50Ω instruments.

Schmitt Trigger

Positive feedback can be applied from the output for applications that require input hysteresis.

Board Layout

Care should be taken with component placement. Use a solid ground plane under the device. Tracks should be short or terminated with their characteristic impedance. The supply pins should be decoupled to ground with good high frequency decoupling capacitors, located close to the device pins.

ANALOG APPLICATION (Fig.4)

SP92701, SL560 combination. Forming a low noise, low cost 30dB amplifier and differential line driver (100Ω twisted pair). Response is flat to 350MHz ± 1dB.

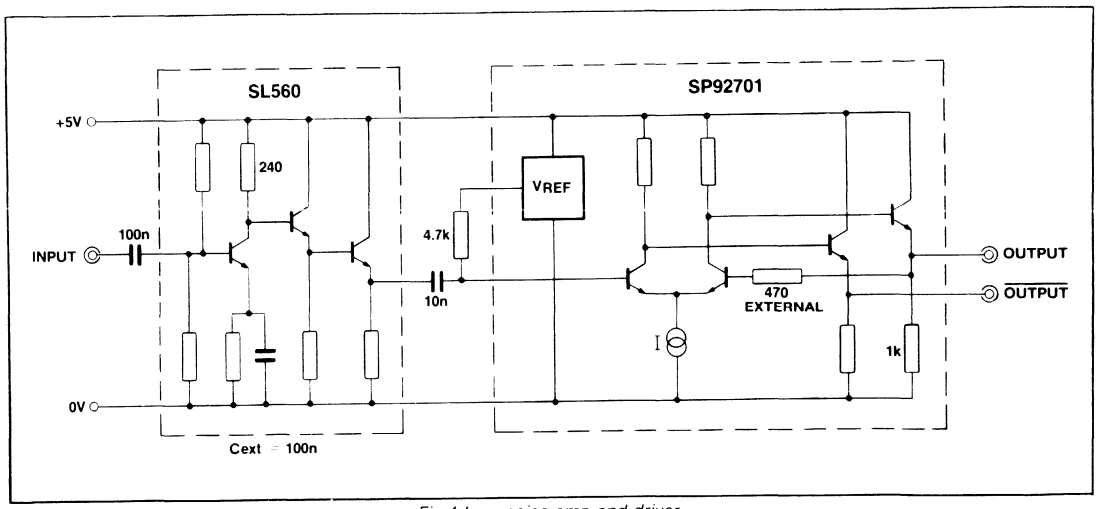


Fig.4 Low noise amp and driver

PLESSEY
Semiconductors

SP93802

SUB-NANOSECOND DUAL COMPARATOR

(SUPERSEDES AUGUST 1987 DATABOOK EDITION)

The Plessey SP93802 contains two independent matched ultra high speed comparators. Each comparator is followed by a latch which may be used to sample the comparator output. The gain of this comparator has been optimised for low propagation delay and high stability, therefore hysteresis is rarely required.

Each comparator includes a glitch capture circuit which enables the detection and latching of a 20mVns output glitch, when the device is in compare mode. As each comparator is separately clocked, the device can be used as a matched pair.

Special attention has been paid to the clock circuit and packaging to minimise crosstalk.

These features are not only beneficial to logic analyser and counter designs, but also in many other high speed data conversion or data communication systems.

FEATURES

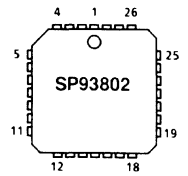
- -40°C to +85°C Temperature Range
- Typical Delay < 1ns
- Glitch Capture, 20mVns (Typ.)
- On Chip Band Gap Reference Circuitry
- 50 Ohm Drive Capability
- On Chip Clock Buffers
- 2 Matched Comparator/Latched Channels
- Channel Propagation Delay Matching < 100ps
- High Input Impedance
- Quad and Octal Versions SP93804/SP93808

APPLICATIONS

- Automatic Test Equipment
- Instrumentation
- Line Receiver/Driver
- Cascadable Differential Amplifier
- Analog to Digital Conversion
- Fibre Optics
- Logic Analysers

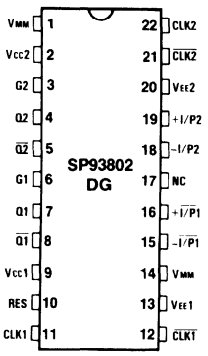
ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC} - V_{MM}	+6V
Supply voltage V_{MM} - V_{EE}	-6V
Operating temperature range	-40°C to +85°C
Storage temperature range	-55°C to +125°C
Output current	≤30mA
Maximum input voltage	
Common mode positive	≤V_{CC}
Common mode negative	≥V_{EE}
Differential input voltage	≤±3.8V



HG28

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	V_{MM}	8	NC	15	CLK1	22	NC
2	V_{CC2}	9	G1	16	$\overline{CLK1}$	23	-I/P2
3	O/P V_{CC2}	10	Q1	17	V_{EE1}	24	+I/P2
4	NC	11	$\overline{Q1}$	18	V_{MM}	25	NC
5	G2	12	O/P V_{CC1}	19	NC	26	V_{EE2}
6	Q2	13	V_{CC1}	20	-I/P1	27	$\overline{CLK2}$
7	$\overline{Q2}$	14	RESET	21	+I/P1	28	CLK2



DG22

Fig.1 Pin connections - top view

ORDERING INFORMATION

SP93802 B HG (Industrial - Quad Cerpac (J-Form) package)
SP93802 B DG (Industrial - Ceramic DIL package)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = -40°C to +85°C, I/P and O/P V_{CC} = +5V ± 0.25V,
V_{EE} = -5V ± 0.25V, V_{MM} = 0V (see Fig.4), Load = 50Ω to Vcc - 2V

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Positive supply current	I_{CC}		38.5	50	mA	V_{CC} = 5V, V_{EE} = -5V No load. Each comparator.
Negative supply current	I_{EE}		16.0	21	mA	V_{CC} = 5V, V_{EE} = -5V No load. Each comparator.
Positive supply voltage	V_{CC}	I/P MAX +1.55	5.0	I/P MIN +7.3	V	
Negative supply voltage	V_{EE}	-5.5	-5.0	-4.9	V	
Input offset voltage	V_{OS}	-3.5		+3.5	mV	
Input bias current	I_B		5.25	9	μA	
Input offset current	I_{OS}		0.95	1.2	μA	
Input capacitance	C_I		1.5 (Note 1)		pF	HG package
Input impedance	R_I		250		kΩ	Measured at DC
Differential input range	V_{DIF}			±3.8	V	
Common mode input range	CMIR	-2.1		+2.6	V	
Output voltage high	V_{OH}	Vcc-1.050		Vcc-0.81	V	+25°C, V_{IN} > 60mV
		Vcc-1.140		Vcc-0.91	V	-40°C, V_{IN} > 60mV
		Vcc-0.965		Vcc-0.704	V	+85°C, V_{IN} > 60mV
Output voltage low	V_{OL}	Vcc-1.712		Vcc-1.544	V	+25°C, V_{IN} < -60mV
		Vcc-1.792		Vcc-1.650	V	-40°C, V_{IN} < -60mV
		Vcc-1.638		Vcc-1.465	V	+85°C, V_{IN} < -60mV
Gain (transparent mode)			20		dB	Differential
Common mode rejection	CMRR		50		dB	+25°C, with respect to I/P
Supply voltage rejection	PSRR		70		dB	+25°C, with respect to I/P offset
Clock input:						
Common mode range	CMRC	V_{MM} + 2V		Vcc-1.35V	V	
Differential swing	DS	400		1600	mV	

NOTES 1 Guaranteed but not tested

Dynamic Characteristics (Note 1) See dynamic test circuit Fig.9.

Characteristic	Symbol	Value			Units	Condition
		Min.	Typ.	Max.		
Latch setup time	t_S		150		ps	20mV overdrive
Hold time	t_h		600		ps	20mV overdrive
Input to Q delay	t_{iQ}		800		ps	20mV overdrive
Latch to Q delay	t_{LQ}		1500		ps	20mV overdrive
Glitch capture regeneration	t_{RD}		900		ps	20mV overdrive at Qn
Propagation delay matching	t_{PDM}	-100		+100	ps	Within each device
Min. compare pulse width	t_{PW}		950		ps	20mV overdrive
Min. reset pulse width	t_{RM}		800		ps	
Max. flip flop reset time	t_{RR}		800		ps	
Min. hold time of Qn after reset	t_{GH}		800		ps	
Delay between Qn and Gn	t_{QG}		900		ps	
Propagation delay RES to Gn	t_{RG}		800		ps	

NOTES 1 Guaranteed but not tested

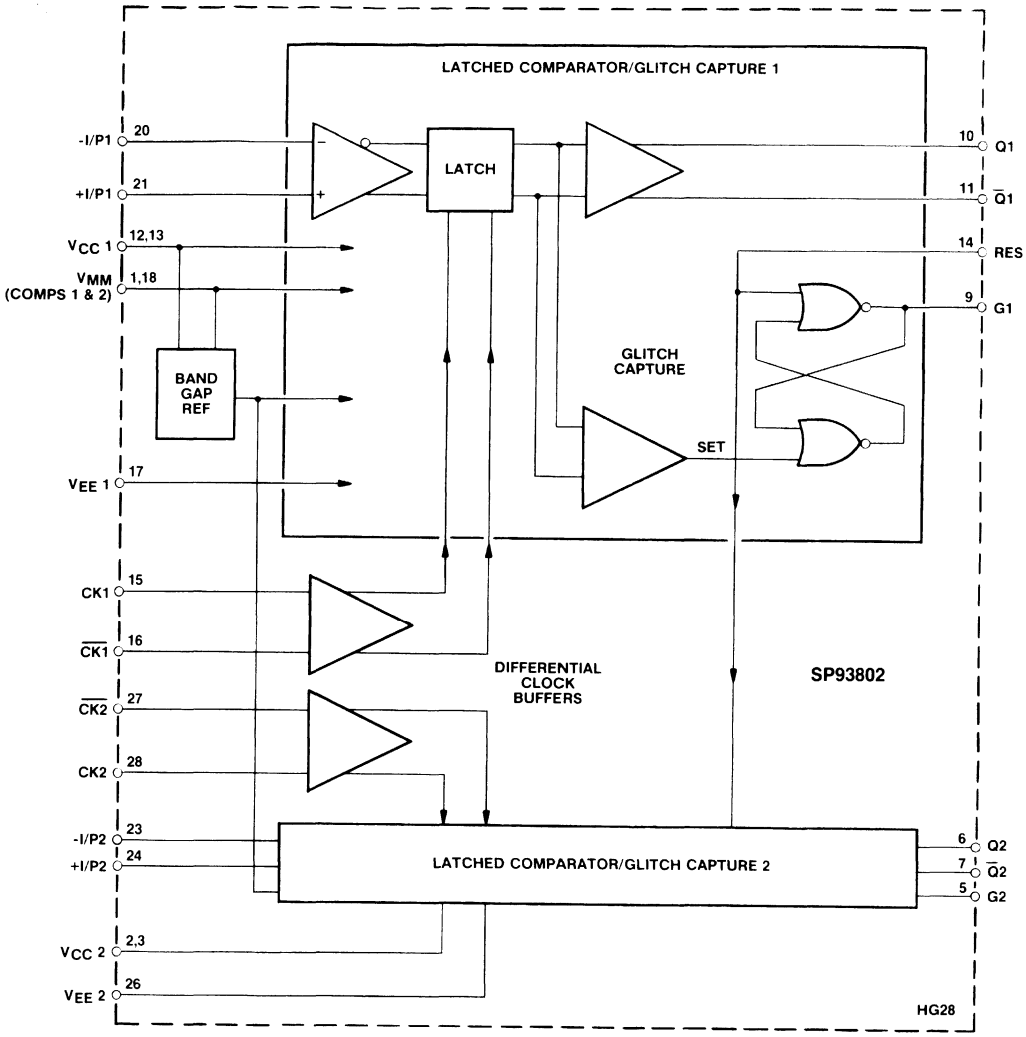


Fig.2 Internal block diagram, with pins shown for HG28 package (comparator 2 as detailed for comparator 1)

PIN FUNCTIONS

Name	HG28 Pin	Description
$V_{CC}1$	13,12	Positive supply connection for comparator 1 and the bandgap reference.
$V_{CC}2$	2,3	Positive supply connection for comparator 2.
-I/Pn ·I/Pn	20/23, 21/24	Inverting and non-inverting inputs to comparators 1 and 2, respectively.
Qn/$\overline{Q}$n	10/11, 6/7	Q and $\overline{Q}$ outputs of comparators 1 and 2, respectively.
Gn	9,5	Outputs of glitch capture circuits 1 and 2, respectively.
RESET	14	Reset pin for glitch capture circuit. This active high ECL signal will set the outputs (Gn) of the Glitch capture circuits to '0'.
CLK1, $\overline{CLK}$1	15/16	Clock input pins for comparator 1. Active low signal which latches the outputs of comparator 1.
CLK2, $\overline{CLK}$2	28/27	Clock input pins for comparator 2. Active low signal which latches the outputs of comparator 2.
$V_{EE}1$	17	Negative supply voltage for comparator 1.
$V_{EE}2$	26	Negative supply voltage for comparator 2.
V_{MM}	1,18	Mid-supply voltage rail for reset, clock drivers, glitch capture and band gap ref.

OPERATING NOTES

Transparent Mode

The SP93802 has been designed to maximise high input impedance and minimise propagation delay.

While CLK is high ($\overline{CLK}$ low), the outputs of the comparators are unlatched and are therefore transparent, with a gain of typically 20dB. In this mode, for example, a 20mV input overdrive signal will result in a 200mV differential output.

For applications such as logic analyser probes etc. this output signal may then be passed along a transmission line to a second SP93802 to enable strobing at a remote point from the comparator. Thus the gain and delay has been distributed within the application. The net result is reduced overall propagation delay and reduced channel to channel time skew.

In the transparent mode of operation the glitch capture circuit is continuously active.

Latched Mode

The output of each comparator is strobed into a very high bandwidth latch by taking CLK low ($\overline{CLK}$ high). The latch will then regenerate and produce full ECL output levels. This method produces the minimum system propagation delay.

Supply Connections

The SP93802 operates from supply voltages of 0V, -5V and -10V (Fig.3) or ±5V (Fig.4). The choice of supply connections depends on the input voltage range required and also the input voltage of the following circuits. As the ECL outputs from this device are 0.8V down from V_{CC}, then to interface with other ECL circuits directly, supplies of 0V, -5V, -10V should be provided. This will give an input common mode range of -2.4V to -7.3V. Therefore when two devices are used in a system, the first (line driver) should have supplies as shown in Fig.3 and the second (line receiver) should have supplies as shown in Fig.4.

If it is inconvenient to provide the mid-supply voltage (V_{MM}), then a 5.1V Zener diode can be used. The current taken by this diode will be typically 32mA, see Fig.3.

The supply connections shown in Fig.3 give output levels that are directly compatible with ECL 10k inputs. An optional 5.1V Zener diode is shown; this is only required if a -5V supply is not available.

The SP93802 ECL outputs can be connected directly to other ECL circuitry if these circuits are supplied from the +5V and 0V rails (O/PH, see Fig.4). Alternatively, a 5.1V Zener diode can be used to level shift the outputs for connection to standard ECL circuits supplied from the 0V and -5V rails.

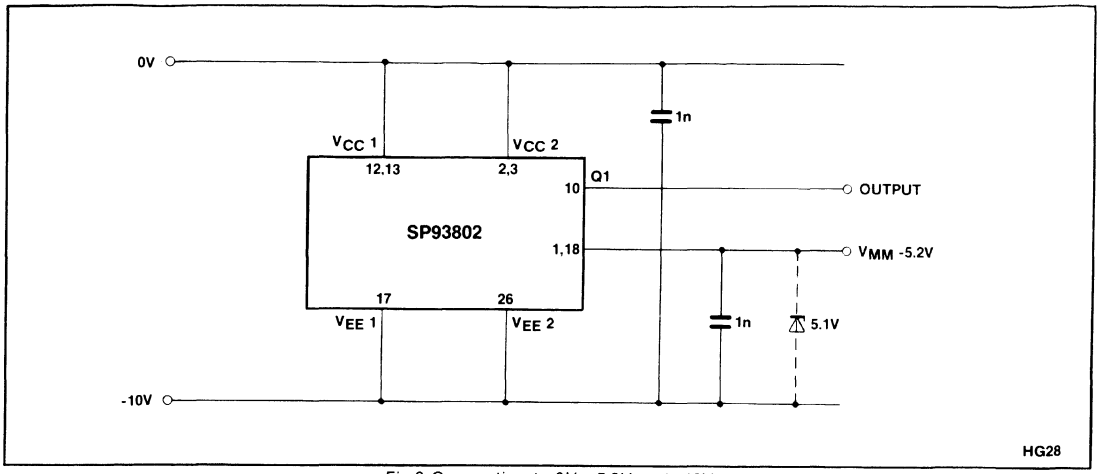


Fig.3 Connection to 0V, -5.2V and -10V

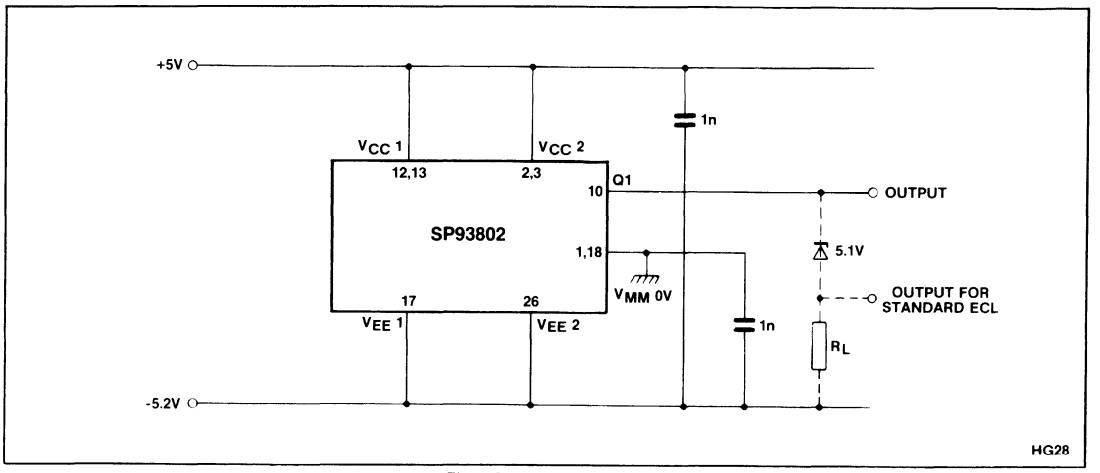


Fig.4 Connection to ±5V

External Components

The Qn, $\overline{Q}$n and Gn outputs are open emitters and therefore required external pulldown resistors (R_L). These resistors may be in the range of 50-250Ω connected to V_{CC}-2V (V_T) or 250-2000Ω connected to V_{MM}.

Due to the sub-ns conversion speeds and edge speeds of this device, the performance is dependent on both board layout and component placement.

The performance of the comparator is enhanced by minimising the number of external components and minimising the external strays around the device. The use of high quality chip resistors is recommended, especially for loads.

Decoupling capacitors should be positioned close to the device supply pins. Decoupling between supplies and V_{EE} is also recommended.

The device has been packaged for maximum isolation between channels. This has been achieved by positioning an un-bonded (not internally connected) pin between each set of comparator inputs. These N/C pins can be connected to the ground plane, providing further isolation.

Clock Inputs

The SP93802 can be used in transparent mode by connecting the CLK input to ECL '1' and the $\overline{CLK}$ input to an ECL '0'. The device can also be used as two single comparators as both comparators can be clocked separately.

As the device contains two clock input buffers, a range of clock input configurations are possible. With the device V_{CC} connected to 0V the clock inputs will accept standard differential ECL signals. However optimum performance in terms of crosstalk will be achieved with a differential input of 400mV p-p.

$\overline{CLK1}$ (pin 15) comparator 1 latched when low.
CLK1 (pin 16) inverse clock for comparator 1.
$\overline{CLK2}$ (pin 28) comparator 2 latched when low.
CLK2 (pin 27) inverse clock for comparator 2.

The clock inputs should have fast rise times and low jitter. The Plessey SP92701 line receiver can be used to clean up the clock signal and provide a good differential ECL drive for this comparator.

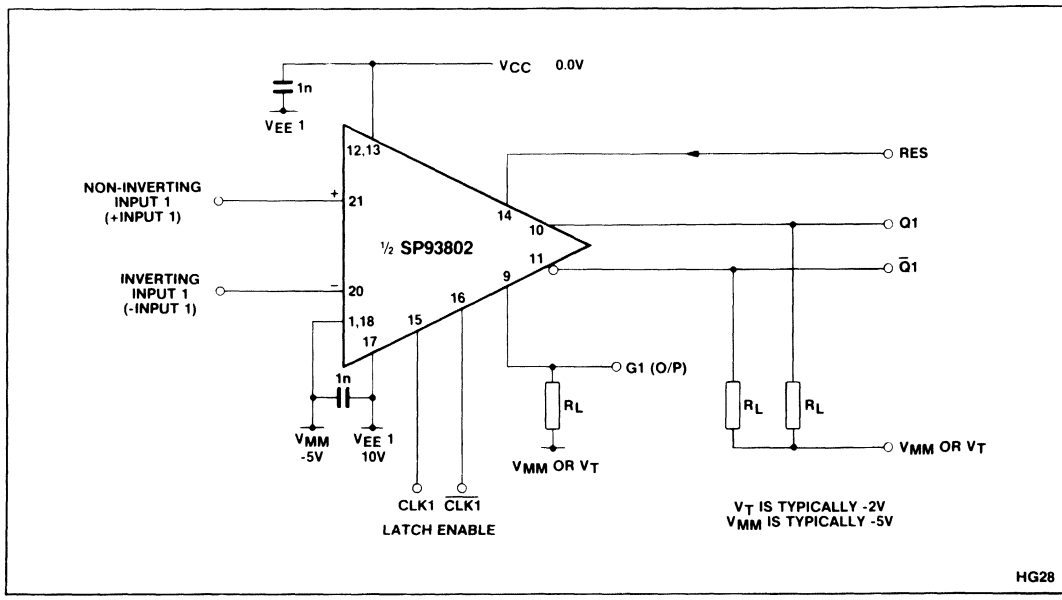


Fig.5 Applications circuit (one channel)

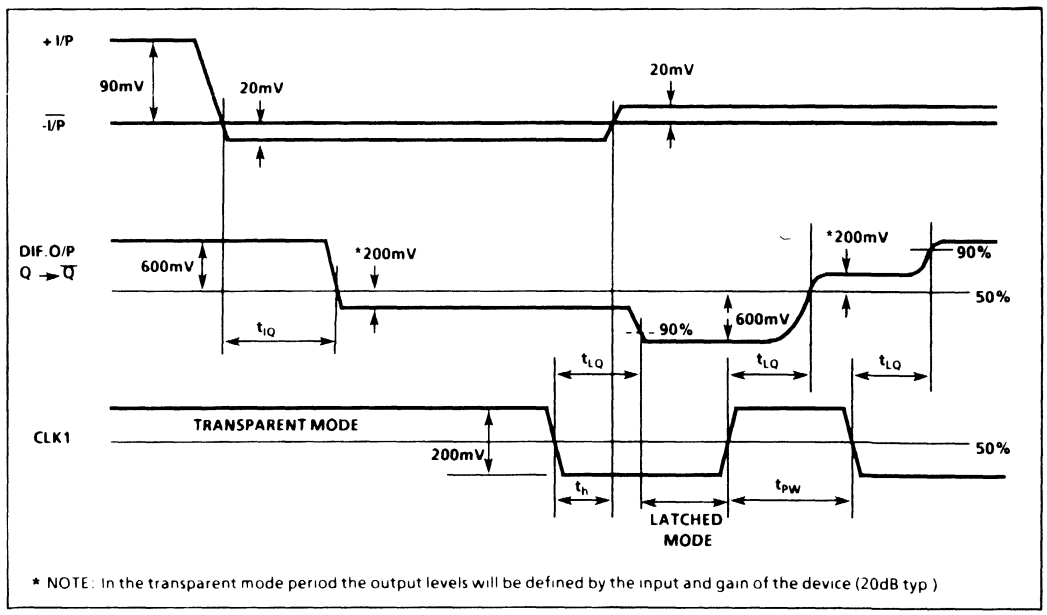


Fig.6 Comparator timing diagram

I/P	CLK	Qn + 1
X	0	Qn
1	1	1
0	1	0

X = Don't Care

Table 1 Truth table for comparator

RES	SET(1) (n + 1)	Gn + 1
1	X	0
0	↗	↗
0	↘	1
0	1	1
0	0	Gn(2)
↘	1	↗
↘	0	0

X = Don't Care

Table 2 Truth table for glitch capture circuit

Glitch Capture Circuit

This advanced feature enables the device to capture sub-nanosecond glitches that may have occurred before the comparator is latched.

The glitch capture circuit (see Fig.2) can be reset at any time by the RES input. When held at ECL '1' (V_{CC} - 0.8V) the RES pin will reset the Gn output to '0' (ECL low). Glitch capture is active when the RES pin is taken low.

If Qn goes positive by more than 20mV for a time $>t_{RD}$ then the Gn output will be set to an ECL '1', it will remain in this state until the RES pin is again taken high.

NOTES
1. SET is the input to the glitch capture circuit and is logically the same as the Q output from the comparator, see Fig.8
2. Gn = 1 is evidence that a transition has occurred at the Q output since the last falling edge of the reset pulse.

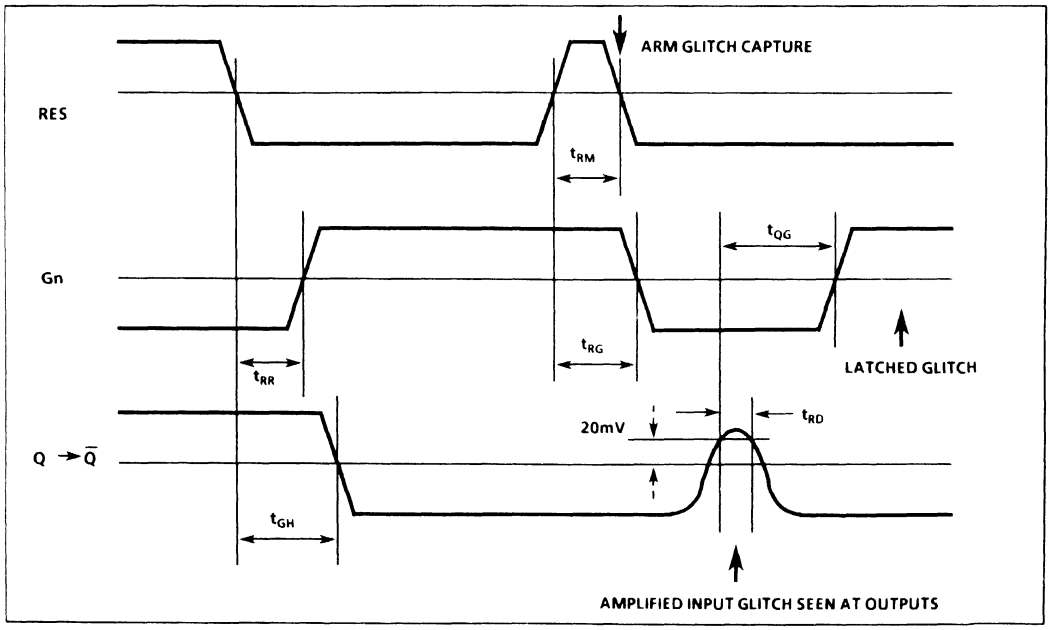
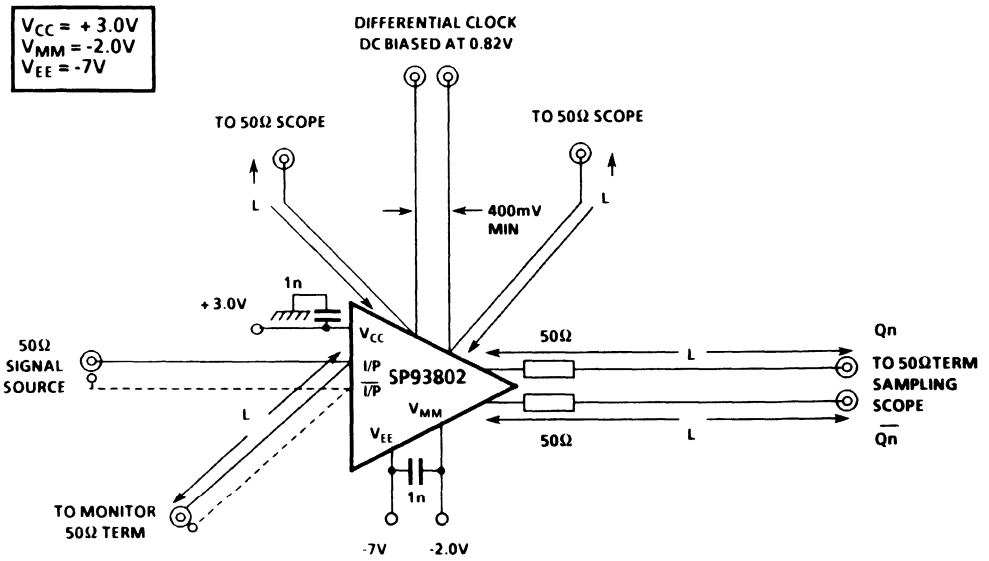


Fig.7 Glitch capture circuit timing



NOTES:-

The supplies have been chosen to allow direct connection of both the outputs and monitor points to measurement instruments with 50Ω input impedance.

1) Lead lengths should be as short as possible and also of equal length. (equal delay).
2) Decoupling should be close to the device (chip type if possible).
3) Use coaxial cables or stripline techniques in board construction.
4) Monitor and both scope channel 50Ω loads must be in circuit for correct termination.
5) A Plessey SP92701 can be used with supplies of +3V and -2V, to drive the clock input. The outputs of the SP92701 should have series 100Ω resistors to reduce the differential swing.

Fig.8 Comparator dynamic test circuit (one channel)

APPLICATION NOTES

High Gain Applications

Increased gain can be obtained on one channel by tying the Qn output to the Reset input. A Q phase ECL signal is then obtained from the Gn output. Approximately 40dB gain is achieved.

Trigger Circuits

A narrow trigger pulse can be obtained directly from one of the two comparators. This is achieved by tying the Qn signal to the Reset input. The trigger pulse is obtained from the Gn output and is approximately 1ns wide, positive going and occurs synchronously with the rising edge of the conventional Q signal.

Construction of Evaluation Board (DG22 Package)

This application board demonstrates the capability of the SP93802 functioning at 500MHz and produces edge speeds of less than one nanosecond.

In the application circuit (Fig.9) for the SP93802 both of the channels are driven together and clocked differentially.

V_{MM} is generated by a Zener diode (5.1V) from the V_{CC} (+3V) and V_{EE} (-7V).

CLK, $\overline{CLK}$, RES inputs are biased for 50Ω termination.

Inverting inputs (18,15) and unused pin (17) should be tied to ground.

Input pins (16,19) are terminated by 50Ω monitor or scope channel to provide the correct terminations.

Outputs Q, $\overline{Q}$ (8,5,7,4) and glitch capture outputs G1,G2(6,3) are terminated through 50Ω series resistors to 50Ω wideband scope channel.

CLK, $\overline{CLK}$ and RESET signals can be generated from the input signal through a divide-by-two (Plessey SP9131, 520MHz ECL dual D-type flip-flop used in cascade to form a divide-by-2 and 4), so no external synchronisation is then needed. The latched outputs can be seen on the scope at 1/2 the normal ECL levels. Alternatively the CLK, $\overline{CLK}$, RESET signals from any other sources can be used phase locked to the input. The Plessey SP92701 is useful for driving the CLK lines.

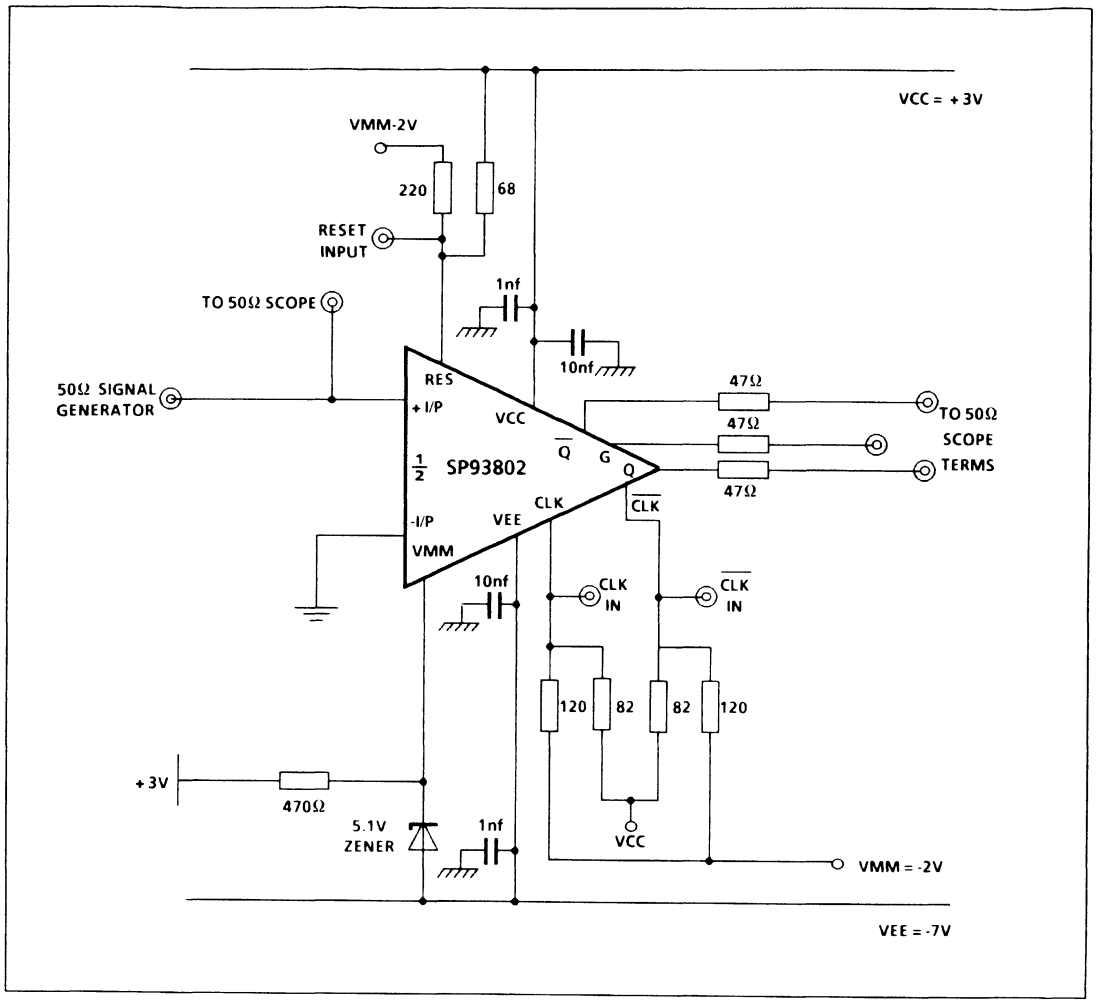


Fig.9 SP93802 application board diagram for one channel

Function	V_{MM}	NC	V_{EE}	CLK	$\overline{CLK}$	Q
Pin/DG22	1,14	17	13,20	11,22	12,21	4,7

Function	$\overline{Q}$	G	V_{CC}	RES	+I/P	-I/P
Pin/DG22	5,8	3,6	2,9	10	16,19	15,18

Table 3 SP93802 pin connections (DG22)

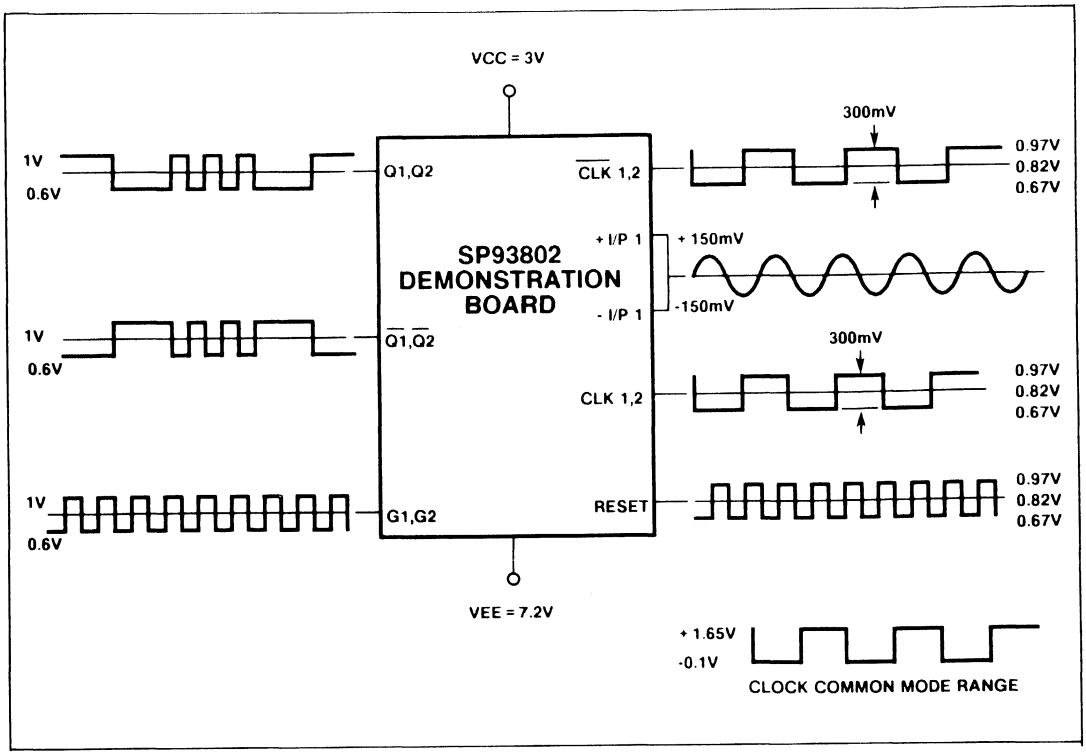
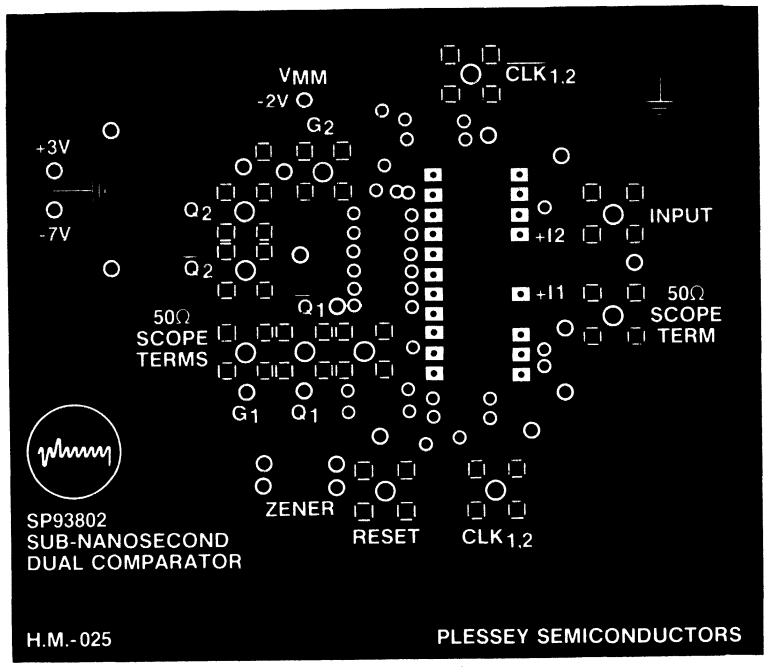
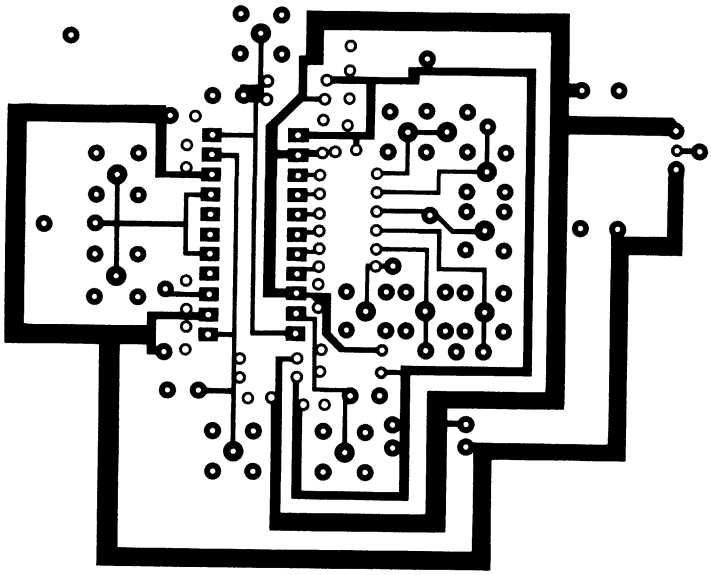


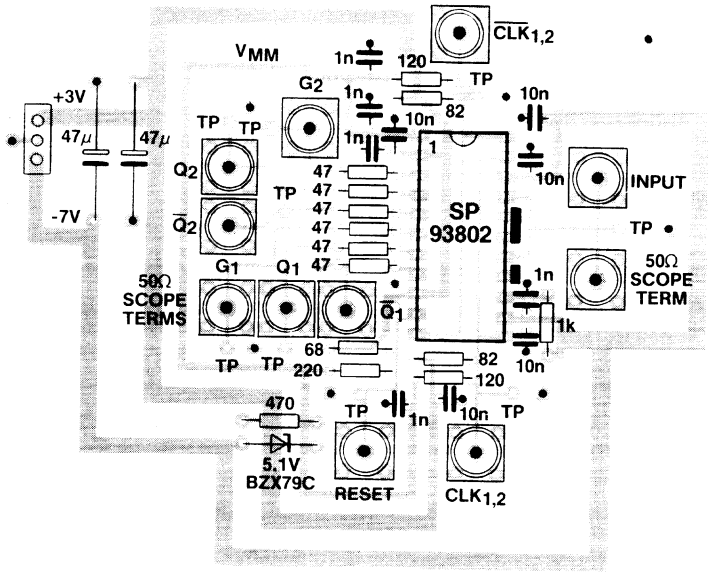
Fig.10 Bias and timing diagram for SP83802 application board



(a) SP93802 ground plane



(b) SP93802 evaluation board, track side



(c) SP93802 evaluation board, component layout

Fig.11 PCB layout for SP93802 demonstration board (circuit of Fig.9). Scale 1:1

PLESSEY
Semiconductors

SP93804

SUB-NANOSECOND QUAD COMPARATOR/GLITCH DETECTOR

(SUPERSEDES AUGUST 1987 DATABOOK EDITION)

The Plessey SP93804 contains four independent matched ultra high speed comparators. Each comparator is followed by a latch which may be used to sample the comparator output. The gain of this comparator has been optimised for low propagation delay and high stability, therefore hysteresis is rarely required.

Each channel includes a glitch capture circuit which enables the detection and latching of a 20mVns output glitch, when the device is in compare mode. The SP93804 can also be used as two matched dual devices, due to comparators 1 and 2 being clocked separately from comparators 3 and 4.

Special attention has been paid to the clock circuit and packaging to minimise crosstalk.

These features are not only beneficial to logic analyser and counter designs, but also in many other high speed data conversion or data communication systems.

ORDERING INFORMATION

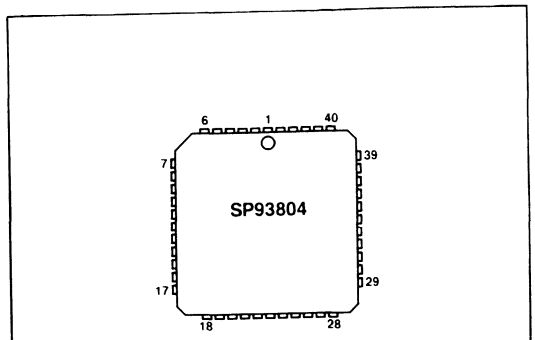
SP93804 B HG (Industrial Quad Cerpac (J-Form) package)

FEATURES

- -40°C to +85°C Temperature Range
- Typical Delay <1ns
- Glitch Capture, 20mVns (Typ.)
- On Chip Band Gap Reference Circuitry
- 50 Ohm Drive Capability
- On Chip Clock Buffers
- 4 Matched Comparator/Latched Channels
- Channel Propagation Delay Matching <100ps
- High Input Impedance
- Dual and Octal Versions SP93802/SP93808

APPLICATIONS

- Automatic Test Equipment
- Instrumentation
- Line Receiver/Driver
- Cascadable Differential Amplifier
- Analog to Digital Conversion
- Fibre Optics
- Logic Analysers



HG44

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	I/P Vcc2	12	NC	23	VMM	34	NC
2	O/P Vcc2	13	G2	24	RES	35	-I/P3
3	G4	14	$\overline{NC}$	25	$\overline{CLK1}$	36	+I/P3
4	$\overline{NC}$	15	$\overline{Q2}$	26	$\overline{CLK1}$	37	NC
5	$\overline{Q4}$	16	Q2	27	VEE1	38	-I/P4
6	Q4	17	NC	28	VMM	39	+I/P4
7	NC	18	$\overline{G1}$	29	-I/P1	40	NC
8	G3	19	$\overline{Q1}$	30	+I/P1	41	$\overline{VEE2}$
9	$\overline{NC}$	20	Q1	31	NC	42	$\overline{CLK2}$
10	$\overline{Q3}$	21	O/P Vcc1	32	-I/P2	43	CLK2
11	Q3	22	I/P Vcc1	33	+I/P2	44	VMM

Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage Vcc - VMM	+6V
Supply voltage VMM - VEE	-6V
Operating temperature range	-40°C to +85°C
Storage temperature range	-55°C to +125°C
Output current	≤30mA
Maximum input voltage	
Common mode positive	≤Vcc
Common mode negative	≥VEE
Differential input voltage	≤±3.8V

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = -40°C to +85°C, I/P and O/P V_{CC} = +5V ± 0.25V,
V_{EE} = -5V ± 0.25V, V_{MM} = 0V (see Fig.4), Load = 50Ω to V_{CC} -2V

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Positive supply current	I_{CC}		38.5	50	mA	V_{CC} = 5V, V_{EE} = -5V No load. Each comparator.
Negative supply current	I_{EE}		16.0	21	mA	V_{CC} = 5V, V_{EE} = -5V No load. Each comparator.
Positive supply voltage	V_{CC}	I/P MAX +1.55	5.0	I/P MIN +7.3	V	
Negative supply voltage	V_{EE}	-5.5	-5.0	-4.9	V	
Input offset voltage	V_{OS}	-3.5		+3.5	mV	
Input bias current	I_B		5.25	9	μA	
Input offset current	I_{OS}		0.95	1.2	μA	
Input capacitance	C_I		1.5 (Note 1)		pF	
Input impedance	R_I		250		kΩ	Measured at DC
Differential input range	V_{DIF}			±3.8	V	
Common mode input range	CMIR	-2.1		+2.6	V	
Output voltage high	V_{OH}	V_{CC}-1.050		V_{CC}-0.81	V	+25°C, V_{IN} > 60mV
		V_{CC}-1.140		V_{CC}-0.91	V	-40°C, V_{IN} > 60mV
		V_{CC}-0.965		V_{CC}-0.704	V	+85°C, V_{IN} > 60mV
Output voltage low	V_{OL}	V_{CC}-1.712		V_{CC}-1.544	V	+25°C, V_{IN} < -60mV
		V_{CC}-1.792		V_{CC}-1.650	V	-40°C, V_{IN} < -60mV
		V_{CC}-1.638		V_{CC}-1.465	V	+85°C, V_{IN} < -60mV
Gain (transparent mode)			20		dB	Differential
Common mode rejection	CMRR	50	50		dB	+25°C, with respect to I/P
Supply voltage rejection	PSRR		70		dB	+25°C, with respect to I/P offset
Clock input:						
Common mode range	CMRC	V_{MM}+2V		V_{CC}-1.35V	V	
Differential swing	DS	400		1600	mV	

NOTES 1 Guaranteed but not tested

Dynamic Characteristics (Note 1)

See dynamic test circuit Fig.9.

Characteristic	Symbol	Value			Units	Condition
		Min.	Typ.	Max.		
Latch setup time	t_S		150		ps	20mV overdrive
Hold time	t_H		600		ps	20mV overdrive
Input to Q delay	t_{IQ}		800		ps	20mV overdrive
Latch to Q delay	t_{LQ}		1500		ps	20mV overdrive
Glitch capture regeneration	t_{RD}		900		ps	20mV overdrive at Qn
Propagation delay matching	t_{PDM}	-100		+100	ps	Within each device
Min. compare pulse width	t_{PW}		950		ps	20mV overdrive
Min. reset pulse width	t_{RM}		800		ps	
Max. flip flop reset time	t_{RR}		800		ps	
Min. hold time of Qn after reset	t_{GH}		800		ps	
Delay between Qn and Gn	t_{OG}		900		ps	
Propagation delay RES to Gn	t_{RG}		800		ps	

NOTES 1 Guaranteed but not tested

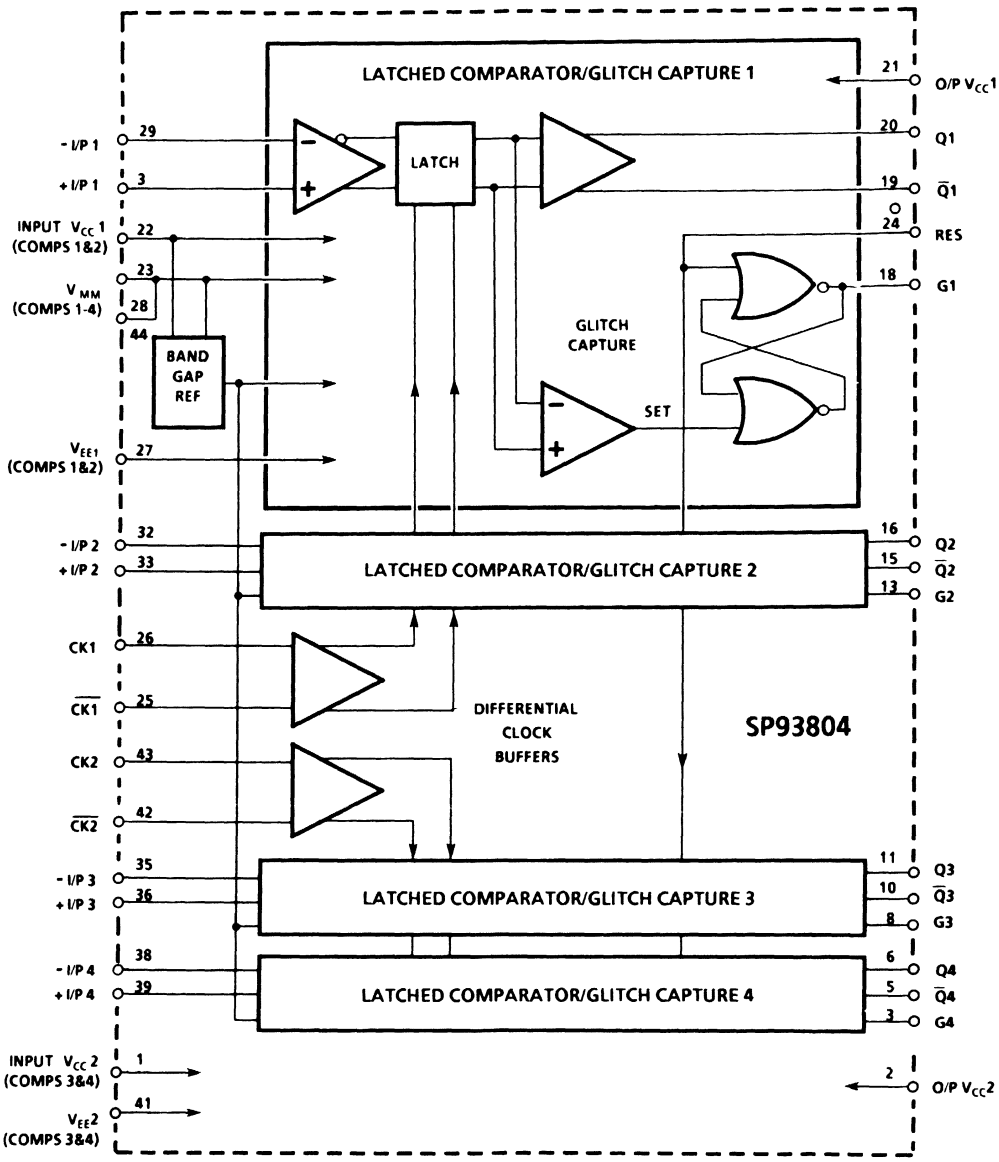


Fig.2 Internal block diagram (all comparators are as detailed for comparator 1)

PIN FUNCTIONS

Name	Pin	Description
I/P $V_{CC}1$	22	Positive supply connection for comparators 1 and 2, and the bandgap reference.
O/P $V_{CC}1$	21	Positive supply connection for the outputs Qn, $\overline{Qn}$ and Gn of comparators 1 and 2 (emitter follower outputs, see Fig.5).
I/P $V_{CC}2$	1	Positive supply connection for comparators 3 and 4.
O/P $V_{CC}2$	2	Positive supply connection for the outputs Qn, $\overline{Qn}$ and Gn of comparators 3 and 4 (emitter follower outputs, see Fig.5).
-I/Pn +I/Pn	29/32, 35/38, 30/33, 36/39	Inverting and non-inverting inputs to comparators 1 to 4, respectively.
Qn/$\overline{Qn}$	6/5, 11/10, 16/15, 20/19	Q and Q outputs of comparators 1 to 4, respectively.
Gn	18,13,8,3	Outputs of glitch capture circuits 1 to 4, respectively.
RES	24	Reset pin for glitch capture circuit. This active high ECL signal will set the outputs (Gn) of the Glitch capture circuits to '0'.
CLK1, $\overline{CLK1}$	25, 26	Clock input pins for comparators 1 and 2. Active low signal which latches the outputs of comparators 1 and 2.
CLK2, $\overline{CLK2}$	42, 43	Clock input pins for comparators 3 and 4. Active low signal which latches the outputs of comparators 3 and 4.
$V_{EE}1$	27	Negative supply voltage for comparators 1 and 2.
$V_{EE}2$	41	Negative supply voltage for comparators 3 and 4.
V_{MM}	23,44,28	Mid-supply voltage rail for reset, clock drivers, glitch capture and band gap ref.

OPERATING NOTES

Transparent Mode

The SP93804 has been designed to maximise high input impedance and minimise propagation delay whilst maintaining a high gain.

While CLK is high ($\overline{CLK}$ low), the outputs of the comparators are unlatched and are therefore transparent, with a gain of typically 20dB. In this mode, for example, a 20mV input overdrive signal will result in a 200mV differential output.

For applications such as logic analyser probes etc. this output signal may then be passed along a transmission line to a second SP93804 to enable strobing at a remote point from the comparator. Thus the gain and delay has been distributed within the application. The net result is reduced overall propagation delay and reduced channel to channel time skew.

In the transparent mode of operation the glitch capture circuit is continuously active.

Latched Mode

The output of each comparator is strobed into a very high bandwidth latch by taking CLK low ($\overline{CLK}$ high). The latch will then regenerate and produce full ECL output levels. This method produces the minimum system propagation delay.

Supply Connections

The SP93804 operates from supply voltages of 0V, -5V and -10V (Fig.3) or ±5V (Fig.4). The choice of supply connections depends on the input voltage range required and also the input voltage of the following circuits. As the ECL outputs from this device are 0.8V down from V_{CC}, then to interface with other ECL circuits directly, supplies of 0V, -5V, -10V should be provided. This will give an input common mode range of -2.4V to -7.3V. Therefore when two devices are used in a system, the first (line driver) should have supplies as shown in Fig.3 and the second (line receiver) should have supplies as shown in Fig.4.

If it is inconvenient to provide the mid-supply voltage (V_{MM}), then a 5.1V Zener diode can be used. The current taken by this diode will be typically 32mA, see Fig.3.

Note that the O/P V_{CC} pins are connected to the collectors of the output emitter followers; load return currents should therefore be directed towards these device pins.

The supply connections shown in Fig.3 give output levels that are directly compatible with ECL 10k inputs. An optional 5.1V Zener diode is shown; this is only required if a -5V supply is not available.

The SP93804 ECL outputs can be connected directly to other ECL circuitry if these circuits are supplied from the +5V and 0V rails (O/PH, see Fig.4). Alternatively, a 5.1V Zener diode can be used to level shift the outputs for connection to standard ECL circuits supplied from the 0V and -5V rails.

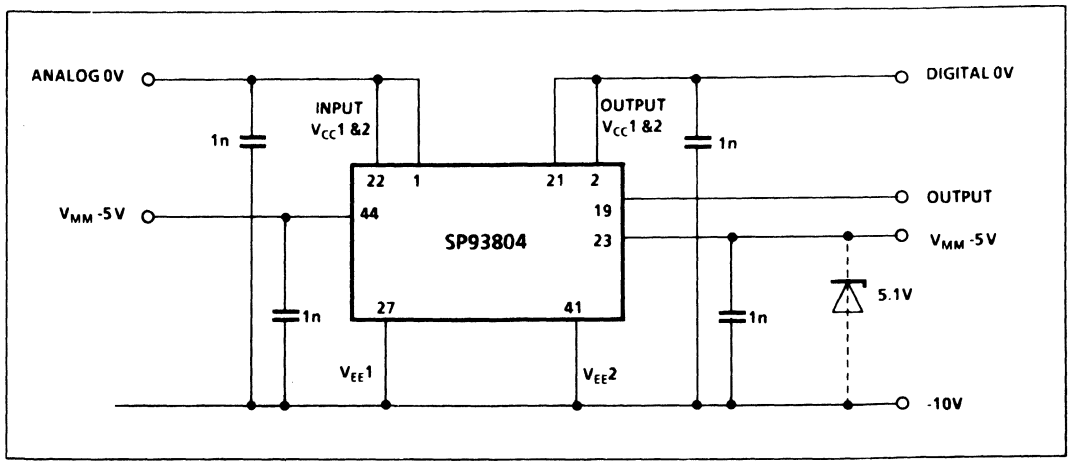


Fig.3 Connection to 0V, -5V and -10V

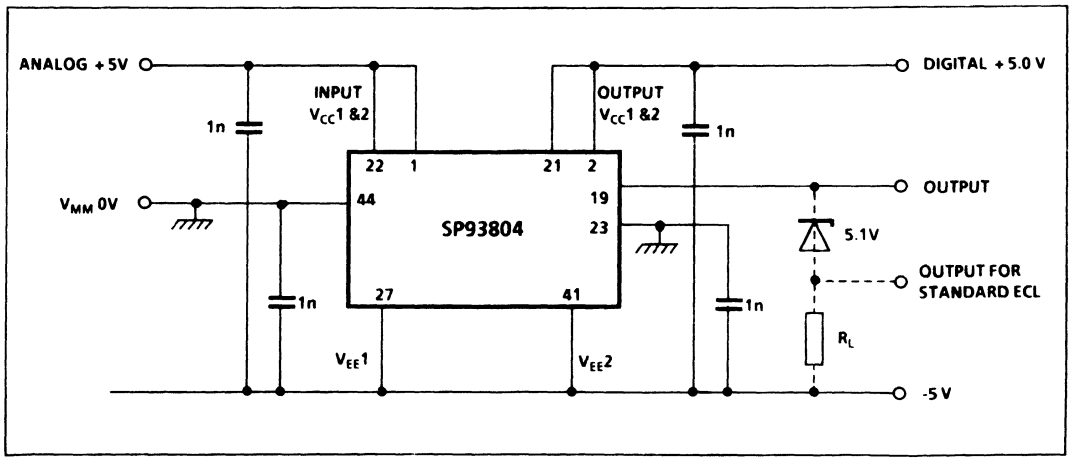


Fig.4 Connection to ±5V

External Components

The Qn, $\overline{Q}$n and Gn outputs are open emitters and therefore required external pulldown resistors (R_L). These resistors may be in the range of 50-250Ω connected to V_{CC}-2V (V_T) or 250-2000Ω connected to V_{MM}.

Due to the sub-ns conversion speeds and edge speeds of this device, the performance is dependent on both board layout and component placement.

The performance of the comparator is enhanced by minimising the number of external components and minimising the external strays around the device. The use of high quality chip resistors is recommended, especially for loads.

Decoupling capacitors should be positioned close to the device supply pins. Decoupling between supplies and V_{EE} is also recommended.

The device has been packaged for maximum isolation between channels. This has been achieved by positioning an un-bonded (not internally connected) pin between each set of comparator inputs. These N/C pins can be connected to the ground plane, providing further isolation.

Clock Inputs

The SP93804 can be used in transparent mode by connecting the CLK input to ECL '1' and the $\overline{CLK}$ input to an ECL '0'. The device can also be used as two dual comparators as comparators 1 and 2 can be clocked separately from comparators 3 and 4.

As the device contains two clock input buffers, a range of clock input configurations are possible. With the device V_{CC} connected to 0V the clock inputs will accept standard differential ECL signals. However optimum performance in terms of crosstalk will be achieved with a differential input of 400mV p-p.

A range of clock input configurations are possible according to the various supply operating.

CLK1 (pin 25) comparators 1 and 2 latch when low.
$\overline{CLK1}$ (pin 26) inverse clock for comparators 1 and 2.
CLK2 (pin 43) comparators 3 and 4 latch when low.
$\overline{CLK2}$ (pin 42) inverse clock for comparators 3 and 4.

The clock inputs should have fast rise times and low jitter. The Plessey SP92701 line receiver can be used to clean up the clock signal and provide a good differential ECL drive for this comparator.

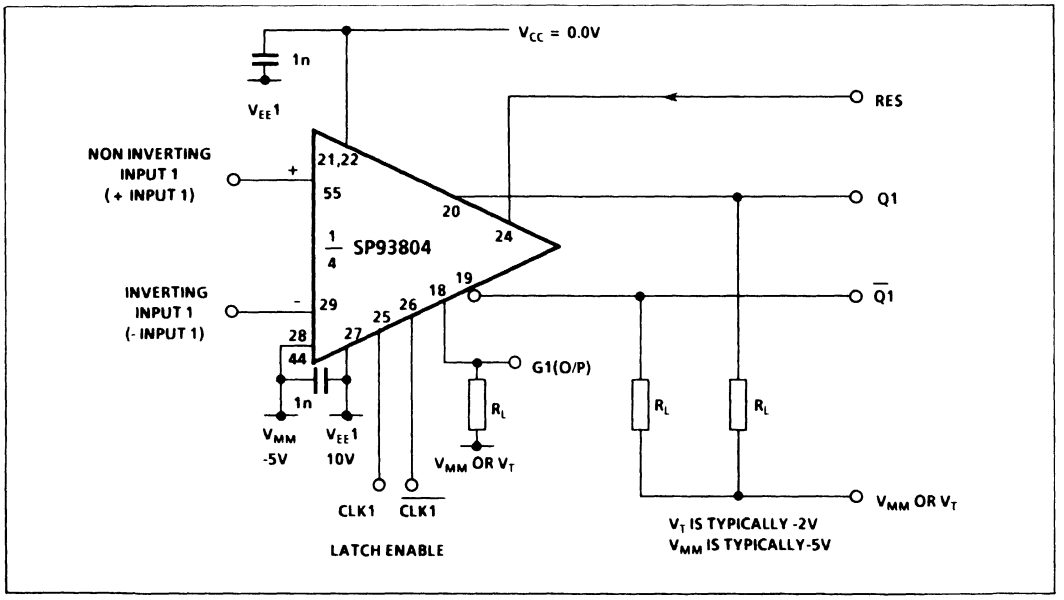


Fig.5 Applications circuit (one channel)

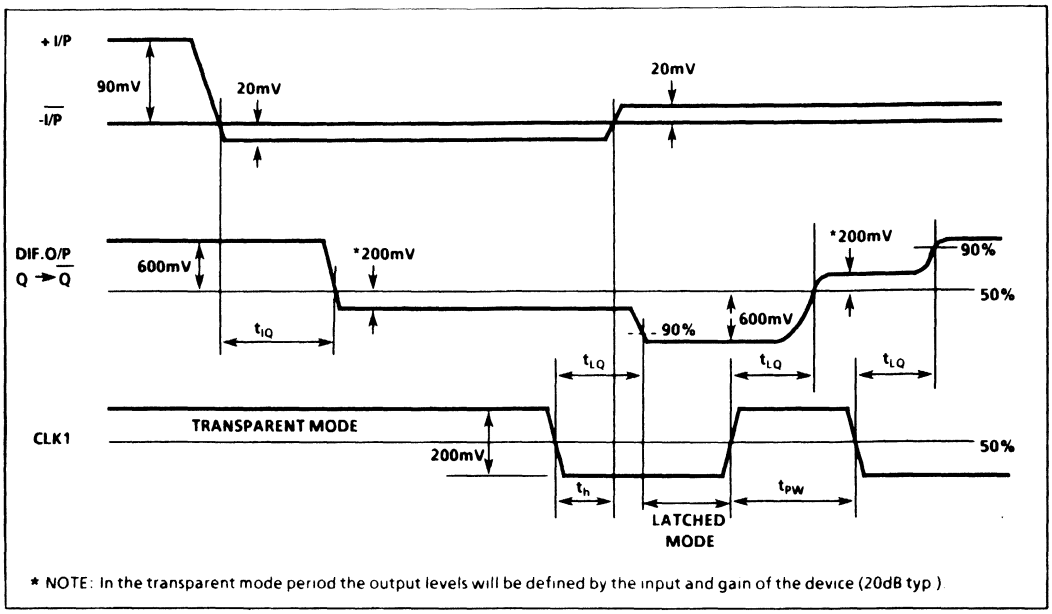


Fig.6 Comparator timing diagram

I/P	CLK	Qn + 1
X	0	Qn
1	1	1
0	1	0

X = Don't Care

Table 1 Truth table for comparator

RES	SET(1) (n + 1)	Gn + 1
1	X	0
0	↗	↗
0	↘	1
0	1	1
0	0	Gn(2)
↘	1	↗
↘	0	0

X = Don't Care

Table 2 Truth table for glitch capture circuit

Glitch Capture Circuit

This advanced feature enables the device to capture sub-nanosecond glitches that may have occurred before the comparator is latched.

The glitch capture circuit (see Fig.2) can be reset at any time by the RES input. When held at ECL '1' (V_{CC}-0.8V) the RES pin will reset the Gn output to '0' (ECL low). Glitch capture is active when the RES pin is taken low.

If Qn goes positive by more than 20mV for a time $>t_{RD}$ then the Gn output will be set to an ECL '1', it will remain in this state until the RES pin is again taken high.

NOTES
1. SET is the input to the glitch capture circuit and is logically the same as the Q output from the comparator, see Fig.8.
2. Gn = 1 is evidence that a transition has occurred at the Q output since the last falling edge of the reset pulse.

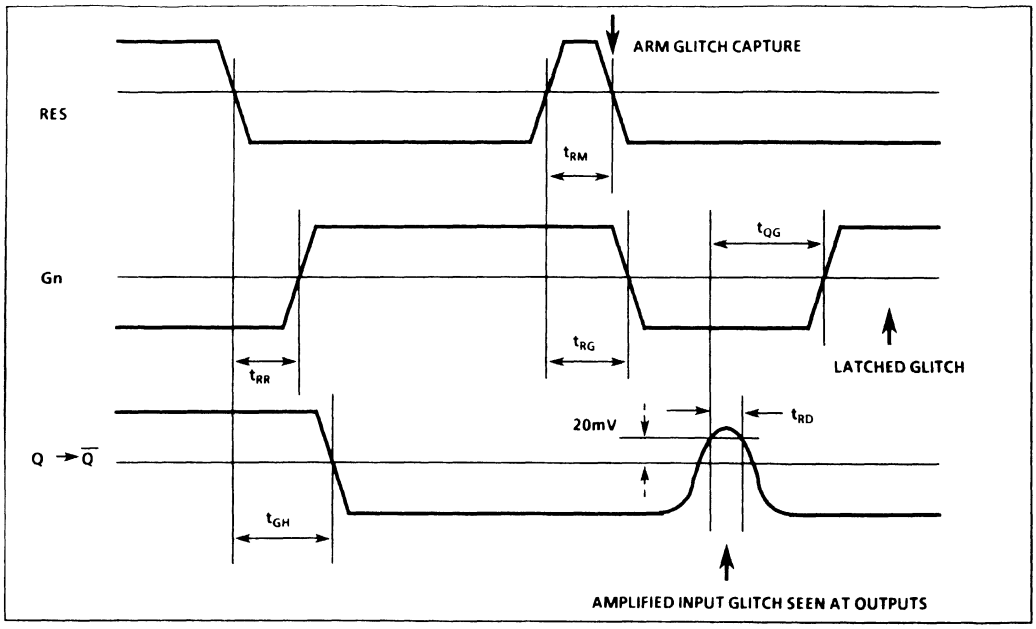
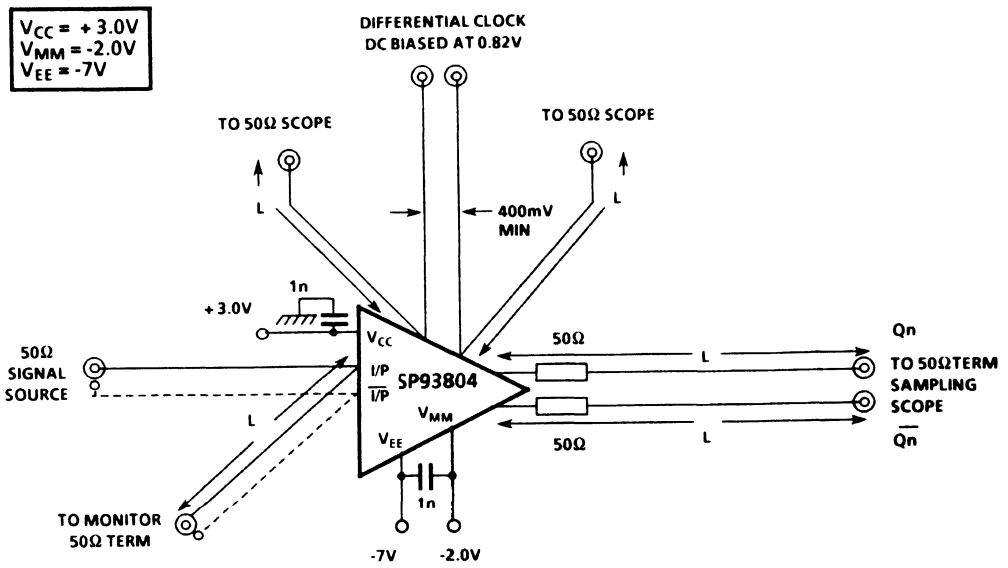


Fig.7 Glitch capture circuit timing



NOTES:-

The supplies have been chosen to allow direct connection of both the outputs and monitor points to measurement instruments with 50Ω input impedance.

1) Lead lengths should be as short as possible and also of equal length. (equal delay).
2) Decoupling should be close to the device (chip type if possible).
3) Use coaxial cables or stripline techniques in board construction.
4) Monitor and both scope channel 50Ω loads must be in circuit for correct termination.
5) A Plessey SP92701 can be used with supplies of +3V and -2V, to drive the clock input. The outputs of the SP92701 should have series 100Ω resistors to reduce the differential swing.

Fig.8 Comparator dynamic test circuit (one channel)

SP93808

SUB-NANOSECOND OCTAL COMPARATOR

(SUPERSEDES AUGUST 1987 DATABOOK EDITION)

The Plessey SP93808 contains eight independent matched ultra high speed comparators. Each comparator is followed by a latch which may be used to sample the comparator output. The gain of this comparator has been optimised for low propagation delay and high stability, therefore hysteresis is rarely required.

Each channel includes a glitch capture circuit which enables the detection and latching of a 20mVns output glitch, when the device is in compare mode. The SP93808 can also be used as two matched quad devices, due to comparators 1 to 4 being clocked separately from comparators 5 to 8.

Special attention has been paid to the clock circuit and packaging to minimise crosstalk.

These features are not only beneficial to logic analyser and counter designs, but also in many other high speed data conversion or data communication systems.

ORDERING INFORMATION

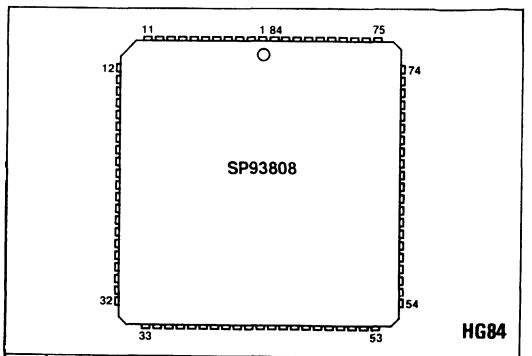
SP93808 B HG (Industrial - Quad Cerpac (J-Form) package)

FEATURES

- -40°C to +85°C Temperature Range
- Typical Delay <1ns
- Glitch Capture, 20mVns (Typ.)
- On Chip Band Gap Reference Circuitry
- 50 Ohm Drive Capability
- On Chip Clock Buffers
- 8 Matched Comparator/Latched Channels
- Channel Propagation Delay Matching <100ps
- High Input Impedance
- Dual and Quad Versions SP93802/SP93804

APPLICATIONS

- Automatic Test Equipment
- Instrumentation
- Line Receiver/Driver
- Cascadable Differential Amplifier
- Analog to Digital Conversion
- Fibre Optics
- Logic Analysers



Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	O/P Vcc2	22	G4	43	I/P Vcc1	64	+I/P4
2	GB	23	NC	44	VMM	65	NC
3	NC	24	Q4	45	RES	66	-I/P5
4	Q8	25	$\overline{Q4}$	46	NC	67	+I/P5
5	$\overline{Q8}$	26	NC	47	CLK1	68	NC
6	NC	27	G3	48	$\overline{CLK1}$	69	-I/P6
7	G7	28	NC	49	NC	70	+I/P6
8	NC	29	Q3	50	VEE1	71	NC
9	Q7	30	$\overline{Q3}$	51	VEE1	72	-I/P7
10	$\overline{Q7}$	31	NC	52	VMM	73	+I/P7
11	NC	32	G2	53	NC	74	NC
12	G6	33	NC	54	-I/P1	75	-I/P8
13	NC	34	Q2	55	+I/P1	76	+I/P8
14	Q6	35	$\overline{Q2}$	56	NC	77	NC
15	$\overline{Q6}$	36	NC	57	-I/P2	78	VEE2
16	NC	37	G1	58	+I/P2	79	VEE2
17	G5	38	NC	59	NC	80	$\overline{CLK2}$
18	NC	39	Q1	60	-I/P3	81	CLK2
19	Q5	40	$\overline{Q1}$	61	+I/P3	82	VMM
20	$\overline{Q5}$	41	O/P Vcc1	62	NC	83	I/P Vcc2
21	NC	42	O/P Vcc1	63	-I/P4	84	O/P Vcc2

Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage Vcc - VMM	+6V
Supply voltage VMM - VEE	-6V
Operating temperature range	-40°C to +85°C
Storage temperature range	-55°C to +125°C
Output current	≤30mA
Maximum input voltage	
Common mode positive	≤Vcc
Common mode negative	≥VEE
Differential input voltage	≤±3.8V

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} -40°C to +85°C, I/P and O/P V_{CC} = +5V ± 0.25V,
V_{EE} = -5V ± 0.25V, V_{MM} = 0V (see Fig.4), Load = 50Ω to V_{CC} - 2V

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Positive supply current	I_{CC}		65.5	84	mA	V_{CC} = 5V, V_{EE} = -5V No load. Each comparator.
Negative supply current	I_{EE}		33.0	42	mA	V_{CC} = 5V, V_{EE} = -5V No load. Each comparator.
Positive supply voltage	V_{CC}	I/P MAX +1.55	5.0	I/P MIN +7.3	V	
Negative supply voltage	V_{EE}	-5.5	-5	-4.9	V	
Input offset voltage	V_{OS}	-3.5		+3.5	mV	
Input bias current	I_B		5.25	9	μA	
Input offset current	I_{OS}		0.95	1.2	μA	
Input capacitance	C_I		1.5 (Note 1)		pF	
Input impedance	R_I		250		kΩ	Measured at DC
Differential input range	V_{DIF}			±3.8	V	
Common mode input range	CMIR	-2.1		+2.6	V	
Output voltage high	V_{OH}	V_{CC}-1.050		V_{CC}-0.81	V	+25°C, V_{IN} > 60mV
		V_{CC}-1.140		V_{CC}-0.91	V	-40°C, V_{IN} > 60mV
		V_{CC}-0.965		V_{CC}-0.704	V	+85°C, V_{IN} > 60mV
Output voltage low	V_{OL}	V_{CC}-1.712		V_{CC}-1.544	V	+25°C, V_{IN} < -60mV
		V_{CC}-1.792		V_{CC}-1.650	V	-40°C, V_{IN} < -60mV
		V_{CC}-1.638		V_{CC}-1.465	V	+85°C, V_{IN} < -60mV
Gain (transparent mode)			20		dB	Differential
Common mode rejection	CMRR	50	50		dB	+25°C, with respect to I/P
Supply voltage rejection	PSRR		70		dB	+25°C, with respect to I/P offset
Clock input:						
Common mode range	CMRC	V_{MM} + 2V		V_{CC}-1.35V	V	
Differential swing	DS	400		1600	mV	

NOTES 1 Guaranteed but not tested

Dynamic Characteristics (Note 1) See dynamic test circuit Fig.9.

Characteristic	Symbol	Value			Units	Condition
		Min.	Typ.	Max.		
Latch setup time	t_S		150		ps	20mV overdrive
Hold time	t_H		600		ps	20mV overdrive
Input to Q delay	t_{IQ}		800		ps	20mV overdrive
Latch to Q delay	t_{LQ}		1500		ps	20mV overdrive
Glitch capture regeneration	t_{RD}		900		ps	20mV overdrive at Qn
Propagation delay matching	t_{PDM}	-100		+100	ps	Within each device
Min. compare pulse width	t_{PW}		950		ps	20mV overdrive
Min. reset pulse width	t_{RM}		800		ps	
Max. flip flop reset time	t_{RR}		800		ps	
Min. hold time of Qn after reset	t_{GH}		800		ps	
Delay between Qn and Gn	t_{QG}		900		ps	
Propagation delay RES to Gn	t_{RG}		800		ps	

NOTES 1 Guaranteed but not tested

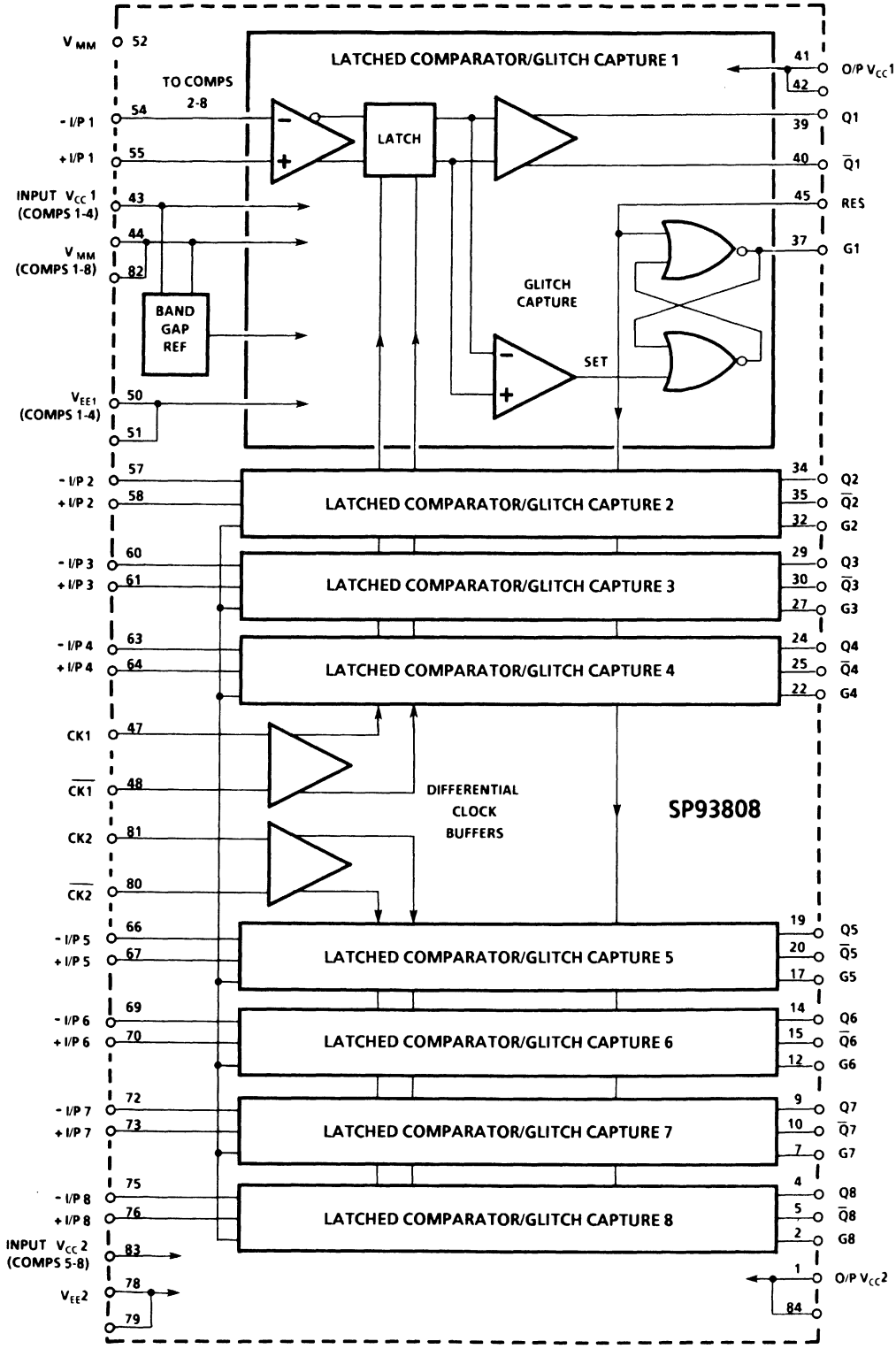


Fig.2 Internal block diagram (all comparators are as detailed for comparator 1)

PIN FUNCTIONS

Name	Pin	Description
I/P $V_{CC}1$	43	Positive supply connection for comparators 1 to 4, and the bandgap reference.
O/P $V_{CC}1$	41 & 42	Positive supply connection for the outputs Qn, $\overline{Q}$n and Gn of comparators 1 to 4 (emitter follower outputs, see Fig.5).
I/P $V_{CC}2$	83	Positive supply connection for comparators 5 to 8.
O/P $V_{CC}2$	1 & 84	Positive supply connection for the outputs Qn, $\overline{Q}$n and Gn of comparators 5 to 8 (emitter follower outputs, see Fig.5).
-I/Pn +I/Pn	54/55, 57/58, 60/61, 63/64, 66/67, 69/70, 72/73, 75/76	Inverting and non-inverting inputs to comparators 1 to 8, respectively.
Qn/$\overline{Q}$n	40/39, 35/34, 30/29, 25/24, 20/19, 15/14, 10/9, 5/4	Q and $\overline{Q}$ outputs of comparators 1 to 8, respectively.
Gn	37,32,27,22, 17,12,7,2	Outputs of glitch capture circuits 1 to 8, respectively.
RES	45	Reset pin for glitch capture circuit. This active high ECL signal will set the outputs (Gn) of the Glitch capture circuits to '0'.
CLK1, $\overline{CLK1}$	47,48	Clock input pins for comparators 1 to 4. ECL active low signal which latches the outputs of comparators 1 to 4.
CLK2, $\overline{CLK2}$	80,81	Clock input pins for comparators 5 to 8. ECL active low signal which latches the outputs of comparators 5 to 8.
$V_{EE}1$	50 & 51	Negative supply voltage for comparators 1 to 4.
$V_{EE}2$	78 & 79	Negative supply voltage for comparators 5 to 8.
V_{MM}	44,82,52	Mid-supply voltage rail for reset, clock drivers, glitch capture and band gap ref.

OPERATING NOTES

Transparent Mode

The SP93808 has been designed to maximise high input impedance and minimise propagation delay whilst maintaining a high gain.

While CLK is high ($\overline{CLK}$ low), the outputs of the comparators are unlatched and are therefore transparent, with a gain of typically 20dB. In this mode, for example, a 20mV input overdrive signal will result in a 200mV differential output.

For applications such as logic analyser probes etc. this output signal may then be passed along a transmission line to a second SP93808 to enable strobing at a remote point from the comparator. Thus the gain and delay has been distributed within the application. The net result is reduced overall propagation delay and reduced channel to channel time skew.

In the transparent mode of operation the glitch capture circuit is continuously active.

Latched Mode

The output of each comparator is strobed into a very high bandwidth latch by taking CLK low ($\overline{CLK}$ high). The latch will then regenerate and produce full ECL output levels. This method produces the minimum system propagation delay.

Supply Connections

The SP93808 operates from supply voltages of 0V, -5V and -10V (Fig.3) or ±5V (Fig.4). The choice of supply connections depends on the input voltage range required and also the input voltage of the following circuits. As the ECL outputs from this device are 0.8V down from V_{CC}, then to interface with other ECL circuits directly, supplies of 0V, -5V, -10V should be provided. This will give an input common mode range of -2.4V to -7.3V. Therefore when two devices are used in a system, the first (line driver) should have supplies as shown in Fig.3 and the second (line receiver) should have supplies as shown in Fig.4.

If it is inconvenient to provide the mid-supply voltage (V_{MM}), then a 5.1V Zener diode can be used. The current taken by this diode will be typically 32mA, see Fig.3.

Note that the O/P V_{CC} pins are connected to the collectors of the output emitter followers; load return currents should therefore be directed towards these device pins.

The supply connections shown in Fig.3 give output levels that are directly compatible with ECL 10k inputs. An optional 5.1V Zener diode is shown; this is only required if a -5V supply is not available.

The SP93808 ECL outputs can be connected directly to other ECL circuitry if these circuits are supplied from the +5V and 0V rails (O/PH, see Fig.4). Alternatively, a 5.1V Zener diode can be used to level shift the outputs for connection to standard ECL circuits supplied from the 0V and -5V rails.

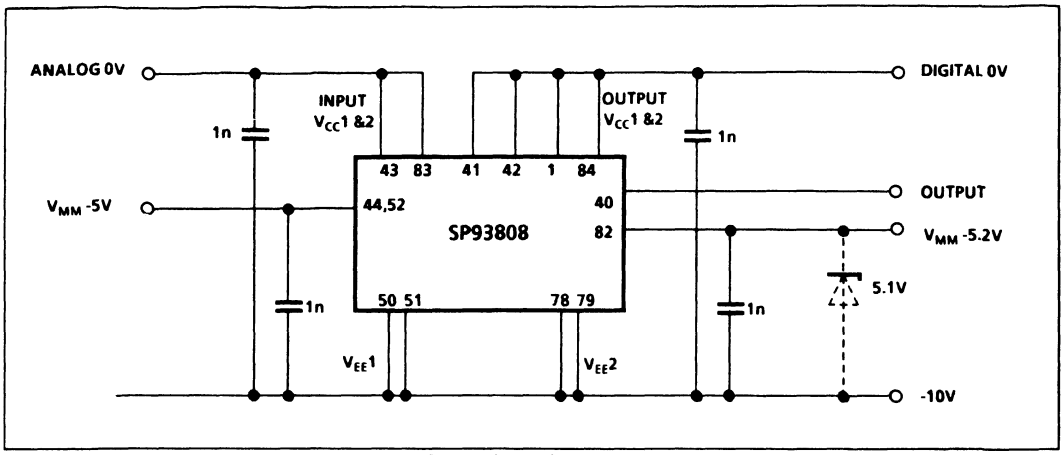


Fig.3 Connection to 0V, -5V and -10V

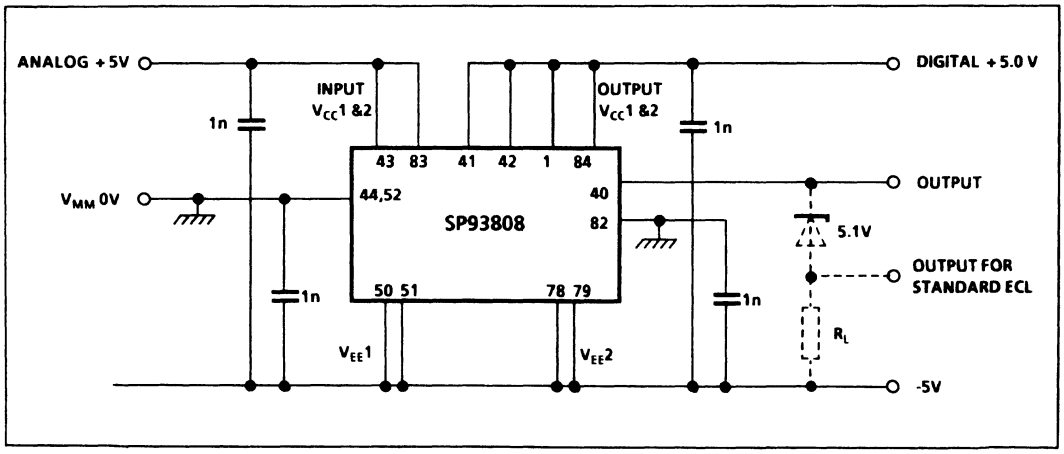


Fig.4 Connection to ±5V

External Components

The Qn, $\overline{Qn}$ and Gn outputs are open emitters and therefore required external pulldown resistors (R_L). These resistors may be in the range of 50-250Ω connected to V_{CC}-2V (V_T) or 250-2000Ω connected to V_{MM}.

Due to the sub-ns conversion speeds and edge speeds of this device, the performance is dependent on both board layout and component placement.

The performance of the comparator is enhanced by minimising the number of external components and minimising the external strays around the device. The use of high quality chip resistors is recommended, especially for loads.

Decoupling capacitors should be positioned close to the device supply pins. Decoupling between supplies and V_{EE} is also recommended.

The device has been packaged for maximum isolation between channels. This has been achieved by positioning an un-bonded (not internally connected) pin between each set of comparator inputs. These N/C pins can be connected to the ground plane, providing further isolation.

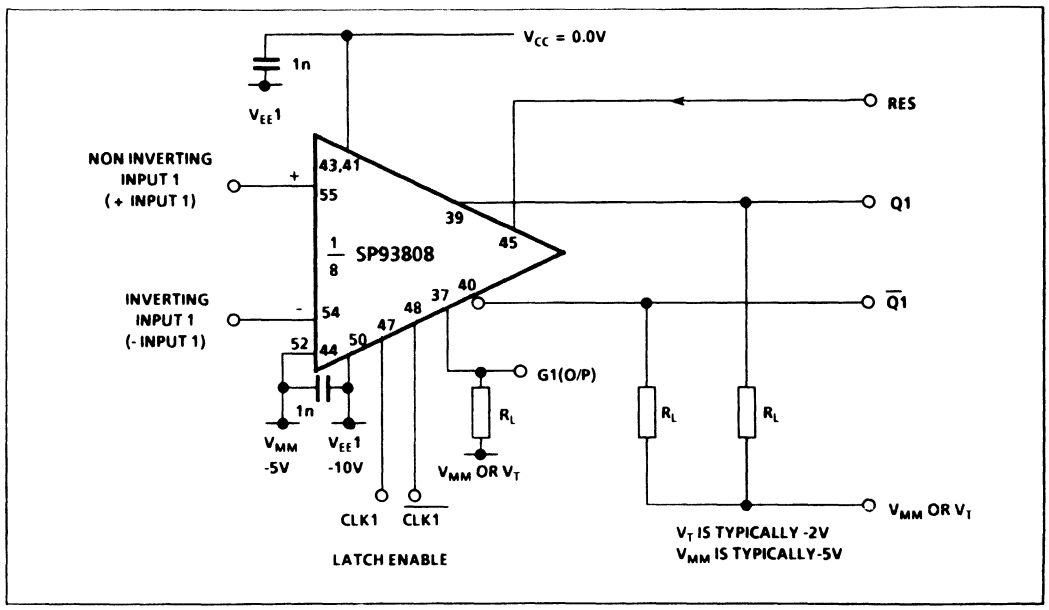


Fig.5 Applications circuit (one channel)

Clock Inputs

The SP93808 can be used in transparent mode by connecting the CLK input to ECL '1' and the $\overline{CLK}$ input to an ECL '0'. The device can also be used as a dual quad comparator as comparators 1 to 4 can be clocked separately from comparators 5 to 8.

As the device contains two clock input buffers, a range of clock input configurations are possible. With the device V_{CC} connected to 0V the clock inputs will accept standard differential ECL signals. However optimum performance in terms of crosstalk will be achieved with a differential input of 400mV p-p.

CLK1 (pin 47) comparators 1 to 4 latch when low.
$\overline{CLK1}$ (pin 48) inverse clock for comparators 1 to 4.
CLK2 (pin 81) comparators 5 to 8 latch when low.
$\overline{CLK2}$ (pin 80) inverse clock for comparators 5 to 8.

The clock inputs should have fast rise times and low jitter. The Plessey SP92701 line receiver can be used to clean up the clock signal and provide a good differential ECL drive for this comparator.

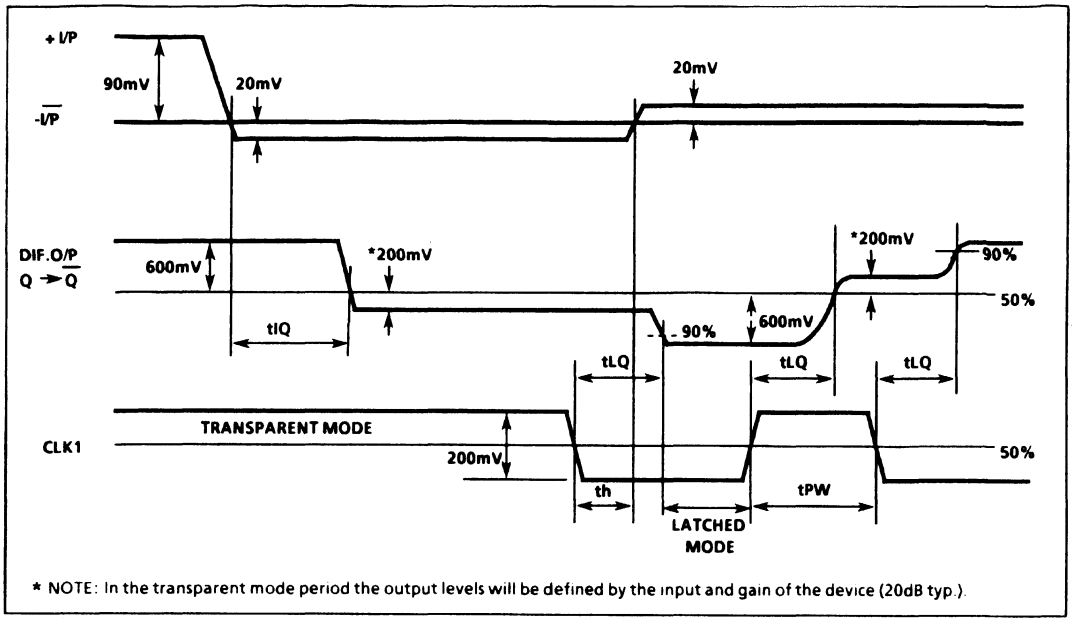


Fig.6 Comparator timing diagram

I/P	CLK	Qn + 1
X	0	Qn
1	1	1
0	1	0

X = Don't Care

Table 1 Truth table for comparator

Glitch Capture Circuit

This advanced feature enables the device to capture sub-nanosecond glitches that may have occurred before the comparator is latched.

The glitch capture circuit (see Fig.2) can be reset at any time by the RES input. When held at ECL '1' (V_{CC}-0.8V) the RES pin will reset the Gn output to '0' (ECL low). Glitch capture is active when the RES pin is taken low.

If Qn goes positive by more than 20mV for a time $>t_{RD}$ then the Gn output will be set to an ECL '1', it will remain in this state until the RES pin is again taken high.

RES	SET(1) (n + 1)	Gn + 1
1	X	0
0	↗	↗
0	↘	1
0	1	1
0	0	Gn(2)
↘	1	↗
↘	0	0

X = Don't Care

Table 2 Truth table for glitch capture circuit

NOTES
1. SET is the input to the glitch capture circuit and is logically the same as the Q output from the comparator, see Fig.8.
2. Gn = 1 is evidence that a transition has occurred at the Q output since the last falling edge of the reset pulse.

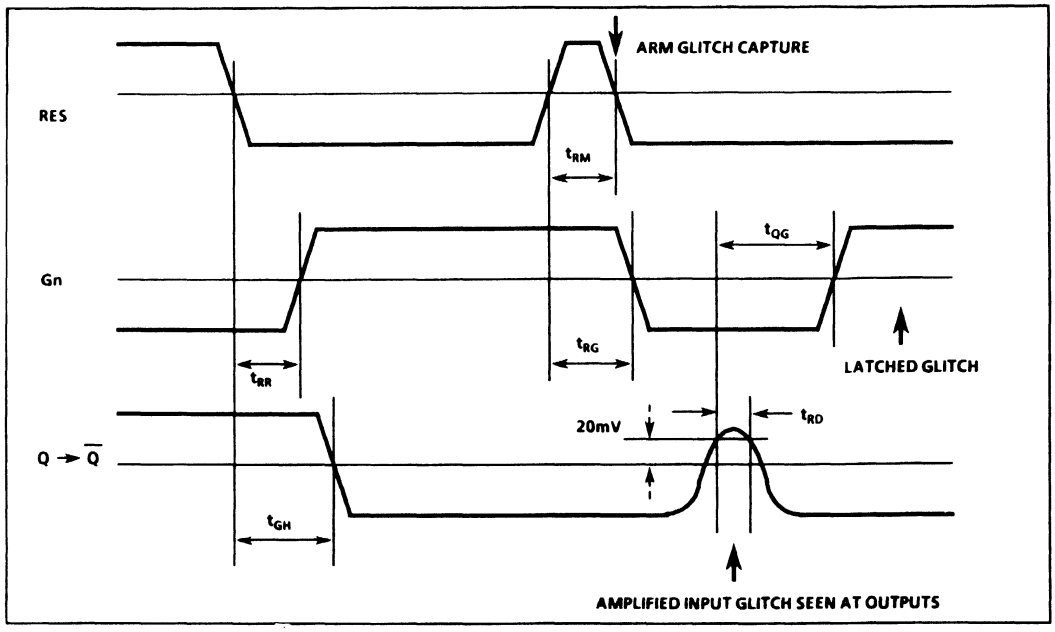
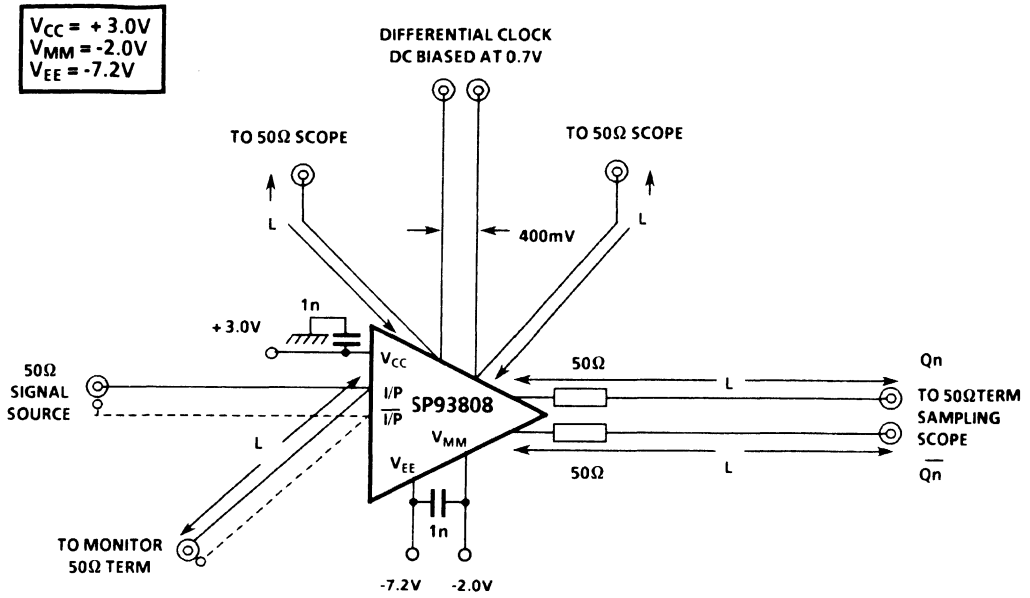


Fig.7 Glitch capture circuit timing



NOTES:-

The supplies have been chosen to allow direct connection of both the outputs and monitor points to measurement instruments with 50Ω input impedance.

1) Lead lengths should be as short as possible and also of equal length. (equal delay).
2) Decoupling should be close to the device (chip type if possible).
3) Use coaxial cables or stripline techniques in board construction.
4) Monitor and both scope channel 50Ω loads must be in circuit for correct termination.
5) A Plessey SP92701 can be used with supplies of +3V and -2V, to drive the clock input. The outputs of the SP92701 should have series 100Ω resistors to reduce the differential swing.

Fig.8 Comparator dynamic test circuit (one channel)

PLESSEY
Semiconductors

SP94308

8-BIT VIDEO SYSTEM ADC

The Plessey SP94308 analog to digital converter has been specially designed for use with NTSC or PAL video signals.

A 1V video signal is AC coupled to the device input, where it is DC clamped, amplified by two and fed through a buffer which drives the ADC input capacitance.

A sync or burst gate pulse can be used to drive the DC clamp circuit. This circuit can be externally adjusted to provide conversion of video only or video and sync.

This analog to digital converter samples the input waveform on the rising edge of the clock and produces a latched output which can be acquired simply by an inverted clock signal.

Also within the SP94308 is an internal clock amplifier and driver. This allows a low level clock signal to be AC coupled directly into the device for applications that may be sensitive to clock radiation.

The clock frequency and analog bandwidth of the SP94308 are compatible with both PAL and NTSC standards where conversion of luma or full composite video signals are required.

FEATURES

- 8 Bits, 20MHz
- ±0.75 LSB Differential Linearity (Typ.)
- No Sample and Hold or Input Buffer Required
- Internal Clock Amplifier
- Internal Clamp Circuit
- Internal Output Latch
- 6MHz Min. Analog Bandwidth
- Output Levels are TTL/CMOS Compatible
- 0°C to 70°C Temperature Range
- Full Static Protection
- On Chip ×2 Amplifier and ADC Buffer

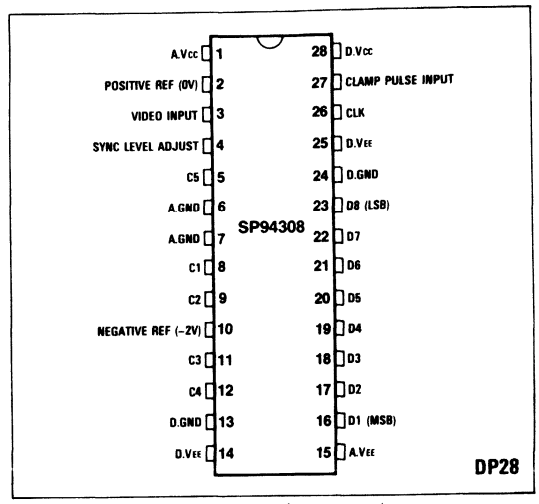


Fig.1 Pin connections - top view

ORDERING INFORMATION

SP94308C DP (Commercial - Plastic DIL package)

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}-V_{EE}	<12V
Output current	<20mA
Storage temperature	-65°C to +150°C
Junction operating temperature	<150°C

THERMAL INFORMATION

Chip to ambient temperature θ_{JA} = 55°C/W

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 0°C to 70°C, V_{CC} = +5V ± 0.25V, V_{EE} = -5.2V ± 0.25V

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Positive supply current	I_{CC}		35	44	mA	
Negative supply current	I_{EE}		110	150	mA	
Power consumption			750		mW	
Resolution		8			Bits	
Reference current	I_{ref}		12	16	mA	V_{ref} = -2V
Maximum clock rate	f_C	20			MHz	
Clock input level		0.25		1.0	V p-p	AC coupled
Analog bandwidth	f_a	6			MHz	Note 3
Input impedance	R_{IN}	100K			Ω	
Differential linearity			±0.75	±1.0	LSB	25°C
Integral linearity				±1.0	LSB	25°C
Differential gain				1.5	%	f_C = 20.0MHz
Differential phase			1		Deg	
Logic '1'	V_{IH}	V_{CC}-1.3	V_{CC}-1		V	I_{source} = 1mA
	V_{IH}	V_{CC}-1.1	V_{CC}-0.9		V	I_{source} = 0.1mA
Logic '0'	V_{OL}		0.3	0.4	V	I_{sink} = 1.6mA (Note 2)
Tilt/line			-1.5		mV	100nF input capacitor
Input level			1		V p-p	AC coupled
Sync level adjust output			-1.4		V	Unadjusted (Note 1)
Data valid time	t_V		45		ns	At 20MHz clock

NOTES
1. Gain of x2 in input stage.
2. See Fig.7 for equivalent TTL load.
3. Guaranteed but not tested.

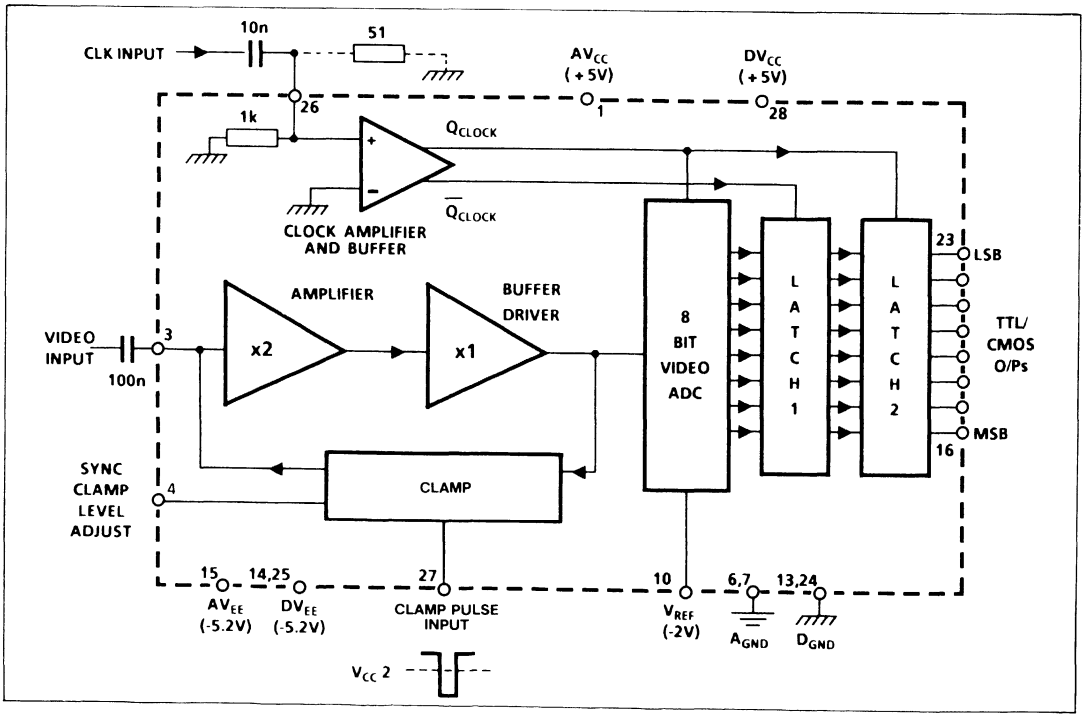


Fig.2 Internal block diagram

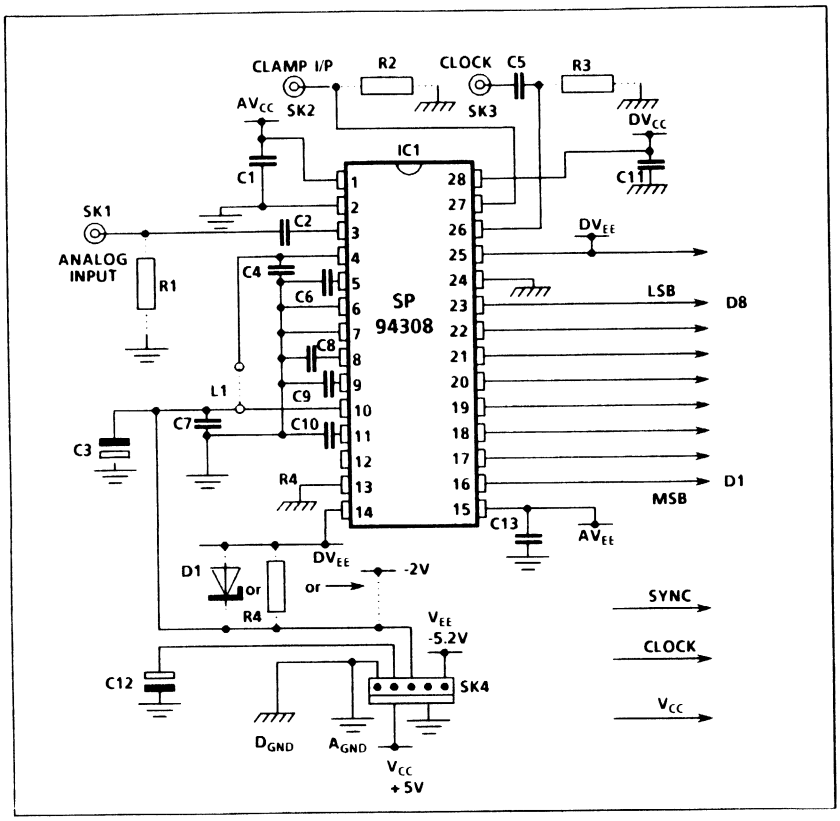


Fig.3 Minimum component application circuit

COMPONENT LIST FOR FIG.4

Resistors

R1	75Ω (optional termination)
R2	47Ω (optional termination)
R3	47Ω (optional termination)
R4	Approx. 560Ω (optional)

Semiconductors

IC1	SP94308
D1	BZX79C3V0 (optional)

Sockets

S1-S3	Sub Vis sockets (optional)
S4	KK Molex socket (optional)

Capacitors for ADC, clamp, bias etc.

C1	100nF (optional decoupling)
C2	100nF (input coupling and line clamp)
C3	47μF (electrolytic decoupling)
C4	100nF (optional decoupling)
C5	100nF (coupling)
C6	27pF at 20MHz or 47pF at 10MHz clock
C7	100nF (decoupling)
C8	100nF (decoupling)
C9	100nF (decoupling)
C10	100nF (decoupling)
C11	100nF (optional decoupling)
C12	47μF (electrolytic decoupling)
C13	100nF (optional decoupling)

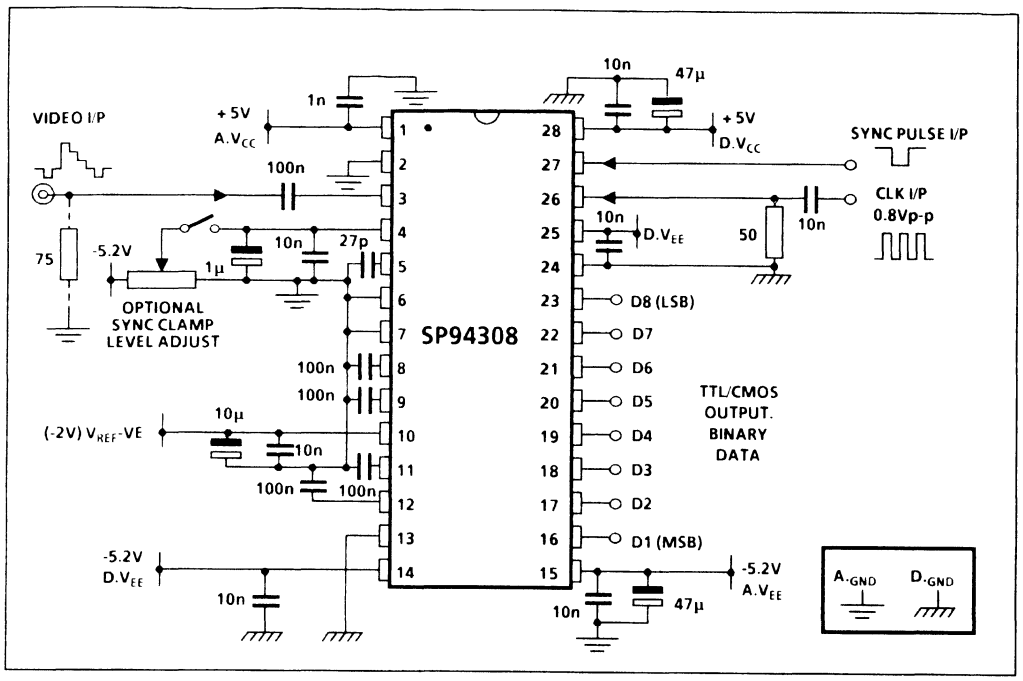


Fig.4 Full test circuit

APPLICATIONS

The SP94308 combines a clamp circuit, sample and hold, x2 amplifier, ADC driver, video ADC and output latch that form a conventional 8-bit video digitising system.

An on-chip clock amplifier allows the device to be clocked from low level sine or square wave signals. This reduces the possibility of patterning due to crosstalk.

The device offers the flexibility for either sync clamping or black level clamping of the video signal.

Sync Clamp

Sync clamping is provided by applying a negative going clamp pulse to pin 27 during the sync period. This pulse should be more than 1.5μs wide and it should cross the internal switching threshold of $V_{CC}/2$. Pin 4 should be connected to V_{REF} (pin 10 -2V) to allow the total video with its sync to be digitised.

Black Level Clamping

This can be achieved by applying a negative clamp pulse to pin 27 within the back porch of the video signal. The clamp pulse should avoid the colour burst - this ensures no attenuation of the burst signal.

The clamping pulse can be derived from a burst gate pulse or by delaying the sync pulse with a dual monostable (SN74123N).

When using a back porch clamping pulse, pin 4 should be decoupled to analog ground using a 100nF capacitor. The device will then self-bias this pin to -1.4V. This provides full digitisation of the video and its sync.

It is also possible to adjust the voltage on pin 4 and reduce the reference voltage pin 10 to provide digitisation of the active video information only.

If a clamp pulse is not readily available within the application it can be generated from the incoming video signal (see circuit shown in Fig.5). The variable resistor RV can be adjusted for different slice levels of the incoming video sync.

The digital outputs of the SP94308 are latched and have a 90% of CLK, data valid time at 20MHz. This allows the 8-Bit TTL output to be acquired simply by an inverse CLK signal. See Fig.6.

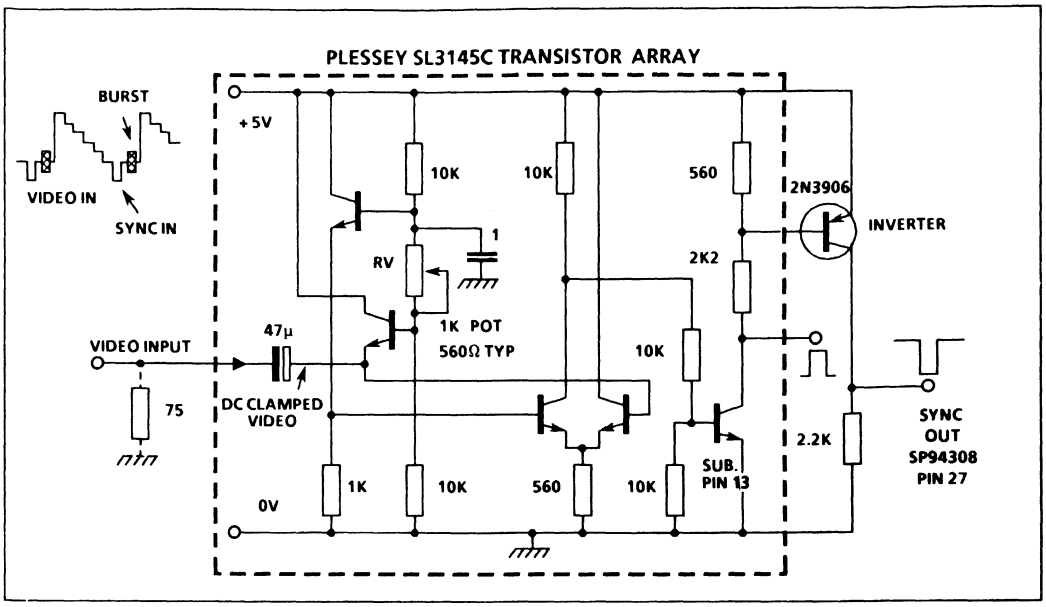


Fig.5 Sync pulse generation for test/evaluation circuit

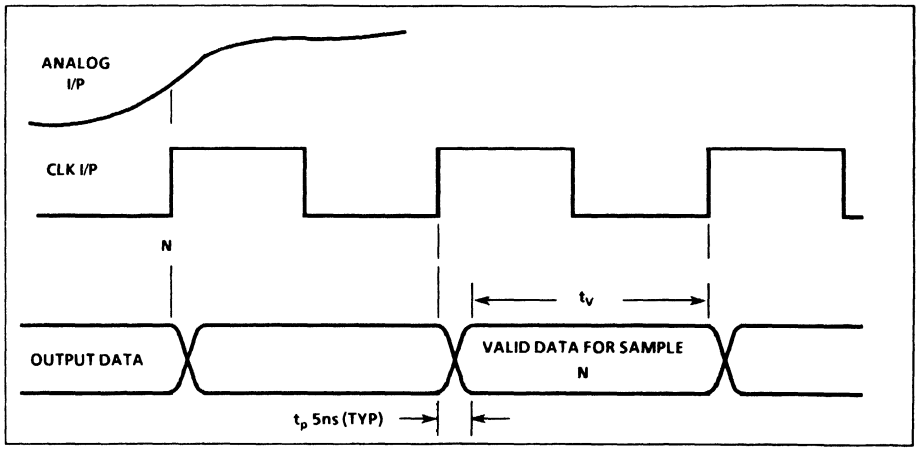


Fig.6 Timing diagram

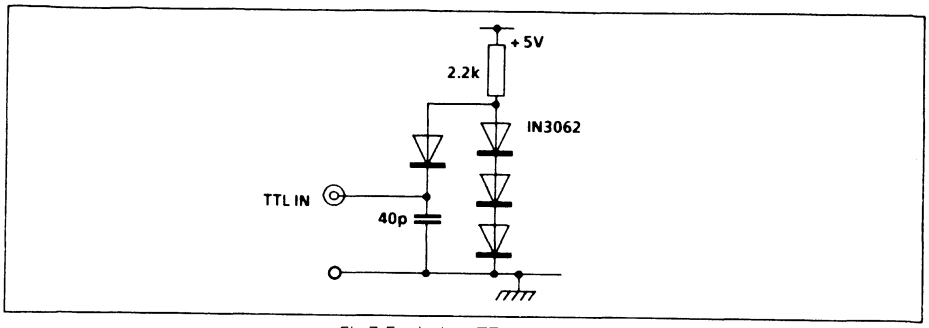


Fig.7 Equivalent TTL test load

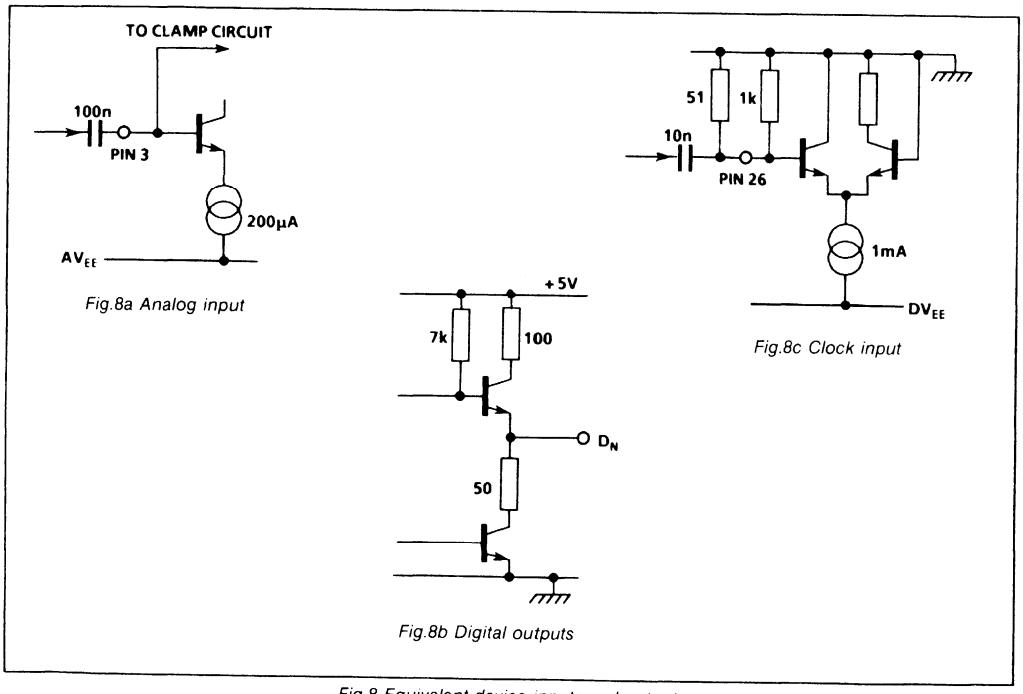


Fig.8a Analog input

Fig.8b Digital outputs

Fig.8c Clock input

Fig.8 Equivalent device inputs and outputs.

PLESSEY
Semiconductors

SP973E8

30MHz ECL 8-BIT FLASH ADC

(SUPERSEDES AUGUST 1987 EDITION)

The Plessey SP973E8 contains 255 high speed comparators which form a full flash analog to digital converter that requires no preceding sample and hold.

Its wideband input allows signals with frequencies up to the Nyquist limit to be digitised with high accuracy. An internal bandgap voltage reference gives low DC drift over a wide operating temperature range (−40°C to +85°C in DG package).

Also within the device is a full 8-bit D-type latch, which ensures that the 8 ECL outputs are accurately registered and have a good data valid time at high clock speeds. The output data can therefore be acquired with ease. The SP973E8 is available in two variants: the SP973E8 has ±½ LSB differential linearity and the SP973E8 C has ±1 LSB differential linearity, with a consequent cost advantage.

The ADC is designed for applications where power consumption is at a premium (520mW typ).

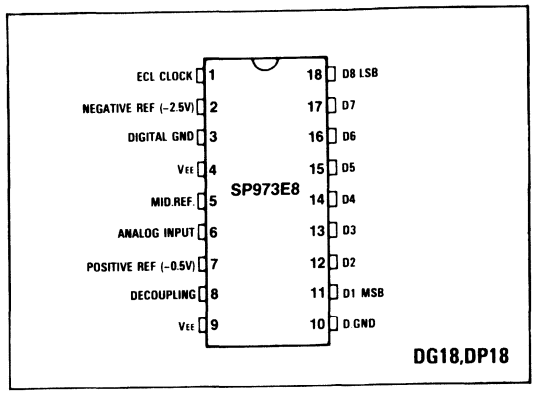


Fig.1 Pin connections - top view

ORDERING INFORMATION

SP973E8 B DG (Industrial - Ceramic DIL package)
SP973E8 C DP (Commercial - Plastic DIL package)

FEATURES

- Wideband Analog Input 70MHz (Typ.)
- Flash Converter, No Sample and Hold Required
- Low Power Consumption (520mW Typ.)
- Latched ECL Compatible Outputs
- Band Gap for Good Temperature Stability
- Wide Operating Temperature Range
- Static Protection on all Digital Inputs and Outputs
- No Missing Codes

APPLICATIONS

- Studio Quality Video
- DBS Broadcast Video
- High Resolution TV
- Nucleonics
- Radar
- Computing

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{EE}	12V
Output current	10mA
Input voltage	V_{EE}
Storage temperature	−55°C to +175°C
Operating temperature	<150°C

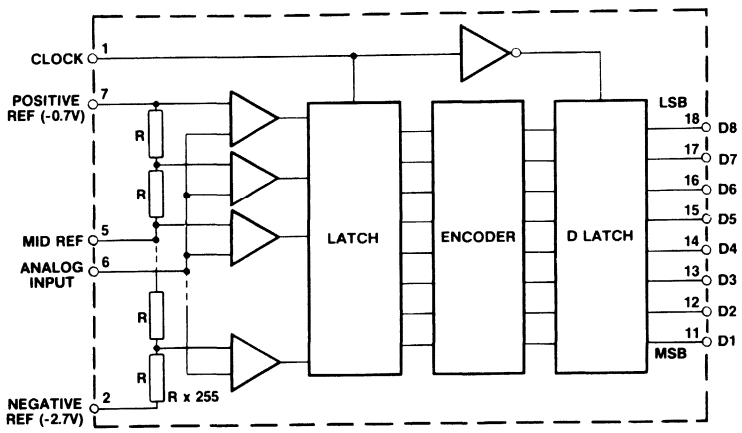


Fig.2 Internal block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to 70°C, V_{EE} = -5.2V ± 0.25V

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	I_{EE}		100		mA	
Power consumption			520	650	mW	
Clock frequency	f_C	30			MHz	ECL
Digital output level high	V_H	-0.96		-0.81	V	1K load, 25°C
Digital output level low	V_L	-1.85		-1.62	V	1K load, 25°C
Reference chain resistance	Rr		390		Ω	
Analog input range	V_{IN}	-2.7		-0.7	V	
Analog input capacitance	C_{IN}		40		pF	
Differential linearity				±0.5	LSB	SP973E8 B (DG package)
Integral linearity				±1.0	LSB	SP973E8 B (DG package)
Differential linearity				±1.0	LSB	SP973E8 C (DG package)
Integral linearity				±1.0	LSB	SP973E8 C (DG package)
Data valid time	t_V	40	45		ns	20MHz clock
Clock to output propagation delay	t_{pd}			8	ns	After ½ cycle delay
Differential gain				1	%	
Differential phase				1	Deg	

THERMAL CHARACTERISTICS

SP973E8 B θ_{JA} = 92°C/W
θ_{JC} = 21°C/W
SP973E8 C θ_{JA} = 75°C/W
θ_{JC} = 20°C/W

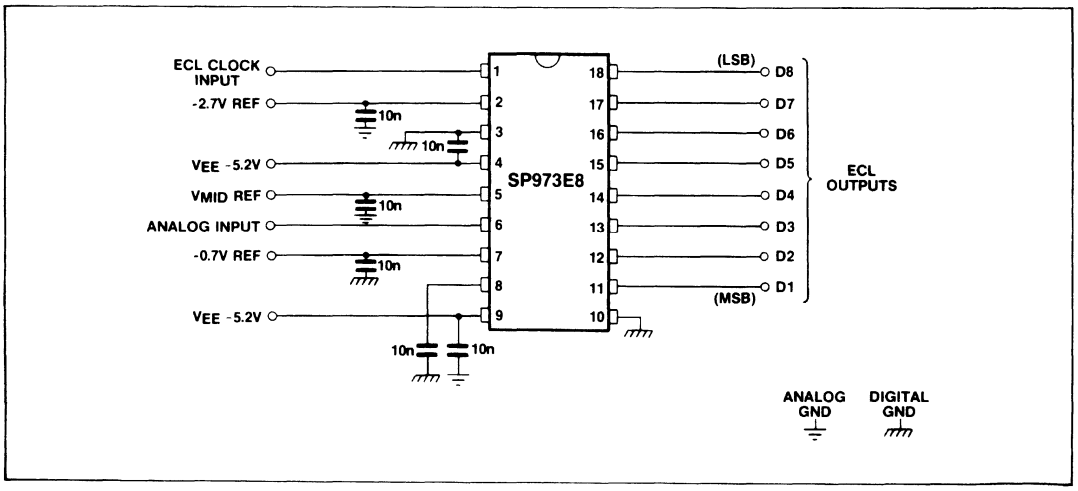


Fig.3 Test/applications circuit

OPERATING NOTES

The SP973E8 ADC will operate at clock frequencies up to and above 30MHz. It is therefore necessary to take care with the ground plane and component placement around the device.

Split analog and digital grounds with good decoupling close to the device pins, will reduce digital to analog crosstalk and hence aid performance. The voltage between A_{GND} and D_{GND} should not be >±50mV.

The optimum differential linearity is achieved using the widest possible reference voltage. Therefore standard applications should use -0.7V on pin 7 and -2.7V on pin 2.

The optimum input signal for use with these recommended reference voltages is 2V p-p biased at -1.7V.

For optimum performance the tolerance on the reference inputs is ±0.1V and on the supplies the tolerance is ±0.25V.

The Plessey SL9999 is a suitable op-amp/ADC driver to provide this offset and drive the SP973E8 input at high speed.

The digital outputs can drive 100Ω loads to -2V (or Thevenin equivalent).

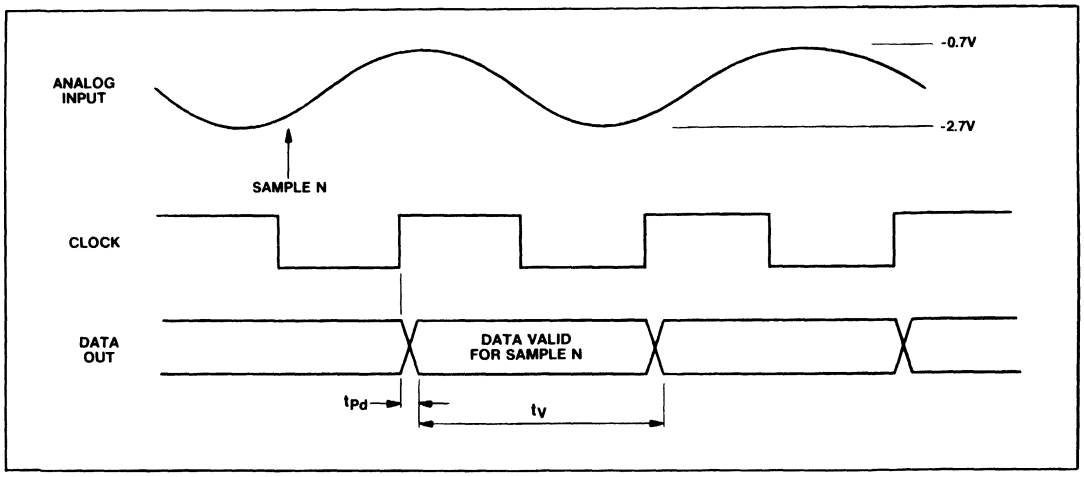


Fig.4 Timing diagram

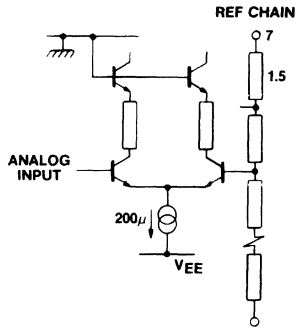


Fig.5a One of 255 analog inputs connected to pin 8

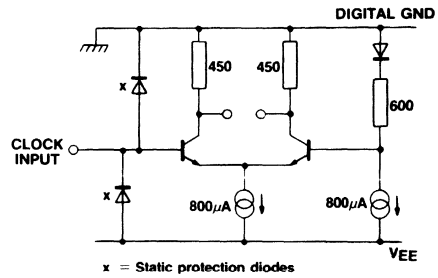


Fig.5b Clock input

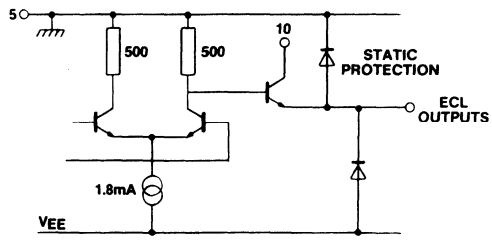


Fig.5c Digital outputs

Fig.5 Input/output internal circuits

SP973T8

30MHz TTL/CMOS 8-BIT FLASH ADC

The Plessey SP973T8 contains 255 high speed comparators which form a full flash analog to digital converter that requires no preceding sample and hold.

Its wideband input allows signals with frequencies up to the Nyquist limit to be digitised with high accuracy. An internal bandgap voltage reference gives low DC drift over a wide operating temperature range (-40°C to +85°C in DG package).

The device also contains a full 8-bit D-type latch, which ensures that the 8 TTL/CMOS outputs are accurately registered and have a good data valid time at high clock speeds.

The SP973T8 is available in two variants: the SP973T8 B has ±½ LSB differential linearity and the SP973T8 C has ±1 LSB differential linearity, with a consequent cost advantage.

The ADC is designed for applications where power consumption is at a premium (550mW typ).

ORDERING INFORMATION

SP973T8 B DG (Industrial - Ceramic DIL package)
SP973T8 C DP (Commercial - Plastic DIL package)

FEATURES

- Wideband Analog Input: 70MHz 3dB (Typ.)
- Flash Converter, No Sample and Hold Required
- Low Power Consumption (550mW Typ.)
- Latched TTL/CMOS Compatible Outputs
- Band Gap for Good Temperature Stability
- Wide Operating Temperature Range
- Static Protection on all Digital Inputs and Outputs
- Designed for Wideband Application
- Single 5V Supply
- No Missing Codes

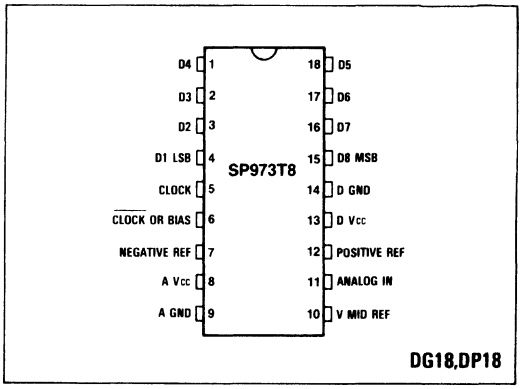


Fig.1 Pin connections - top view

APPLICATIONS

- Studio Quality Video
- DBS Broadcast Video
- High Resolution TV
- Nucleonics
- Radar
- Computing

ABSOLUTE MAXIMUM RATINGS

Supply voltage Vcc	12V
Output current	10mA
Input voltage	Vcc
Storage temperature	-55°C to +175°C
Operating temperature	<150°C

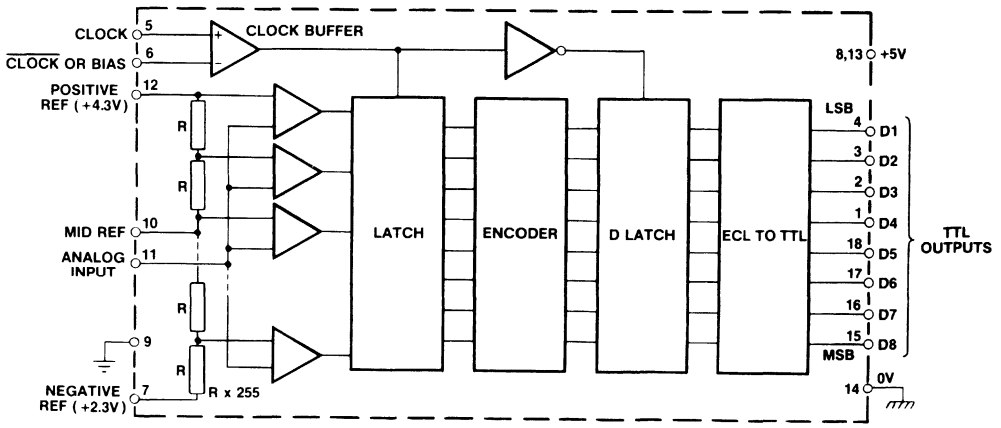


Fig.2 Internal block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to 70°C, V_{CC} = +5V ± 0.25V,

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Positive supply current	I_{CC}		95		mA	
Power consumption			550	700	mW	
Clock frequency	fc	30			MHz	
Digital output level high	V_H	3.5	4.3		V	One TTL load. Fig.5
Digital output level low	V_L		0.3	0.4	V	One TTL load. Fig.5
Reference chain resistance	Rr		390		Ω	
Analog input range	V_{IN}	2.3		4.3	V	
Analog input capacitance	C_{IN}		40		pF	
Differential linearity				±0.5	LSB	SP973T8 B (DG package)
Integral linearity				±1.0	LSB	SP973T8 B (DG package)
Differential linearity				±1.0	LSB	SP973T8 C (DP package)
Integral linearity				±1.0	LSB	SP973T8 C (DP package)
Data valid time	tv	40	45		ns	20MHz clock
Clock to output propagation delay	t_{pd}			10	ns	After 1 cycle delay
Differential gain				1	%	
Differential phase				1	Deg	
3dB bandwidth			80		MHz	

THERMAL CHARACTERISTICS

SP973T8 B θ_{JA} = 92°C/W
θ_{JC} = 21°C/W
SP973T8 C θ_{JA} = 75°C/W
θ_{JC} = 20°C/W

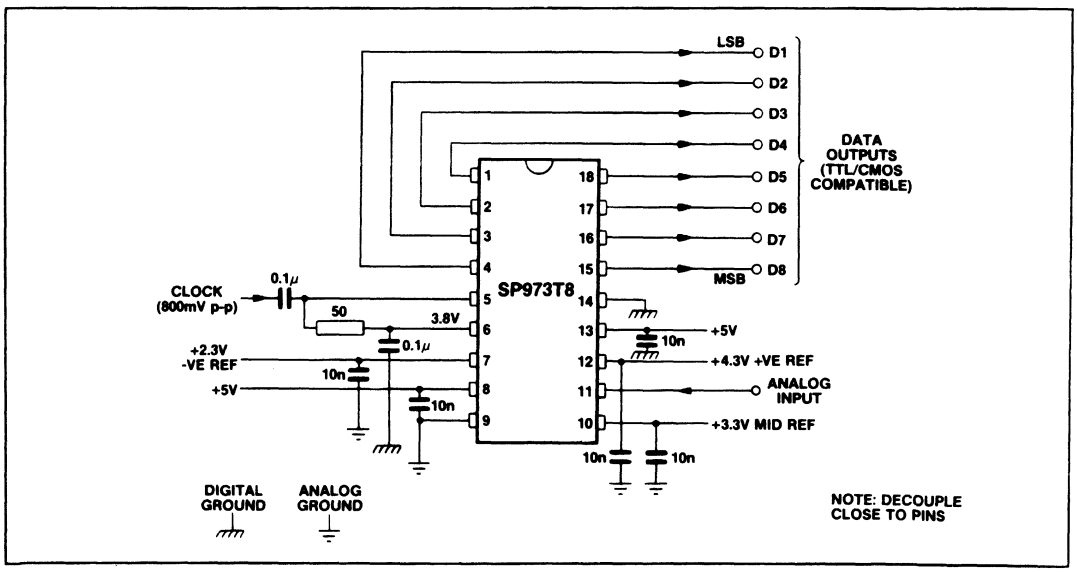


Fig.3 Test/applications circuit

OPERATING NOTES

The SP973T8 ADC will operate at clock frequencies up to and above 30MHz. It is therefore necessary to take care with the ground plane and component placement around the device.

Split analog and digital grounds with good decoupling close to the device pins, will reduce digital to analog crosstalk and hence aid performance.

The optimum differential linearity is achieved using the widest possible reference voltage. Therefore standard applications should use +4.3V positive reference and +2.3V negative reference.

The optimum input signal for use with these recommended reference voltages is 2V p-p biased at +3.3V.

The Plessey SL9999 is a suitable op-amp/ADC driver to provide this offset and drive the SP973T8 input at high speed.

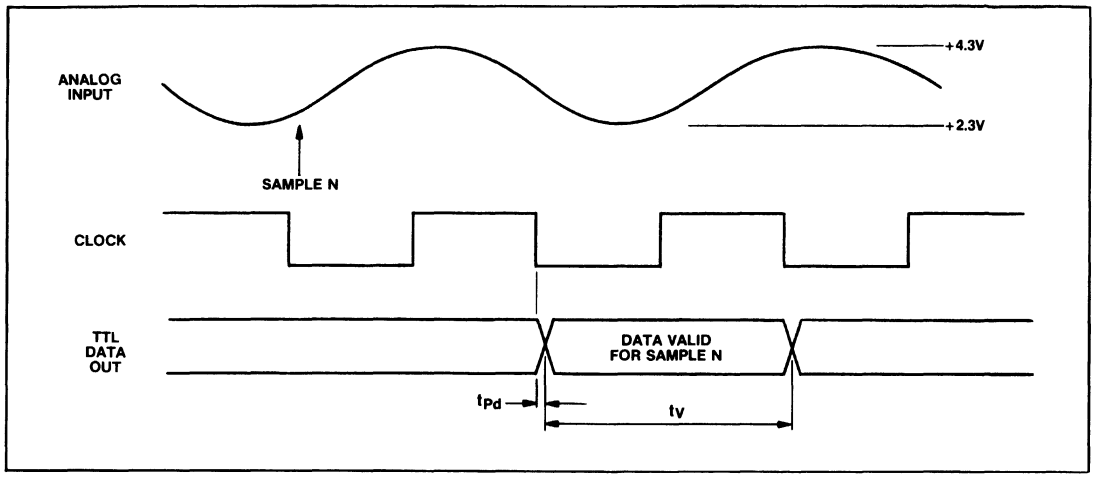


Fig.4 Timing diagram

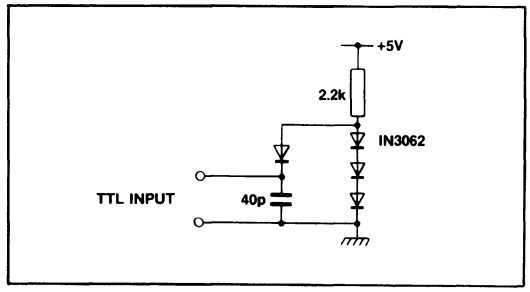


Fig.5 Standard TTL test load

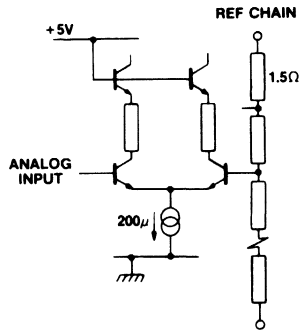


Fig.6a One of 255 analog inputs connected to pin 8

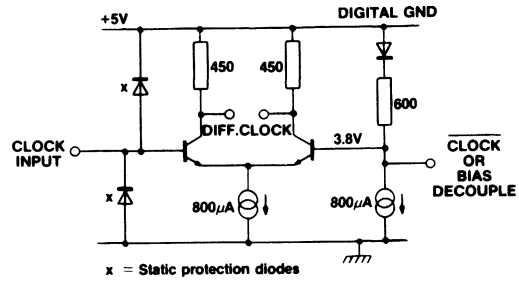


Fig.6b Clock input

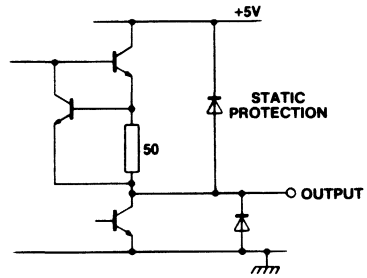


Fig.6c TTL output stage

Fig.6 Internal circuits

PLESSEY
Semiconductors

SP97504

HIGH SPEED FOUR BIT EXPANDABLE A TO D CONVERTER

(SUPERSEDES SP9754, DIRECT PIN REPLACEMENT)

The SP97504 is a fast 4-bit ECL A-D converter, expandable up to 8 bits without additional encoding circuitry.

Designed to maintain high accuracy at high analog input frequencies, the SP97504 is a pin for pin replacement for the industry standard SP9754.

It can convert at sample rates from DC to 110MHz, with analog inputs above Nyquist frequencies. All output levels are ECL compatible.

The latch function to the device provides on-chip sampling which allows the converter to operate without an external sample and hold. Data is clocked through the device in master/slave fashion, ensuring that all outputs are synchronous.

The SP97504 operates from a +5V, -7V supply.

FEATURES

- Operating Temperature Range -30°C to +85°C
- No External Components for 4-Bit Conversion
- 110MHz Conversion Rate
- On-Chip Encoding for Expansion to 8 Bits
- No External Sample and Hold Needed
- Bit Size 10-100mV
- Over 100MHz Full Power Bandwidth
- 10ps Aperture Uncertainty Time
- 8-Bit Accuracy (When Expanded)

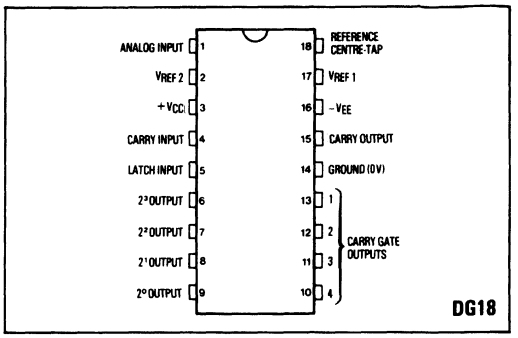


Fig.1 Pin connections (top view)

ABSOLUTE MAXIMUM RATINGS

Positive supply voltage	+5.5V
Negative supply voltage	-7.5V
Storage temperature range	-65°C to +150°C
Junction operating temperature	<175°C
Lead temperature (soldering 60 sec)	300°C

ORDERING INFORMATION

SP97504 DG (Industrial - Ceramic DIL package)

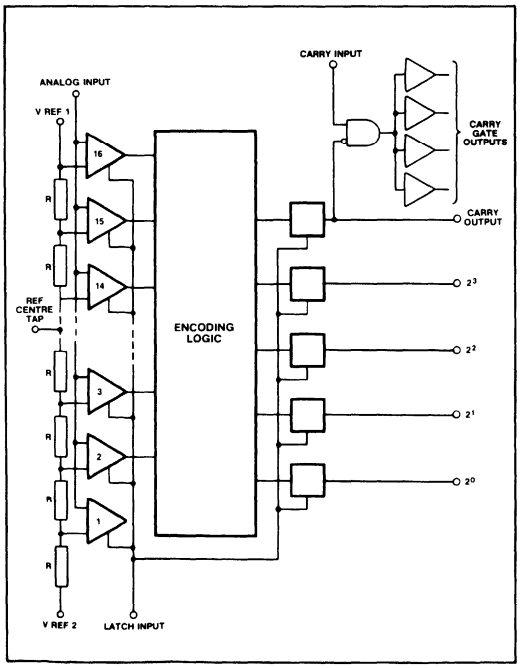


Fig.2 Functional diagram

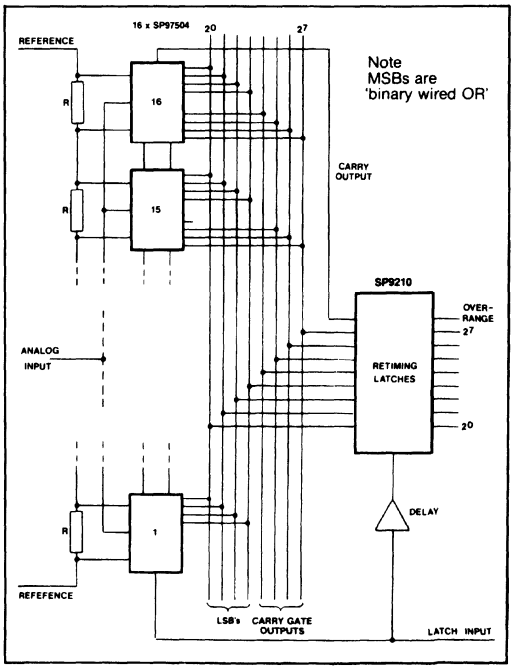


Fig.3 8-bit all-parallel system

ELECTRICAL CHARACTERISTICS

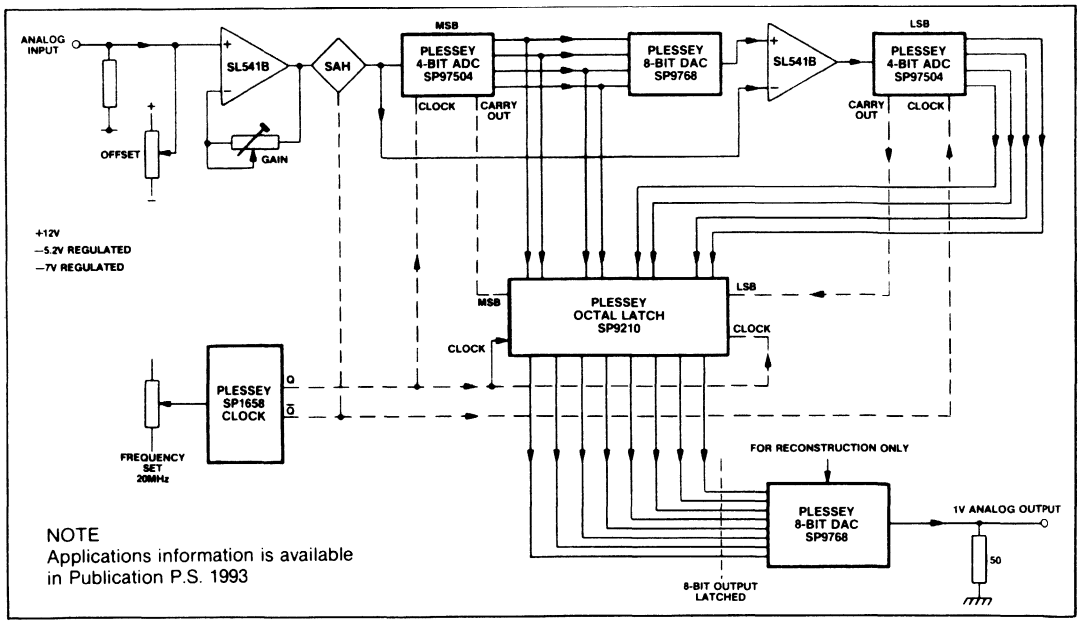
Test conditions (unless otherwise stated):
T_{amb} = 25°C, V_{CC} = +5V ± 0.25V, V_{EE} = -7V ± 0.25V, R_L = 100Ω to -2V

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Analog input current	I_B		30	100	μA	V_{IN} = 0V
Analog input capacitance	C_{IN}		10		pF	
Common mode range	V_{CM}	-2		+2	V	
Maximum input slew rate			1000		V/μs	
Latch input capacitance	C_{IN}		2		pF	
Positive supply current	I_{CC}		72*	92*	mA	
Negative supply current	I_{EE}		75*	96*	mA	
Reference resistor chain			25		Ω	Total
Reference bit size		10		100	mV	
Comparator offset voltage	V_{OS}			-5	mV	
Total power dissipation	P_{DISS}		935*	1230*	mW	All outputs loaded
Input and output logic levels						
Logic high	V_{OH}	-0.930		-0.720	V	For 100Ω load
Logic low	V_{OL}	-1.90		-1.620	V	to -2V
Minimum latch set-up time	ts		1.5	2	ns	10mV overdrive
Data uncertain			5		ns	<1mV overdrive
Latch to output propagation delay						
Latch enable to output high	t_{pd} + (E)		6*	8	ns	10mV overdrive
Latch enable to output low	t_{pd} - (E)		5	8	ns	
Carry input to carry gate	t_{pd} (C)		3	5	ns	
O/P delay						
Maximum sample rate	$F_{C\,max}$	100	110		MHz	
Aperture uncertainty time	ta		10		ps	

* Values differ from SP9754

THERMAL CHARACTERISTICS

θ_{JA} 90°C/W*
θ_{JC} 20°C/W*



NOTE
Applications information is available in Publication P.S. 1993

PERFORMANCE CURVES

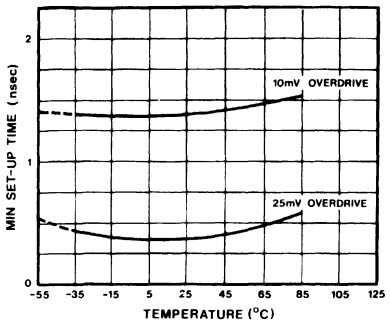


Fig.5 Set-up time as a function of temperature

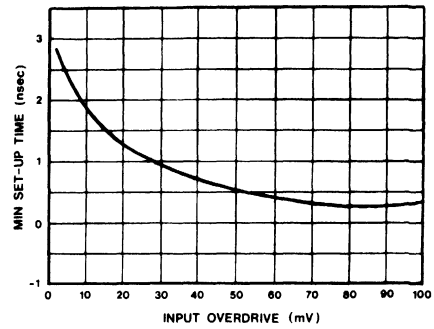


Fig.6 Set-up time as a function of overdrive

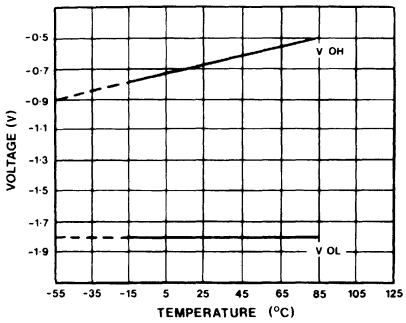


Fig.7 Output logic levels as a function of temperature

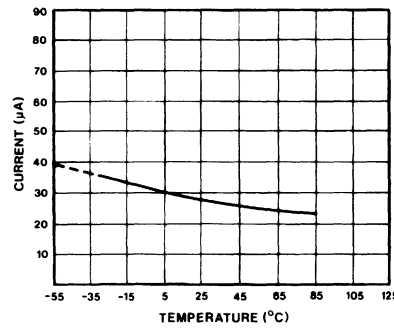


Fig.8 Analog input current as a function of temperature

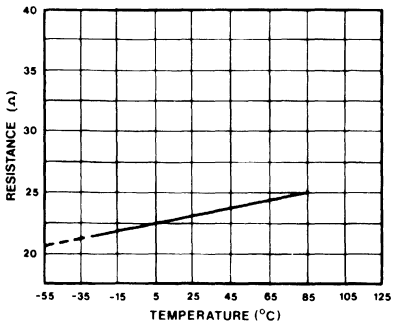


Fig.9 Network resistance as a function of temperature

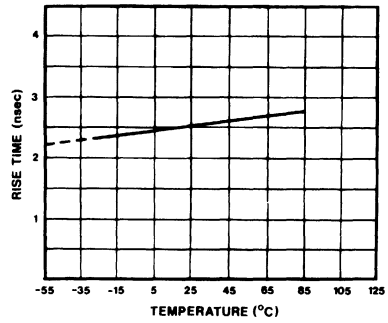


Fig.10 MSB output edge speeds as a function of temperature

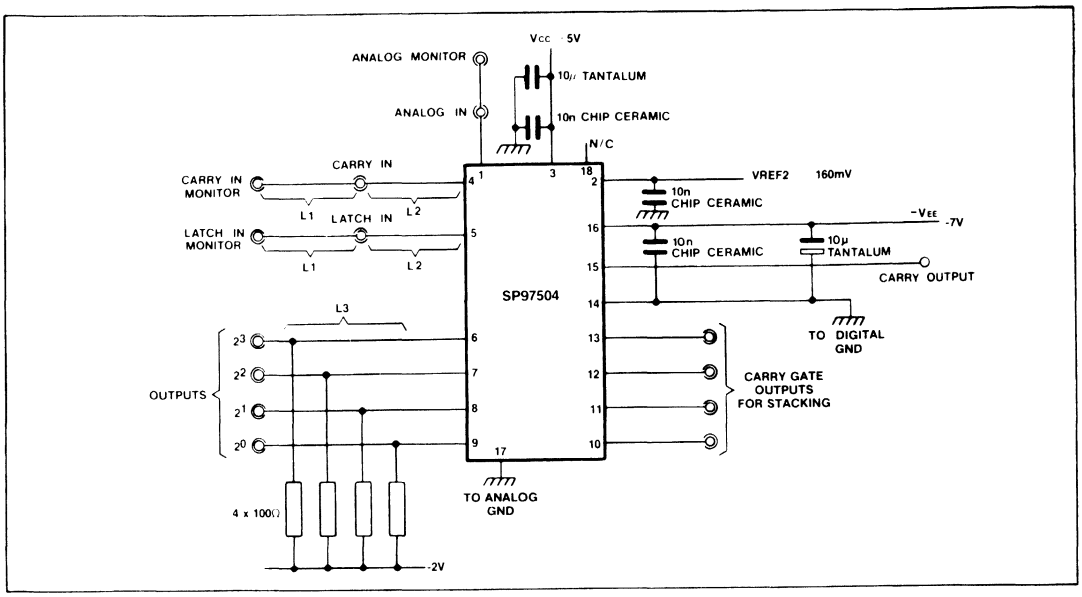


Fig.11 High frequency test circuit

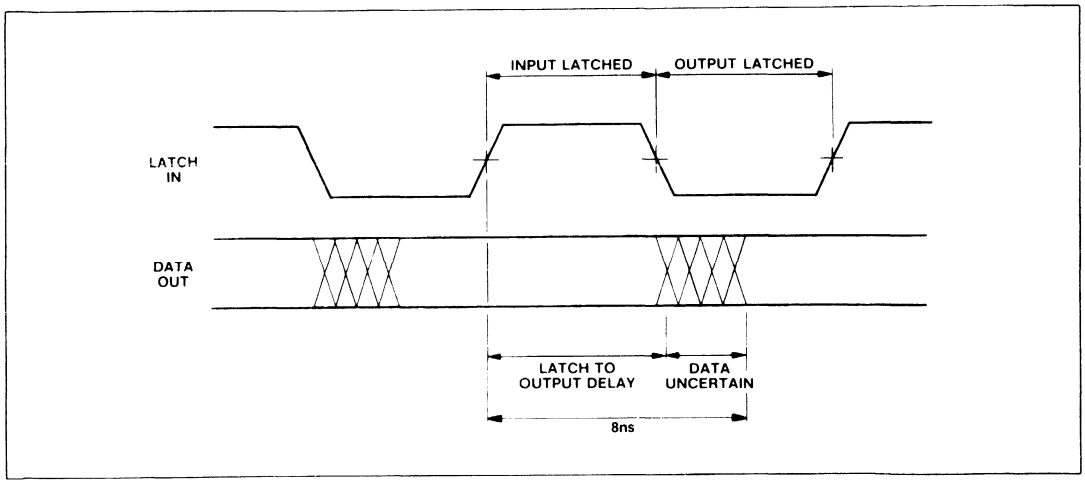


Fig.12 Timing diagram

OPERATING NOTES

1. Carry output (pin 15) is high when the analog input exceeds the top reference voltage (pin 17).

Then the carry gate outputs (pins 10 to 13) go low regardless of carry input (pin 4), when the analog input is between V_{REF} and V_{REF2} and the carry output is low. The carry gate output will be high if the carry input is also high. Similarly if the carry input is low then the carry gate outputs will be low.

2. When used in an ambient temperature in excess of 65 °C the SP97504 must be provided with an external heatsink or forced air cooling. This will ensure that the junction temperature does not exceed 175 °C.

APPLICATION NOTES

1. The SP97504 is ideally suited to subranging systems as it maintains good accuracy at low reference voltages. This enables the second rank to be driven at higher speed from the subtracting Op-Amp.
2. For applications that require low bit error rates at high frequency, the clock signal should be adjusted for 60% ECL low, 40% ECL high mark to space ratio.
3. The SP97504 is ideally suited to applications in communication systems that incorporate multi-level coding (quadrature amplitude modulation).
4. The SP97504 requires a fast edge speed clock. Rise and fall times of ≤4ns are recommended.

SP97508

8-BIT HIGH SPEED ADC

(SUPERSEDES AUGUST 1987 DATABOOK EDITION)

The Plessey SP97508 is an 8-bit flash ECL analog-to-digital converter. It incorporates 255 individual comparators, a reference chain and a full D-type output latch. The ADC is capable of sampling in excess of 110MHz with full (Nyquist) analog bandwidth and has excellent dynamic performance. A conventional unity mark space ratio clock can be used and the output data can be programmed for true or inverse binary and 2s complement coding.

FEATURES

- Pin Replacement for CX20116 — But Faster
- 110MHz Conversion Rate
- Full Scale Input Bandwidth. 120MHz (-3dB)
- Production Tested with 30MHz Analog Input
- Input Capacitance. 40pF
- No External Sample and Hold Needed
- Low Power Consumption: 1.2W (typ.)
- True/Inverse Binary and Twos Complement Coding
- Operating Temperature Range: -40°C to +85°C
- Unity Mark Space Ratio Clock

APPLICATIONS

- Radar Video Digitising
- Instrumentation
- Nucleonics
- Studio Quality Video

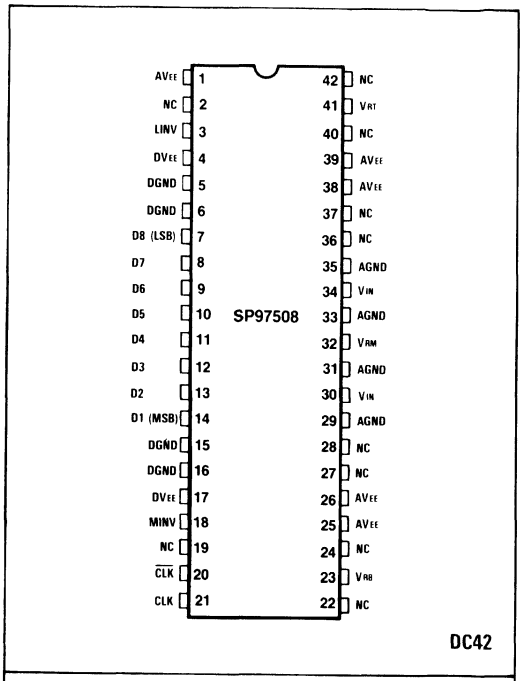
ORDERING INFORMATION

SP97508 B DC (Industrial - sidebrazed DILMON package)
SP97508B HG (Industrial - J-Lead Quad Cerpac)

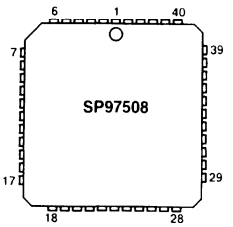
Under Development
SP97508 AC DC (Military - Sidebrazed DILMON package)
SP97508 AC HG (Military - J-Lead Quad Cerpac)

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25°C)

Power Supply V_{EE}	0 to -7V
Analog Input V_{IN}	+0.5 to V_{EE}
Reference Voltages V_{RT}, V_{RM}, V_{RB}	+0.5 to V_{EE}
Reference Range | V_{RT} - V_{RB} |	2.5V
Digital Inputs CLK, $\overline{CLK}$, MINV, LINV	0.5 to -4V
Mid Ref Input Current I_{VRM}	-10 to +10mA
Digital Output Current I_D	0 to -20mA
Voltage between Grounds AGND to DGND	-50 to +50mV
Voltage between Supplies AV_{EE} to DV_{EE}	-50 to +50mV



DC42



HG44

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	NC	12	D4	23	CLK	34	V_{RM}
2	LINV	13	D3	24	NC	35	AGND
3	NC	14	D2	25	V_{RB}	36	V_{IN}
4	DV_{EE}	15	D1 MSB	26	AV_{EE}	37	AGND
5	DGND	16	DGND	27	AV_{EE}	38	NC
6	DGND	17	DGND	28	NC	39	NC
7	NC	18	NC	29	NC	40	NC
8	D8 LSB	19	DV_{EE}	30	NC	41	AV_{EE}
9	D7	20	MINV	31	AGND	42	AV_{EE}
10	D6	21	$\overline{NC}$	32	V_{IN}	43	NC
11	D5	22	$\overline{CLK}$	33	AGND	44	V_{RT}

Fig.1 Pin connections - top view

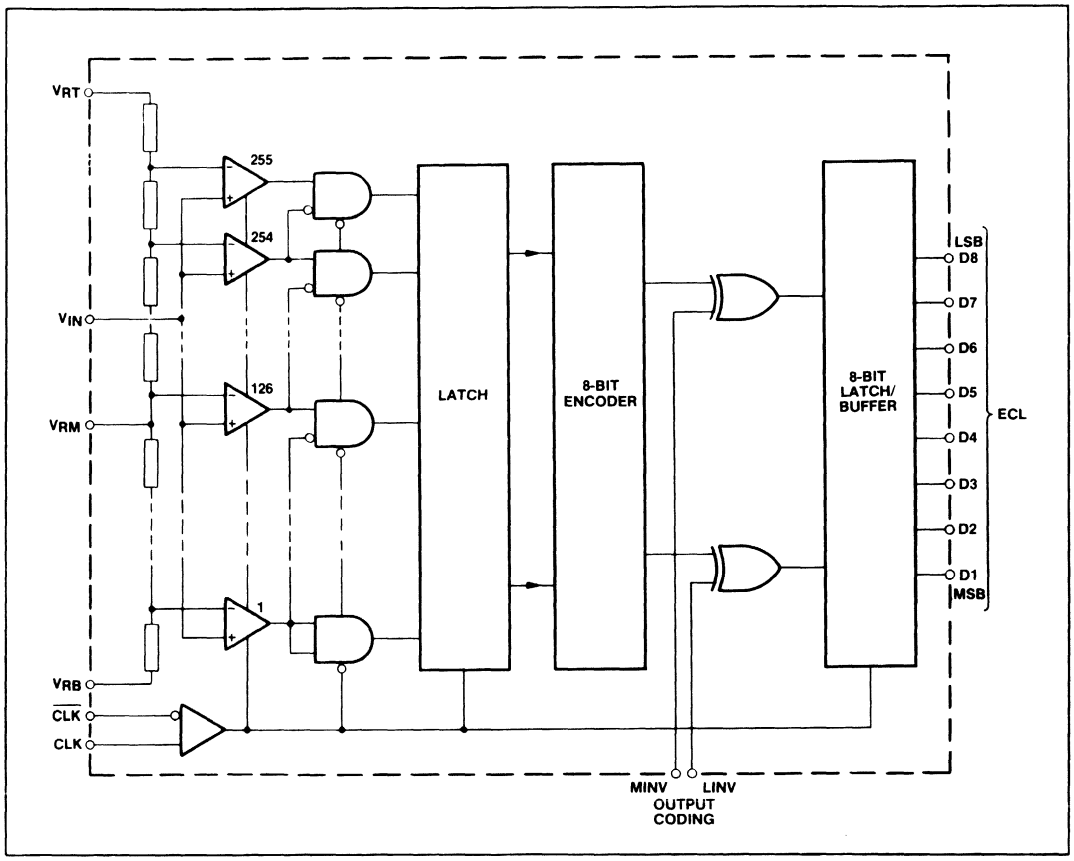


Fig.2 SP97508 functional block diagram

PIN DESCRIPTION

Symbol	Function
AV_{EE}	Analog V_{EE}, -5.2V (typ).
LINV	Input pin for output polarity invertion of data (see Table 1).
DV_{EE}	Digital V_{EE}, -5.2V (typ).
DGND	Digital GND, which is separated from the Analog GND.
D1 - D8	Digital data output pins, ECL level. D1 = MSB. D8 = LSB. Pull-down resistors are necessary externally (typically 620Ω).
MINV	Input pin for output polarity inversion of D1 (MSB) (see Table 1). ECL level. '0' is held when it is open circuit.
$\overline{CLK}$	Inverse clock input pin, ECL level.
CLK	Clock input pin, ECL level. Analog aquired on rising edge.
V_{RB}	Reference voltage (bottom) -2V (typ).
AGND	Analog GND.
V_{IN}	Analog input, input range is (V_{RT} - V_{RB}) p-p.
V_{RM}	Middle point of the reference voltage, it can be used for linearity adjustment.
V_{RT}	Reference voltage (top), 0V (typ).
NC	Empty pins (Not Connected). 2 and 19 should be grounded to DGND, the others should be grounded to AGND.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25° C, V_{EE} = -5.2V, V_{RT} = 0V, V_{RB} = -2V

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Maximum conversion rate	fc	110			MHz	V_{IN} = 0 to -2V,fin = 1kHz, ramp
Analog conversion bandwidth			50		MHz	No missing codes
Supply current	I_{EE}	-180	-245	-300	mA	
Analog input capacitance	C_{IN}		35		pF	V_{IN} = -1V + 0.07V rms
Analog input bias current	I_{IN}		150	400	μA	V_{IN} = -1V
Reference resistor (see Note 1)	R_r		105		Ω	
Offset voltage at ends of the	V_{RT}		9		mV	
reference cabinet	V_{RB}		17		mV	
Digital input voltage	V_{IH}	-1.0	-0.9	-0.7	V	
	V_{IL}	-1.9	-1.75	-1.6	V	
Digital input current	I_{IH}	0		0.4	mA	V_{IH} = -0.9V
	I_{IL}	-0.05		0.35	mA	V_{IL} = -1.75V
Digital output voltage	V_{OH}	-1.0			V	R_L = 620Ω to V_{EE}
	V_{OL}			-1.6	V	
Output data delay	Td		2.5		ns	R_L = 620Ω to V_{EE}
Integral linearity error (DC)			±0.5		LSB	fc = 100MHz V_{IN} = 0 to -2V, fin = 48.8kHz sine
Differential linearity (DC)				Note 2		fc = 100MHz,fin = 48.8kHz sine
Differential gain	DG		1.5		%	NTSC 40 IRE mod. ramp
Differential phase	DP		0.5		deg.	fc = 100MHz
Aperture jitter			30		ps	

NOTES
1. R_r is the total resistance from V_{RT} to V_{RB}.
2. Not more than 7 codes outside ±0.5 LSB; no codes in excess of 0.75 LSB.

THERMAL CHARACTERISTICS

Storage Temperature Range	-65°C to +150°C
Maximum Junction Operating Temperature	+175°C
Lead Temperature (Soldering 60 seconds)	300°C
θ_{JA}	40°C/W
θ_{JC}	10°C/W

RECOMMENDED OPERATING CONDITIONS

Supply Voltage		-5.2V ± 0.25V
Reference (V_{RT})		0V ± 0.1V
Reference (V_{RB})		-2.0V ± 0.2V
AV_{EE} to DV_{EE}		0mV ± 50mV
AGND to DGND		0mV ± 50mV
Analog Input		2V p-p max.
Clock ECL High	tpw1 = 6.8ns	for lowest BER
Clock ECL Low	tpw0 = 2.3ns	
Output Load		680Ω to -5.2V

APPLICATION NOTES

Analog Input (Figs. 4 and 9)

The maximum amplitude and offset of the input is defined by the reference voltages (V_{RB} to V_{RT}). The optimum input is 2V p-p with a DC offset of -1V.

Input buffering internal to the device results in an input capacitance of 35pF (typ). Gain, offset and low impedance drive can all be provided by the use of a high slew rate ADC driver such as the Plessey SL9999.

Reference Pins (Figs. 8 and 9)

Between pin 41 (V_{RT}) and pin 23 (V_{RB}) there are 256 series resistors forming the reference chain. The total resistance may be between 90 and 120Ω. A mid reference pin 32 (V_{RM}) is also provided as an option for precision setting of integral linearity. Both V_{RM} and V_{RB} should be adequately decoupled to the analog GND. For optimum performance V_{RT} is connected directly to analog GND and V_{RB} is driven from a -2V DC supply. For precise reference setting this supply should be adjustable by ±0.2V.

Clock Inputs CLK and $\overline{CLK}$ (Figs.3 and 5)

The Plessey SP97508 can be driven from both differential or single ended ECL clocks. In either mode the clock lines should be terminated with the lines characteristic impedance, close to the device clock pins. Clock signals can be improved by incorporating the Plessey SP92701 line receiver into the circuit, between the clock source and the SP97508.

Single ended drive can be simply provided by adding a 1nF chip or encapsulated chip capacitor from the $\overline{CLK}$ pin to DGND. The $\overline{CLK}$ pin will then self bias at -1.28V which is the mid threshold for ECL. The device can therefore be clocked by an ECL signal into the CLK input.

For full 100MHz operation a conventional unity mark space ratio clock can be used. The device will give optimum performance with ECL CLK input high for 7.5ns and low for 2.5ns.

8-Bit ECL Outputs (Figs. 7 and 9)

The outputs are standard ECL open emitters and therefore require pull-down resistors from the outputs to -5.2V or -2V digital supply. Single in-line resistors of value 500 to 1kΩ are recommended. The outputs are capable of driving 100Ω terminations to a -2V supply. For 50Ω applications the Plessey SP9210 can be incorporated.

Output Coding (Table 1)

With pin 18 (MINV) and pin 3 (LINV) left open circuit, the device output will be coded in standard binary with the all 1s code corresponding to the most positive input. $V_{IN} = V_{RT} =$ 0V. An inverse binary output can be provided by connecting both MINV and LINV to GND. 2s complement coding (inverted MSB) can be provided by connecting only the MINV pin to GND and inverse 2s complement coding can be achieved by connecting only the LINV pin to GND.

Timing (Fig.3)

The anlog input is acquired by the device shortly after the rising edge of the CLK signal. The internal latch causes a 1 cycle delay, hence the output data is valid one clock cycle after the acquisition of the analog signal.

The output data is further delayed by the CLK to output delay (T_d = 2.5ns typ). This gives the advantage that the same timing and phase of the SP97508 CLK signal can be used to acquire the output data.

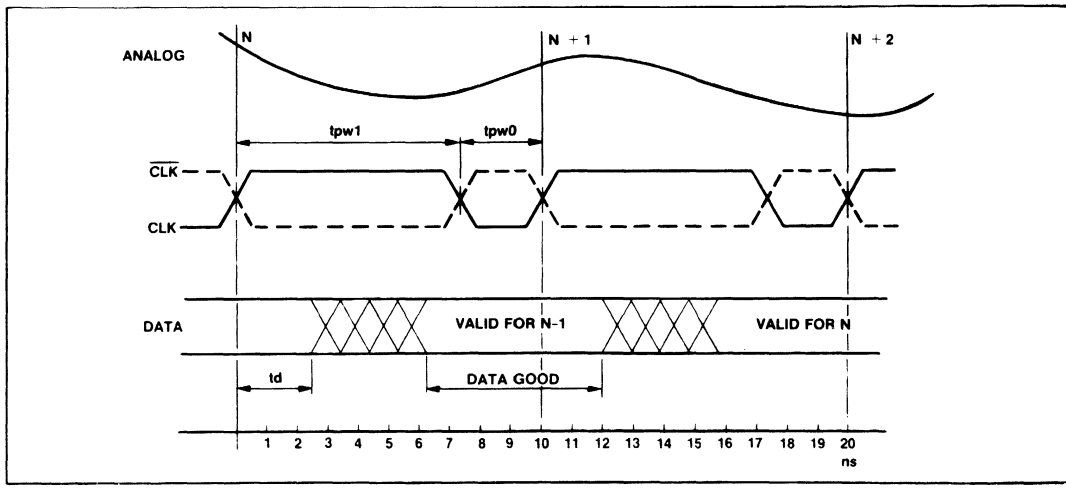


Fig.3 Optimum timing at 100MHz (typ)

		Binary	Inv '2s' Comp.	'2s' Comp.	Inv Binary
	MINV = LINV =	OPEN (0) OPEN (0)	OPEN (0) GND (1)	GND (1) OPEN (0)	GND (1) GND (1)
V_{IN}	0V	111 11	100 00	011 11	000 00
		111 10	100 01	011 10	000 01
		-	-	-	-
		-	-	-	-
		-	-	-	-
		100 00	111 11	000 00	011 11
		011 11	000 00	111 11	100 00
		-	-	-	-
		-	-	-	-
		-	-	-	-
		000 01	011 10	100 01	111 10
	-2V	000 00	011 11	100 00	111 11

Table 1

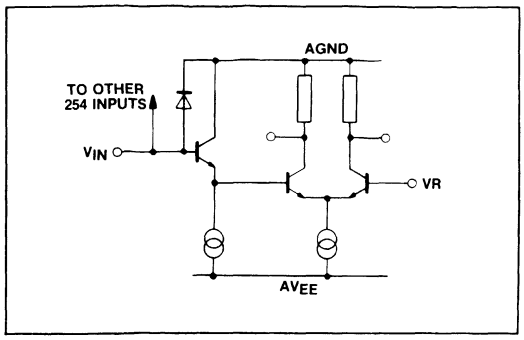


Fig.4 Analog input

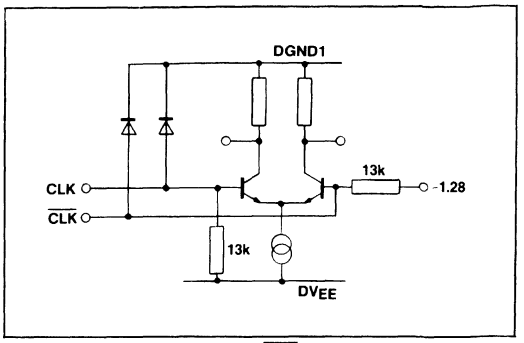


Fig.5 CLK, $\overline{CLK}$ input

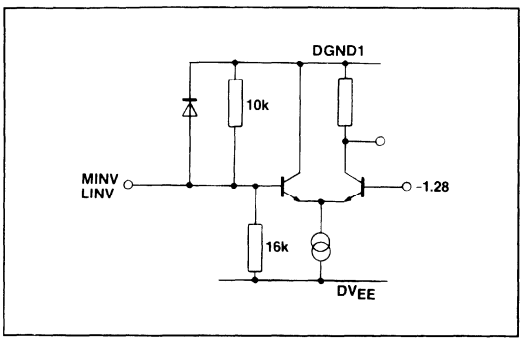


Fig.6 MINV, LINV input

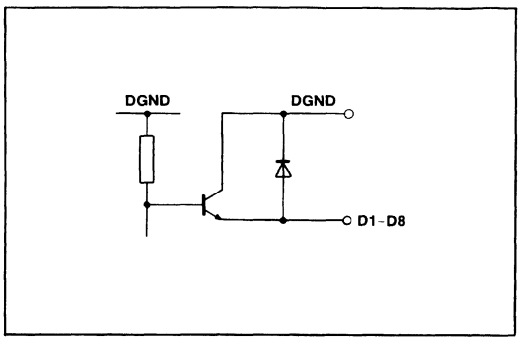


Fig.7 Digital output

CIRCUIT BOARD CONSTRUCTION

As with most PCB construction for analog-to-digital conversion, the best performance from the SP97508 can be achieved by separating the ground plane into two sections, analog GND, and digital GND. This aids the device performance by reducing the amount of digital switching noise fed back into the analog section of the converter.

The digital noise is produced mainly by the ECL binary outputs, which ideally should be terminated through a 680Ω load to the -5.2V digital supply, DV_{EE}.

The device supplies are also a source of digital feedback, as they can be modulated by the digital output current. Therefore it is wise to decouple the SP97508 close to the device supply pins with good quality high frequency capacitors.

Notes on Construction

1. Use split analog and digital ground planes connected together close to the device. Do not run the analog input next to the clock or data lines.
2. All NC pins must be grounded: connect pins 2 and 19 to DGND, all others to AGND.
3. Connect both digital and analog supplies together on the PCB at a point away from the device.
4. Use 10nF capacitors for supply decoupling.
5. Use strip-line techniques for signal paths greater than 5cm (2 inches).
6. Use a 47μF electrolytic capacitor to decouple the -5.2V V_{EE} supply.

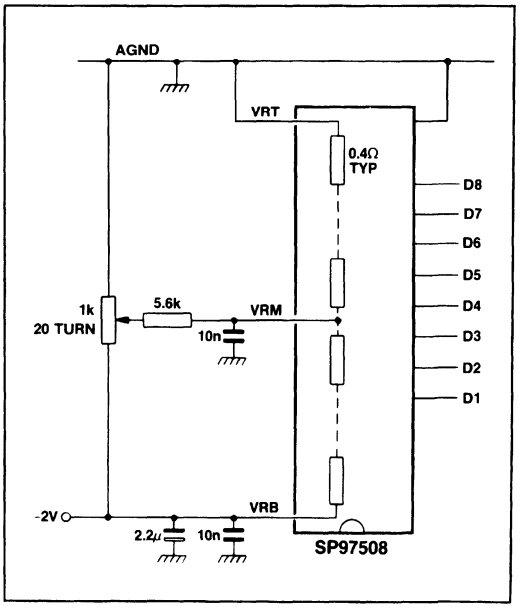


Fig.8 Reference connections

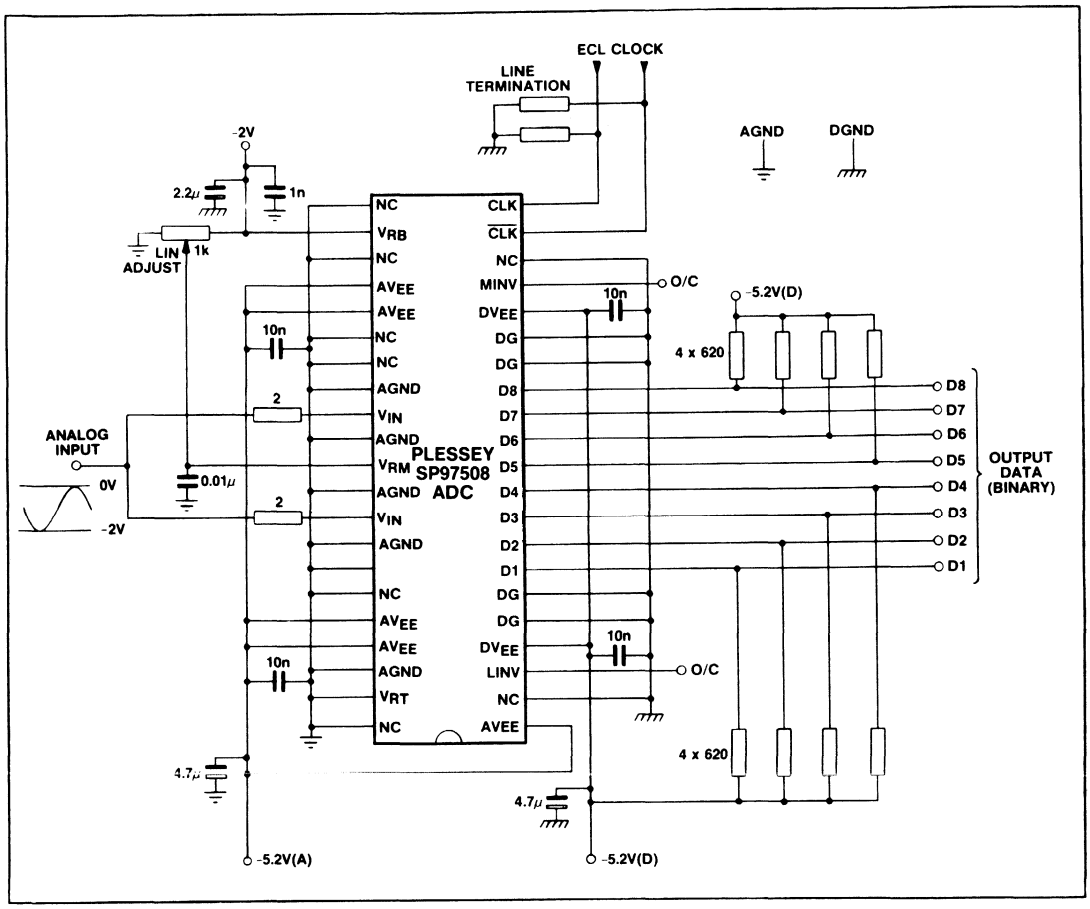


Fig.9 Test and applications circuit

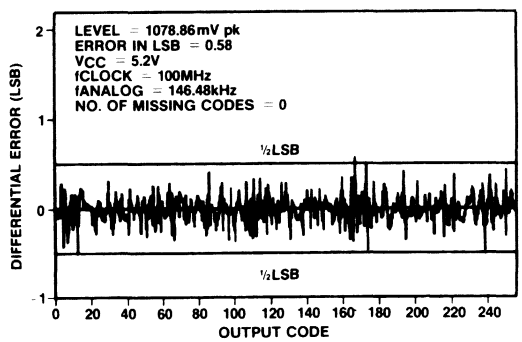


Fig.10 Differential linearity in LSB, typical production device

SP97618

8-BIT HIGH SPEED GRAPHICS DAC

The SP97618 is a 200 MegaSample Per Second (MSPS), 8-bit digital-to-analog converter, capable of directly driving a 75Ω load to standard video levels. Most applications require no extra registering, buffering, or deglitching. Four special level controls make the device ideal for video applications. All data and control inputs are ECL compatible.

FEATURES

- Pin Replacement for TDC1018 - But Faster
- 200 MSPS Update Rate (Typ.)
  150 MSPS Update Rate (Guaranteed)
- 8-Bit Resolution and Accuracy
- 1/2 LSB Linearity
- Power Supply Noise Rejection Typically >80dB
- Registered Data and Video Controls
- Differential Current Outputs
- Video Controls: SYNC, BLANK, BRighT, Force High
- Inherently Low Glitch Energy
- ECL Compatible
- Multiplying Mode Capability
- Power Dissipation 800mW
- Available in 24 Lead DIP Package
- Single -5.2V Power Supply
- On Board Reference Buffer
- Operating Temperature Range:
  Industrial Plastic -40°C to +85°C

ORDERING INFORMATION

SP97618C DP (Industrial Plastic Package)

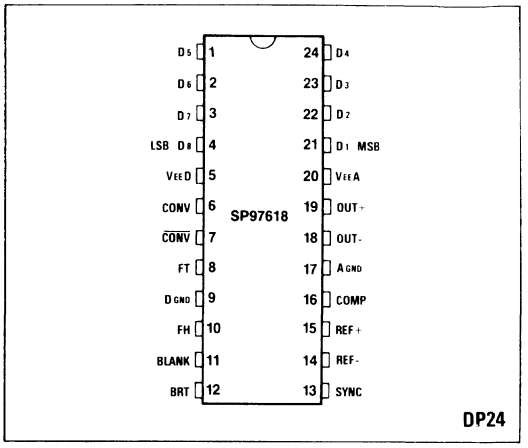


Fig.1 Pin connections (top view)

APPLICATIONS

- RGB Graphics (1K x 1K pixels)
- High Resolution Video
- Raster Graphic Displays
- Digital Waveform Synthesisers
- Automated Test Equipment
- Digital Transmitters/Modulators

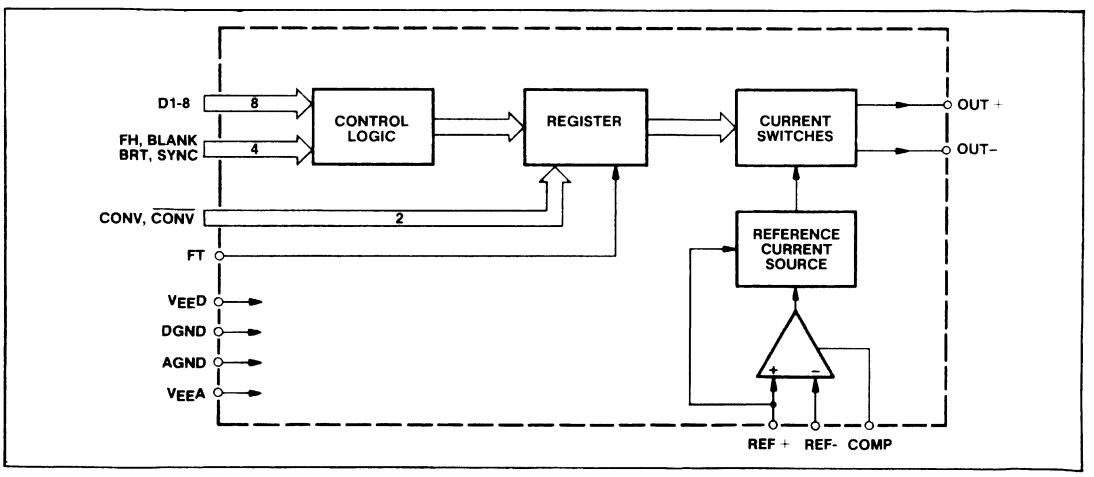


Fig.2 SP97618 functional block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C

DC Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Digital supply voltage	V_{EED}	-4.9	-5.2	-5.5	V	Measured to D_{GND}
Analog supply voltage	V_{EEA}	-4.9	-5.2	-5.5	V	Measured to A_{GND}
Supply current	$I_{EEA} + I_{EED}$			140	mA	$V_{EEA} = V_{EED}$ = Max
Analog ground voltage	V_{AGND}	-0.1	0.0	0.1	V	Measured to D_{GND}
Supply voltage differential	$V_{EEA} - V_{EED}$	-0.1	0.0	+0.1	V	
CONV input voltage, common mode range	V_{ICM}	-0.5		-2.5	V	
CONV input voltage differential	V_{IDF}	0.4		1.2	V	
Min. CONV pulse width, LOW	t_{PWL}		2	3	ns	
Min. CONV pulse width, HIGH	t_{PWH}		2	3	ns	
Min. Set up time, data and controls	t_S		2	4	ns	
Hold time, data and controls	t_H	0			ns	
Input voltage, logic LOW	V_{IL}	-1.5			V	
Input voltage, logic HIGH	V_{IH}			-1.0	V	
Reference current	I_{REF}				mA	
Video standard levels		1.059	1.115	1.171		
8-bit linearity		1.0		1.3	mA	
Compensation capacitor	C_C		5		nF	

System Performance Characteristics

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Linearity error integral, terminal based	ELI			±0.2	%	V_{EEA},V_{EED} = Nom I_{REF} = Nom
Linearity error differential	ELD			±0.2	%	V_{EEA}, V_{EED} = Nom I_{REF} = Nom
Output offset current	I_{OF}		0.7	10	μA	V_{EEA}, V_{EED} = Max
Absolute gain error	E_G		±0.5	±5	%	V_{EEA}, V_{EED} = Min I_{REF} = Nom
Gain error tempco	TC_G			±0.024	%/°C	V_{EEA}, V_{EED} = Min I_{REF} = Nom
Power supply rejection ratio (Note (1))	PSRR		90	45	dB	V_{EEA}, V_{EED} = Nom I_{REF} = Nom
Power supply rejection ratio (Note (2))	PSRR		90	55	dB	V_{EEA}, V_{EED} = Nom I_{REF} = Nom
Power supply sensitivity	PSS			120	μA/V	V_{EEA}, V_{EED} = Nom I_{REF} = Nom
Peak glitch energy (Area) (Note (3))	G_E		14	30	pV-sec	FT = 1
Feedthrough clock (Note (4))	FT_C		-70	-50	dB	Data = Constant
Feedthrough data (Note (4))	FT_D		-60	-50	dB	Clock = Constant

NOTES
1. 20kHz • 0.3V ripple on $V_{EE}A$, $V_{EE}D$ dB's relative to full Gray Scale.
2. 60Hz • 0.3V ripple on $V_{EE}A$, $V_{EE}D$ dB's relative to full Gray Scale.
3. 37.5 Ohm load. Average glitch energy approaches zero.
4. dB relative to full Gray Scale. 150MHz bandwidth limit.

AC Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Maximum update rate	F_S	150	200		MSPS	$V_{EE}A$, $V_{EE}D$ = Min
Clock to output delay clocked mode	t_{DSC}			8	ns	$V_{EE}A$, $V_{EE}D$ = Min, FT = 0
Data to output delay, transparent mode	t_{DST}			13	ns	$V_{EE}A$, $V_{EE}D$ = Min, FT = 1
Current settling time clocked mode	t_{SI}					$V_{EE}A$, $V_{EE}D$ = Min, FT = 0
0.2 %				10	ns	
0.8 %				8	ns	
3.2 %				5	ns	
Rise time, current	t_{RI}			1.1	ns	10 % to 90 % of Gray Scale

ABSOLUTE MAXIMUM RATINGS

Supply Voltage

$V_{EE}D$ (measured to D_{GND})	7V
$V_{EE}A$ (measured to A_{GND})	7V
A_{GND} (measured to D_{GND})	±0.5V

Input

CONV, Data and Controls (measured to D_{GND})	$V_{EE}D$ to 0.5V
Reference input, applied voltage (measured to A_{GND})	
REF +	$V_{EE}A$ to 0.5V
REF-	$V_{EE}A$ to 0.5V
Reference input, applied current, externally forced.	
REF +	6.0mA
REF-	0.5mA

Output

Analog output, applied voltage (measured to A_{GND})	
OUT +	-2V to +2V
OUT-	-2V to +2V
Analog output, applied current externally forced.	
OUT +	50mA
OUT-	50mA

THERMAL CHARACTERISTICS

θ_{JA}	65 deg C/W (typ)
θ_{JC}	15 deg C/W (typ)
T_{amb}	-40°C to +85°C
Maximum storage temperature	-55°C to +150°C
Lead temperature (soldering 60 sec)	300°C

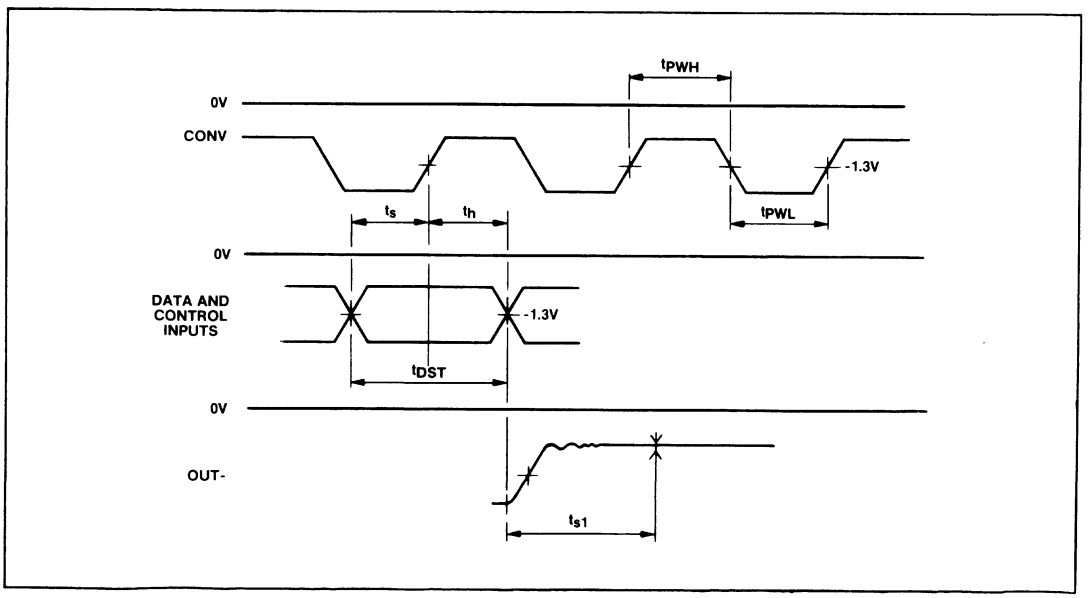


Fig.3 Timing diagram

DEVICE PIN FUNCTIONAL DESCRIPTION

Pin No.	Name	Description
21 - 24, 1 - 4	D_1 - D_8	To allow the internal register to aquire the input data correctly the eight digital data inputs, D_1 - D_8, must be valid one data set-up time before each rising edge of the clock, and remain valid for one data hold time after this rising edge. D_1 - D_8 are overridden by FH, BLANK, or SYNC = 1.
5	$V_{EE}D$	Digital supply voltage, -5.2V typ. ± 0.25V.
6, 7	CONV, $\overline{CONV}$	Differential clock inputs which should have V_{IH} and V_{IL} levels compatible with standard ECL logic.
8	FT	Feedthrough (asynchronous control). When FT = 1, the input register is transparent.
9	D_{GND}	Digital ground.
10	FH	Force High control. FH = 1 forces the output current to the equivalent of all data values D_1 - D_8 high. 10% enhancement of this value is available, via the BRT control. In the hierarchy of the controls, FH overrides only the data.
11	BLANK	Blank level control. When high, BLANK forces the output to -20.826mA (if I_{REF} = 1.185mA), which is slightly below the normal low level signal generated by data = 0. BLANK takes precedence over all controls except SYNC and disables BRT.
12	BRT	Brightness enhancement control. When high, BRT increases the signal present by 10 % of the full scale current. This control is disabled when SYNC or BLANK is asserted.
13	SYNC	SYNC level control. When high, SYNC forces the output of the chip to a full negative output (standard -28.57mA for an I_{REF} input of 1.185mA). SYNC = 1 takes precedence over all other controls and disables BRT.
15, 14	REF +, REF-	Connections for a differential reference current source.
16	COMP	Connection for compensation capacitor for internal reference buffer.
17	A_{GND}	Analog ground.
19, 18	OUT +, OUT-	Current outputs, which comprise a differential pair designed to drive 37.5Ω loads directly.
20	$V_{EE}A$	Analog supply voltage, -5.2V typ. ± 0.25V.

SYNC	BLANK	FORCE HIGH	BRIGHT	DATA INPUT	OUT- (mA) NOTE (1)	OUT- (V) NOTE (2)	OUT- (IRE) NOTE (3)	DESCRIPTION NOTE (4)
1	X	X	X	X	28.57	-1.071	-40	SYNC LEVEL
0	1	X	X	X	20.83	-0.781	0	BLANK LEVEL
0	0	1	1	X	0.00	0.00	110	ENHANCED HIGH LEVEL
0	0	1	0	X	1.95	-0.073	100	NORMAL HIGH LEVEL
0	0	0	0	000 . .	19.40	-0.728	7.5	NORMAL LOW LEVEL
0	0	0	0	111 . .	1.95	-0.073	100	NORMAL HIGH LEVEL
0	0	0	1	000 . .	17.44	-0.654	17.5	ENHANCED LOW LEVEL
0	0	0	1	111 . .	0.00	0.00	110	ENHANCED HIGH LEVEL

NOTES
1. OUT+ is complementary to OUT- Current is specified as conventional current when flowing into the device.
2. The voltage produced when driving a standard load configuration (37.5ohms).
3. 140 IRE Units = 1.00V
4. RS-343-A tolerance on all control values is assumed.

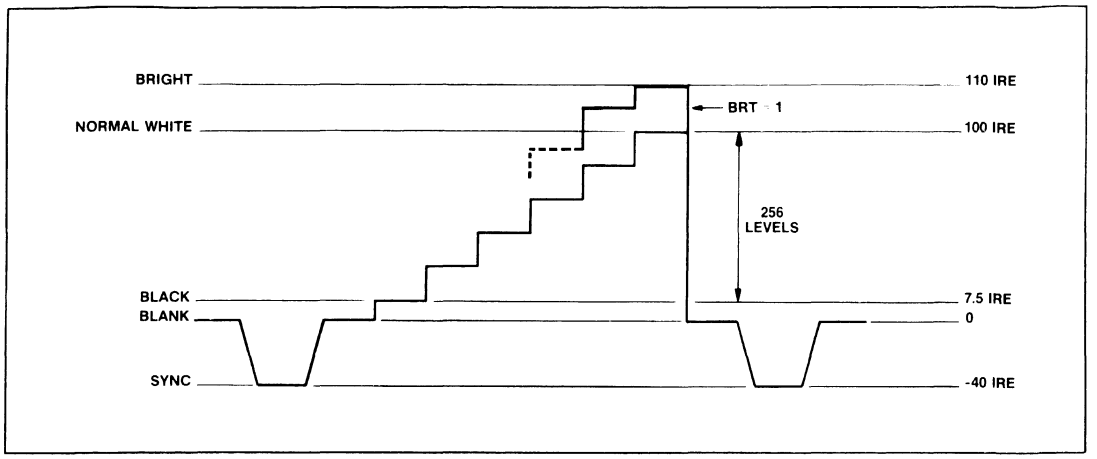


Fig.4 Video waveform

APPLICATIONS

Board Construction

As the Plessey SP97618 contains a mixture of high speed digital and analog circuitry, care must be taken with ground plane and component placement.

Supply decoupling should be placed close to the device with good high frequency, low loss capacitors. Pins 16 and 17 should be decoupled directly to VEEA (pin 20).

The settling time of the output is aided by matching the loads on the OUT + and OUT- outputs. A 37Ω resistor from pin 19 to ground is shown in the applications diagram.

FT Input

The feedthrough input, when high, will cause the internal register to become transparent. When using the D to A converter in the transparent mode, it is essential that time skew on the input data is minimised, because this skew will be converted directly to output glitch energy.

Video Controls

Internal pulldown resistors allow these inputs to be left open circuit when not in use. The pulldown resistors are approximately 40kΩ connected to VEED.

The bright input causes the video information that is above 7.5 IRE to be placed on a pedestal that is 10 IRE units high.

Sync, Blank and Force High cause DC currents at the outputs as specified.

Convert Signal

The input data and controls are acquired into the register on the rising edge of the CONV (convert) command. The device is designed to accept differential ECL levels from devices such as the Plessey SP1658 voltage controlled multivibrator. Single ended CONV signals can be used if the unused CONV inupt is biased at -1.3V and decoupled close to the device pin. Care should be taken with the termination of lines driving the CONV signal. For long lines or voltage levels that are not ECL, a low cost high speed comparator can be used such as the Plessey SP9680.

Data Inputs

As the SP97618 contains an input register, (FT = 0) no external latching is required. Single in-line resistors of values 270Ω and 150Ω can be used in the Thevenin configuration (see applications circuit, Fig.5) for the termination of 100Ω twisted pair data input lines.

If long lines are used and the device is in the transparent mode (FT = 1) then two line receivers such as the Plessey SP1692 can be used before the data inputs. Twos complement data can be converted by simply configuring the SP1692 to invert the MSB.

Multiplying Mode

The output amplitude can be modulated by varying the voltage fed to REF +. This technique is only practical at low modulating frequencies. The multiplying bandwidth is affected by amplitude and the compensation capacitor on pin 16. The circuit will remain stable with this capacitor reduced to 2nF.

Output Load

To maintain the fast settling time of this device, it is recommended that both outputs are terminated with equal resistance. This is regardless of whether single or differential output drive is required (see Fig.5).

Output Compliance

The output voltage of the circuit can be DC offset more positive by connecting the OUT + and OUT- loads to a positive voltage (<1.5V).

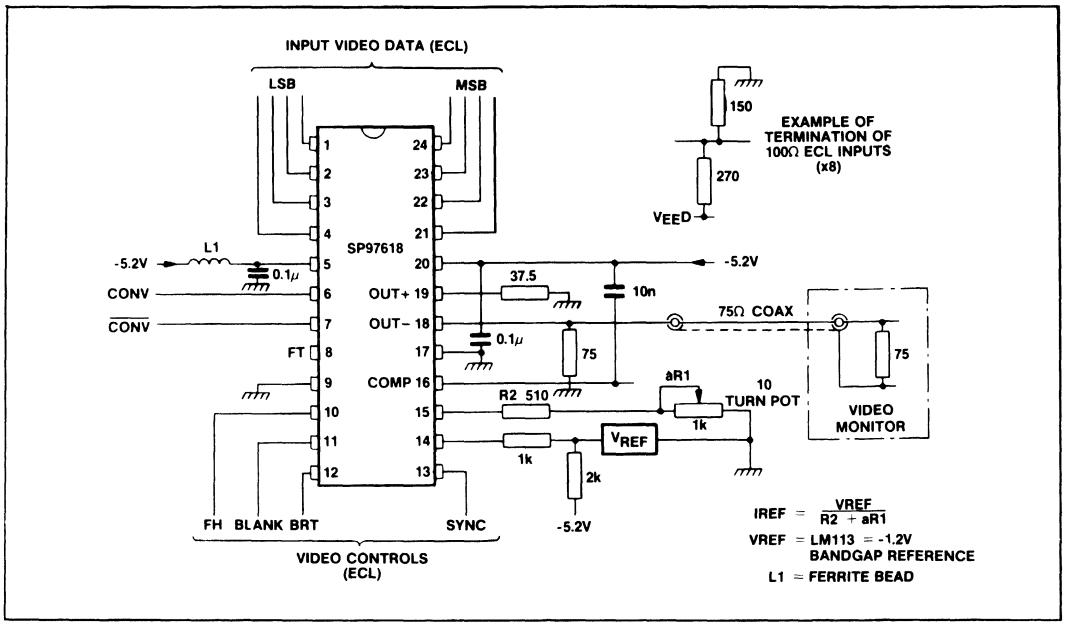


Fig.5 Application diagram SP97618

SP98608

8-BIT LATCHED 450MHz MULTIPLYING D-A CONVERTER

The SP98608 is an ECL 10K compatible 8-bit latched DAC. The 2.2nsec settling time allows a 450 megasample per second conversion rate. An inherently low glitch design is used and the complementary current outputs are suitable for direct transmission line drive. The SP98608 design includes a high performance band-gap voltage reference and reference amplifier.

Both current and voltage multiplying modes are available. The input latch can be switched into transparent mode for applications that require low through delay.

FEATURES

- Latched Inputs
- 2.2ns Settling Time ½ LSB Typically
- 8 Bits ±½ LSB Integral and Differential Linearity
- Operating Temperature Range -40°C to +85°C
- ECL 10K Standard Inputs
- Complementary Current Outputs, 40mA Full Scale
- Reference Temperature Coefficient Typically < 40ppm/°C
- Single -5.2V Supply

ORDERING INFORMATION

SP98608 B DG (Industrial - Ceramic DIL package)
SP98608 LC (Industrial - Ceramic LCC package)
(Under development)

APPLICATIONS

- Data Conversion
- Video Graphic Displays
- Instrumentation
- Waveform Generators
- High Speed Modems
- ADC Evaluation

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-5.7V
Digital input voltage	0 to -4.5V
Minimum R_{SET} (from 0V)	175Ω
Maximum R_{SET}	2.5kΩ
Output reference supply (V_L)	0 to +3V
Reference input	±2V
Storage temperature range	-55°C to 150°C
Operating junction temperature	<175°C
Lead temperature (soldering 60 sec)	300°C

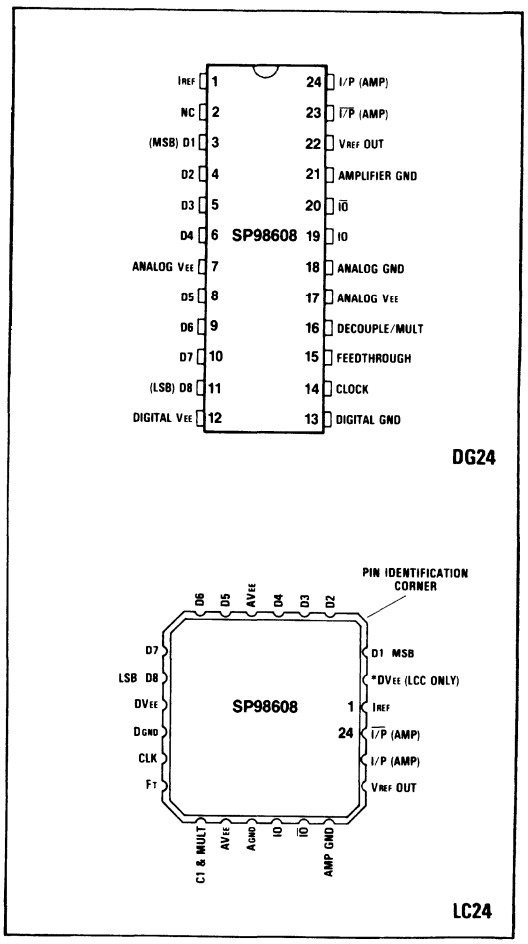


Fig.1 Pin connections - top view

THERMAL CHARACTERISTICS

θJ_C = 28°C/W
θJ_A = 90°C/W

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 25° C; V_{EE} = -5.2V ± 5 %; R_{SET} = 240Ω; Input voltage: High = -0.81V, Low = -1.85V

Characteristic	Value			Unit	Conditions
	Min.	Typ.	Max.		
Supply current I_{EE}		135	154	mA	All inputs at -1.8V
Logic inputs:					
V_{IH}	-0.96		-0.81	V	Standard ECL
V_{IL}	-1.85		-1.65	V	10K compatible
$I_{IN(HI)}$		115	200	μA	All inputs HI
Reference voltage V_{REF}		-1.280		V	
Reference voltage temp. coeff.	-80	0	80	ppm/°C	-30°C to +85°C
Output current - full scale	2		44	mA	R_{SET} 1.3kΩ to 85Ω
Output current - full scale	38	42		mA	R_{SET} = 130Ω
Output compliance	-1.2		+1.0	V	T_{amb} = 25°C Note 3
	-1.0		+1.0	V	T_{amb} = 85°C Note 3
Bit size (LSB)	158	166	175	μA	Current output, R_{SET} = 130Ω
Resolution	8			Bits	
	0.391			%	
Integral non-linearity			0.5	LSB	End point integral
Differential non-linearity			0.5	LSB	
Output dynamic parameters (see Note 1)					
Rise time t_r		600		ps	10 to 90 %
Glitch energy (latched)		20		psV	Mid-point
Glitch energy (transparent)		140		psV	transition
Noise output		-90	-83	dBm	See Note 2
Power supply rejection ratio (output WRT supply)	45	80		dB	±0.3V at 20kHz
Multiplying mode - voltage					
Multiplying input voltage range	-2		0	V	
Reference input resistance		10		kΩ	
Multiplying input bandwidth		30		MHz	-3dB
Transfer function non-linearity		0.2	1.0	%FS	DC
Multiplying mode - current					
Multiplying input current range	1		15	mA	
Set current input resistance		400		Ohms	
Multiplying input bandwidth		300		MHz	-3dB
Transfer function non-linearity		1.0	3.0	%FS	DC

NOTES

1. Dynamic parameters guaranteed but not 100% tested.
2. Noise in any 10kHz band in the range 0.1 to 500MHz, for any digital input.
3. The output positive compliance can be increased beyond +1.0V at the expense of linearity. See Fig.4 for circuit configuration.
4. Analog and digital grounds should be connected together at the device pins.

Dynamic characteristic (Note 1)	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Update rate	F_{CLK}		450		MHz	
Latch setup time	t_s		0.9		ns	
Latch hold time	t_h	0			ns	
Settling time full scale	t_{st}		2		ns	½ LSB
Internal clock delay	t_c		500		ps	
Initial time to 10 %	t_i		50		ps	

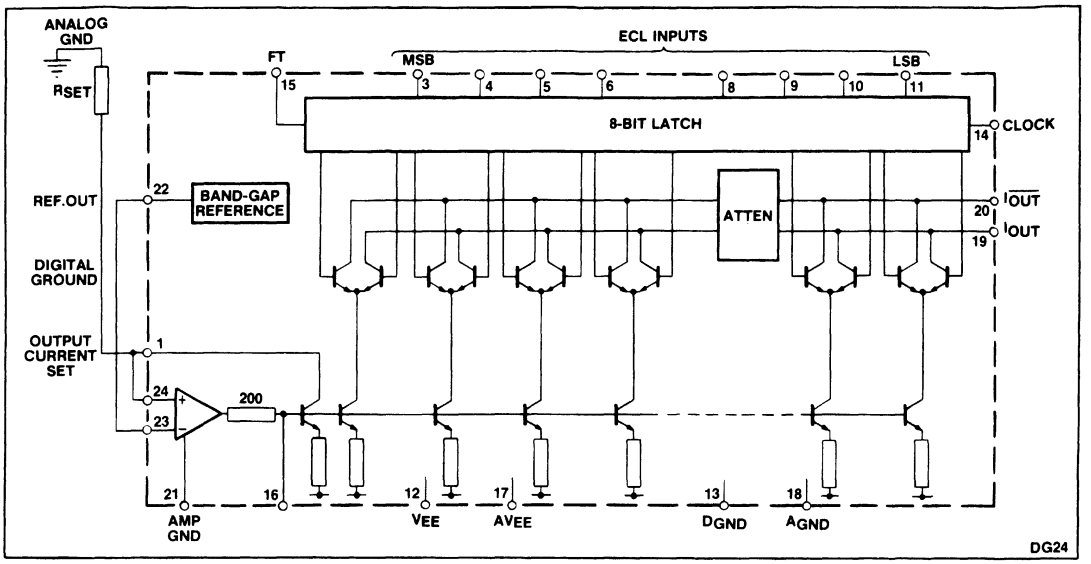


Fig.2 SP98608 block diagram

OPERATING NOTES

The pinout of the device is shown in Fig.1. External components are the current setting resistor and decoupling capacitors.

The DAC has current outputs, with a nominal full-scale of 40mA, corresponding with a 1 volt drop across a 25Ω load.

The actual output current is determined by the on-chip reference voltage and an off-chip current setting resistor. Output current, I_{OUT}, is given by

$$I_{OUT} = 4 \times \frac{V_{REF}}{R_{SET}} \text{ at full scale}$$

A complementary I_{OUT} is also provided. If single output operation is employed it must be ensured that the complementary output is terminated in an identical manner to the used output. The setting resistor, R_{SET}, is typically 130Ω, giving a full-scale output current of 42mA, and should have a temperature coefficient similar to that of the output load resistor.

Reference

The reference supply is internally compensated; however, to reduce the possibility of instability in some circuits, it has been bonded out to pin 16, it can therefore be decoupled to AV_{EE} if required.

Clock

The clock input is ECL 10K compatible. Data at the device inputs are acquired by the input latch on the rising edge of the clock.

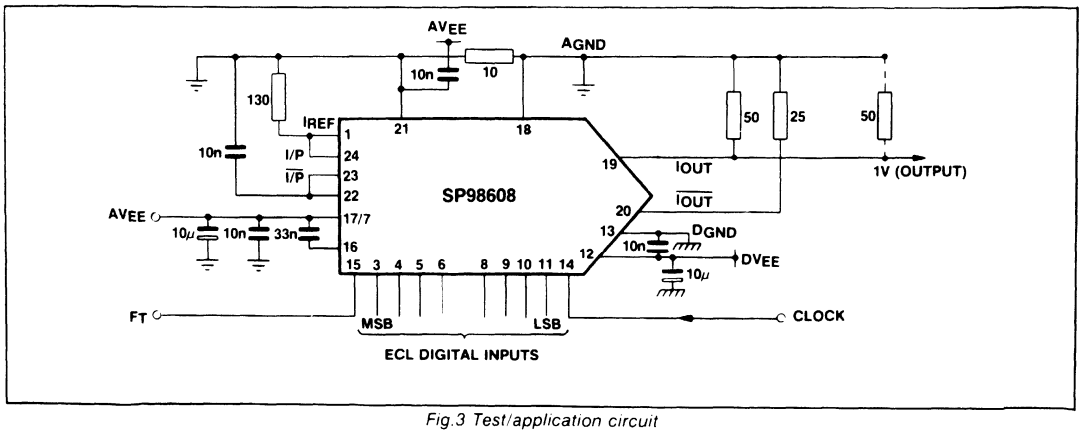


Fig.3 Test/application circuit

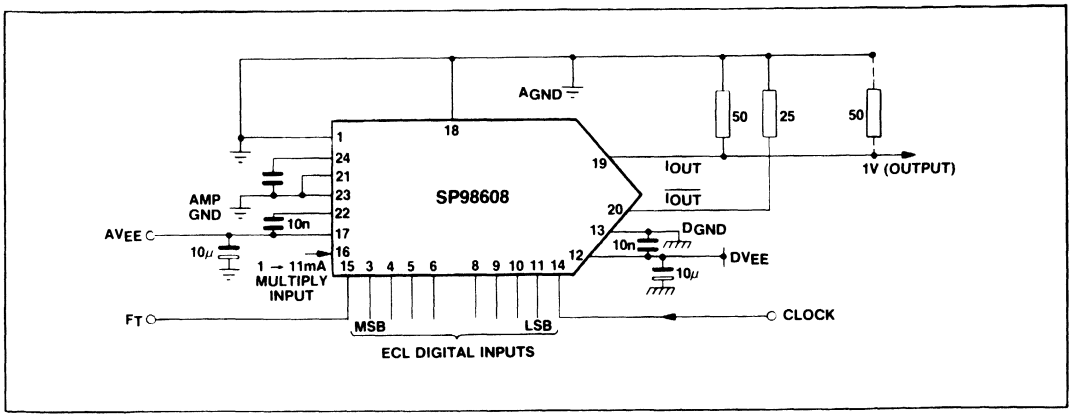


Fig.4 Current multiplying mode

FT (Feedthrough)

The FT input allows both transparent or latched data inputs. When open circuit this pin will self bias to -2V and the data will be retained by the input latch for one clock cycle.

When the FT input is connected to 0V the input latch will be transparent. In this mode, it is essential that the input data has low time skew (<100ps) to avoid output glitches.

Multiplying Mode

Multiplying operation of the DAC is available in two modes: either a voltage applied in place of the internal reference, or a current supplied via the current set pin.

Voltage Multiplying. The transfer function is approximately: IOUT (Full Scale) = 4 x VIN/RSET. While this mode offers the best linearity of operation, the frequency response limitations mean that the maximum usable bandwidth is limited to approximately 50kHz.

Current Multiplying. A circuit for using the DAC in current multiplying mode is shown in Fig.4. The transfer function is approximately: IOUT (Full Scale) = 4 x IIN. In this mode the current setting loop amplifier is not used.

The operational bandwidth of the current input to -3dB is at least 320MHz.

A 1V output is obtained into 25Ω when a current of approximately 11mA is fed into pin 16 and the input code is selected for full output current.

Output Compliance

Using the SP9778 with a load resistor not referred to ground, allows a larger output swing than the conventional connection of Fig.3. Connecting analog ground and the current setting resistor RSET to the load return supply ensures that the scale factor of the output is independent of the load reference.

Extending the compliance beyond +1V may cause slight degradation of linearity. +3V should be considered an absolute maximum.

TIMING

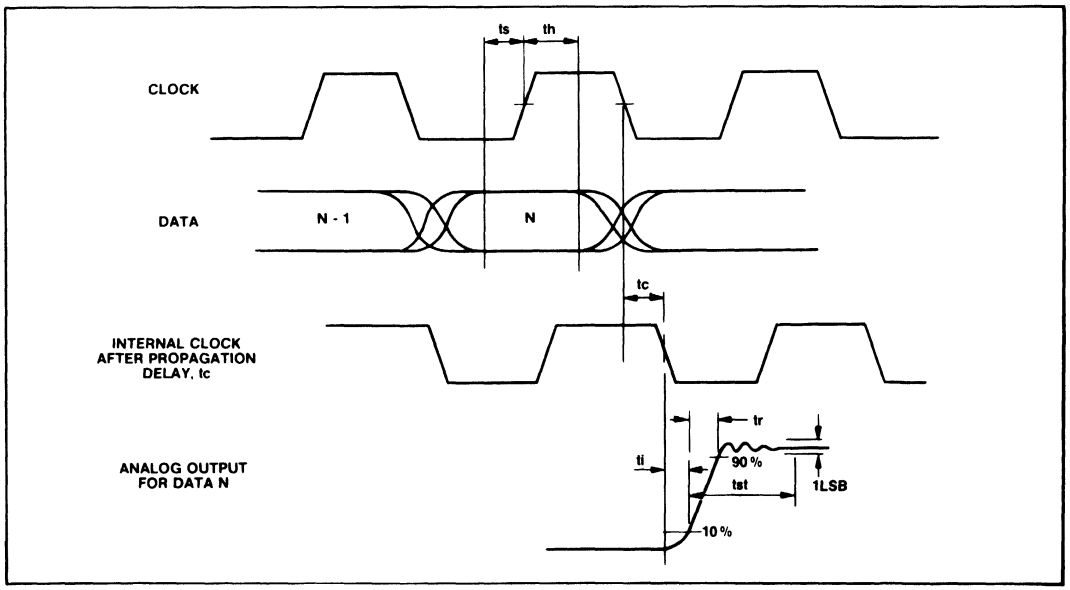


Fig.5 Timing diagram - latched mode

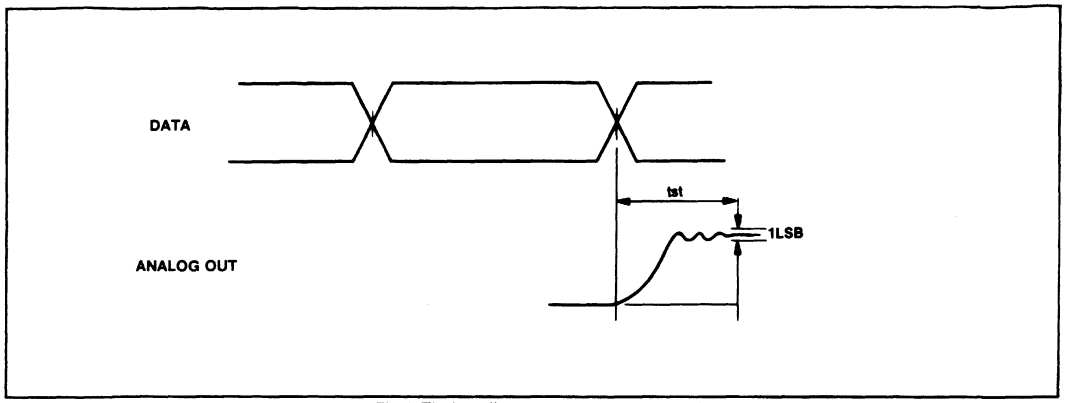


Fig.6 Timing diagram - transparent mode

PLESSEY
Semiconductors

ZN425E-8/ZN425J-8/ZN425D

8-BIT D-A/A-D CONVERTER

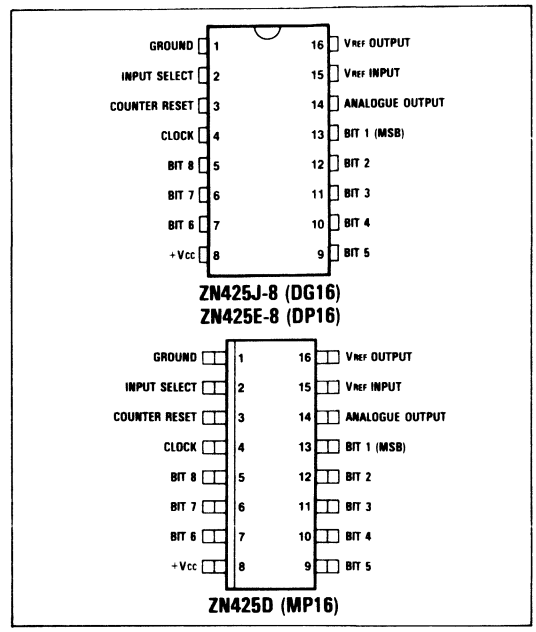
The ZN425 is a monolithic 8-bit D-A converter containing an R-2R ladder network of diffused resistors with precision bipolar switches, and in addition a counter and a 2.5V precision voltage reference. The counter is a powerful addition which allows a precision staircase to be generated very simply by clocking the counter.

FEATURES

- ±½ LSB Linearity Error
- 0°C to +70°C (ZN425E-8, ZN425D)
- -55°C to +125°C (ZN425J-8)
- TTL and 5V CMOS Compatible
- Single +5V Supply
- Settling Time (D-A) 1μs Typical
- Conversion Time (A-D) 1ms Typical, using Ramp and Compare Technique
- Extra Components Required
  D-A:Reference Capacitor (Direct Voltage Output Through 10kohms Typ.)
  A-D:Comparator, Gate, Clock and Reference Capacitor

ORDERING INFORMATION

Device type	Operating temperature	Package
ZN425D	0°C to +70°C	MP16
ZN425E-8	0°C to +70°C	DP16
ZN425J-8	-55°C to +125°C	DG16



Pin connections - top view

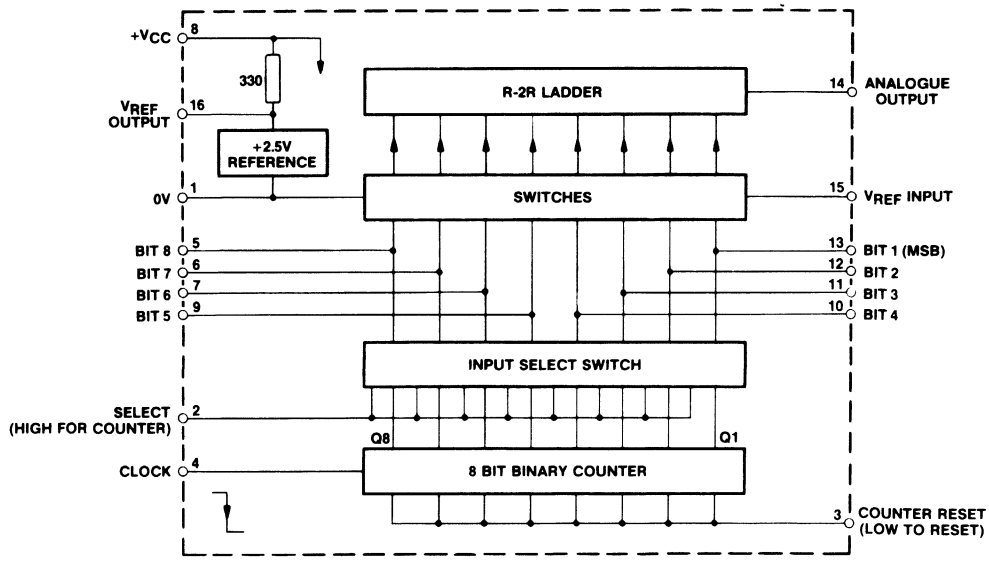


Fig.1 System diagram

INTRODUCTION

The ZN425 is an 8-bit dual mode D-A/A-D converter. It contains an 8-bit D-A converter using an advanced design of R-2R ladder network and an array of precision bipolar switches plus an 8-bit binary counter and a 2.5V precision voltage reference all on a single monolithic chip.

The special design of ladder network results in full 8-bit accuracy using normal diffused resistors.

The use of the on-chip reference voltage is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.

By including on the chip an 8-bit binary counter, A-D conversion can be obtained simply by adding an external comparator (ZN424P) and clock inhibit gating (7400).

By simply clocking the counter the ZN425 can be used as a self-contained precision ramp generator.

A logic input select switch is incorporated which determines whether the precision switches accept the outputs from the binary counter or external digital inputs depending upon whether the control signal is respectively high or low.

The converter is of the voltage switching type and uses an R-2R resistor ladder network as shown in Fig. 2.

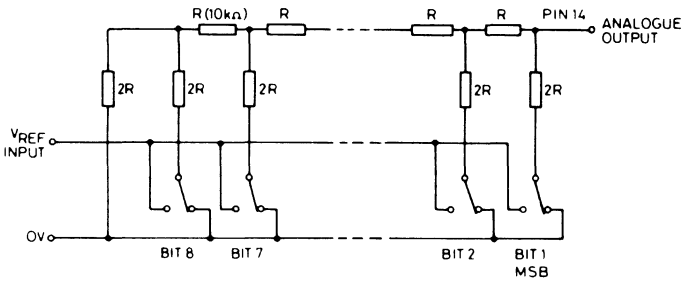


Fig. 2 The R-2R ladder network

Each 2R element is connected either to 0V or V_{REF} by transistor switches specially designed for low offset voltage (typically 1mV).

Binary weighted voltages are produced at the output of the R-2R ladder, the value depending on the digital number applied to the bit inputs.

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	+7.0V
Max. voltage, logic and V_{REF} inputs	+5.5V See note 3
Operating temperature range	0°C to 70°C (ZN425E-8, ZN425D)
	-55°C to +125°C (ZN425J-8)
Storage temperature range	-55°C to +125°C

CHARACTERISTICS (at $T_{amb} = 25°C$ and $V_{CC} = +5V$ unless otherwise specified)

Internal voltage reference

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output voltage	V_{REF}	2.4	2.55	2.7	V	I = 7.5mA (internal)
Slope resistance	R_S	–	2	4	Ω	I = 7.5mA (internal)
V_{REF} temperature coefficient		–	40	–	ppm/°C	I = 7.5mA (internal)

Note: The internal reference requires a 0.22μF stabilising capacitor between pins 1 and 16.

8-Bit D-A converter and counter

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Resolution		8	–	–	bits	
Non-linearity		–	–	±0.5	LSB	See note 3
Differential non-linearity		–	±0.5	–	LSB	See note 6
Settling time		–	1.0	–	μs	1LSB step
Settling time to 0.5LSB		–	1.5	2.5	μs	All bits ON to OFF or OFF to ON
Offset voltage ZN425J-8	V_{OS}	–	8	12	mV	All bits OFF See note 3
ZN425E-8 and ZN425D		–	3	8	mV	
Full-scale output		2.545	2.550	2.555	V	All bits ON Ext. $V_{REF} = 2.56V$
Full-scale temp. coefficient		–	3	–	ppm/°C	Ext. $V_{REF} = 2.56V$
Linearity error temp. coeff.		–	7.5	–	ppm/°C	Relative to F.S.R.
Analogue output resistance	R_o	–	10	–	kΩ	
External reference voltage		0	–	3.0	V	
Supply voltage	V_{CC}	4.5	–	5.5	V	See note 3
Supply current	I_s	–	25	35	mA	
High level input voltage	V_{IH}	2.0	–	–	V	See notes 1 and 2
Low level input voltage	V_{IL}	–	–	0.7	V	

CHARACTERISTICS (cont.)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
High level input current	I_{IH}	–	–	10	μA	V_{CC} = max. V_I = 2.4V
		–	–	100	μA	V_{CC} = max. V_I = 5.5V
Low level input current bit inputs	I_{IL}	–	–	−0.68	mA	V_{CC} = max. V_I = 0.3V
Low level input current, clock reset and input select	I_L	–	–	−0.18	mA	
High level output current	I_{OH}	–	–	−40	μA	
Low level output current	I_{OL}	–	–	1.6	mA	
High level output voltage	V_{OH}	2.4	–	–	V	V_{CC} = min. Q = 1 I_{load} = −40μA
Low level output voltage	V_{OL}	–	–	0.4	V	V_{CC} = min., Q = 0 I_{load} = 1.6mA
Maximum counter clock frequency	f_c	3	5	–	MHz	See note 5
Reset pulse width	t_R	200	–	–	ns	See note 4

Notes:

1. The input select pin (2) must be held low when the bit pins (5, 6, 7, 9, 10, 11, 12 and 13) are driven externally.
2. To obtain counter outputs on bit pins the input select pin (2) should be taken to +Vcc via a 1kΩ resistor.
3. The ZN425J differs from the ZN425E and ZN425D in the following respects:
   (a) For the ZN425J, the maximum linearity error may increase to ±1LSB over the temperature ranges — -55°C to 0°C and +70°C to +125°C.
   (b) Maximum operating voltage. Between 70°C and 125°C the maximum supply voltage is reduced to 5.0V.
   (c) Offset voltage. The difference is due to package lead resistance. This offset will normally be removed by the setting up procedure, and because the offset temperature coefficient is low, the specified accuracy will be maintained.
4. The device may be reset by gating from its own counter.
5. F_{max} in A-D mode is 300kHz, see Operating Note 2.
6. Monotonic over full operating temperature range.

If pin 2 is high then the output equals the Q output of the corresponding counter.

If pin 2 is low then the output transistor, Tr1 is held off.

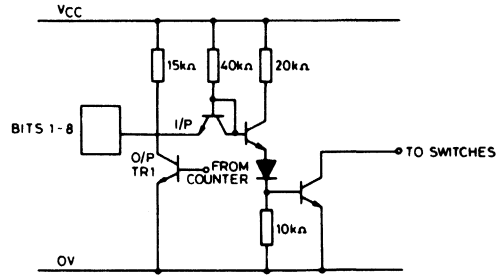


Fig. 3 Bit inputs/outputs

OPERATING NOTES

1. 8-bit D-A converter

The ZN425 gives an analogue voltage output directly from pin 14 therefore the usual current to voltage converting amplifier is not required. The output voltage drift, due to the temperature coefficient of the analogue output resistance R_o, will be less than 0.004% per °C (or 1LSB/100°C) if R_L is chosen to be $\geqslant 650k\Omega$.

In order to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary. Fig. 4 shows a typical scheme using the internal reference voltage. To minimise temperature drift in this and similar applications the source resistance to the inverting input of the operational amplifier should be approximately 6kΩ. The calibration procedure is as follows:

i. Set all bits to OFF (low) and adjust R_2 until $V_{OUT} = 0.000V$.
ii. Set all bits to ON (high) and adjust R_1 until V_{OUT} = Nominal full-scale reading - 1LSB.
iii. Repeat i. and ii.

e.g. Set F.S.R. to +3.840V − 1LSB
= 3.825V

$$(1LSB = \frac{3.84}{256} = 15.0mV)$$

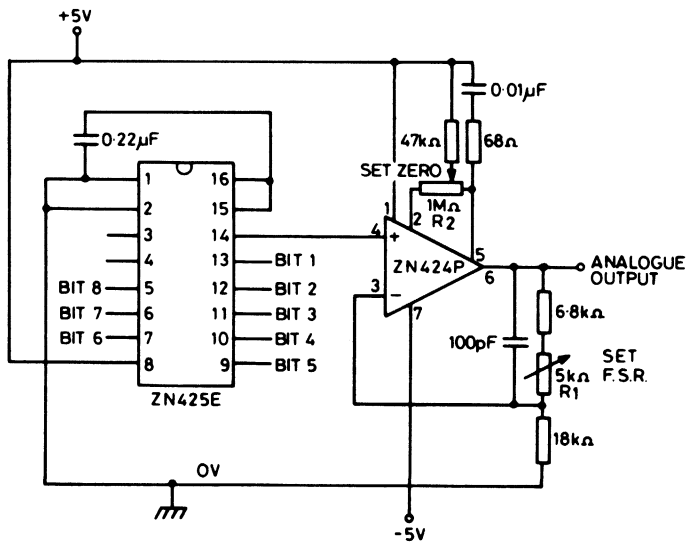


Fig. 4 8-bit D-A converter

2. 8-bit A-D converter

A counter type ADC can be constructed by adding a voltage comparator and a latch as in Fig. 5. On the negative edge of the CONVERT COMMAND pulse (15μs minimum) the counter is set to zero and the STATUS latch to logical 1. On the positive edge the gate is opened, enabling clock pulses to be fed to the counter input of the ZN425. The minimum negative clock pulse width to the ZN425 is 100ns. The analogue output of the ZN425 ramps until it equals the voltage on the other input of the comparator. At this point the comparator output goes low and resets the STATUS latch to inhibit further clock pulses. The logical 0 from the status latch indicates that the 8-bit digital output is a valid representation of the analogue input voltage.

A small capacitor of 47pF is added to the ZN425 output to stop any positive going glitches prematurely resetting the status latch. This capacitance is in parallel with the ZN425 output capacitance (20-30pF) and they form a time constant with the ZN425 output resistance (10kΩ). This time constant is the main limit to the maximum clock frequency. With a fast comparator the clock frequency can be up to 300kHz. Using the ZN424P as a comparator the clock frequency should be restricted to 100kHz. The conversion time varies with the input being a maximum for full-scale input.

Maximum conversion time =

$$\frac{256}{\text{clock frequency in Hz}} \text{ seconds}$$

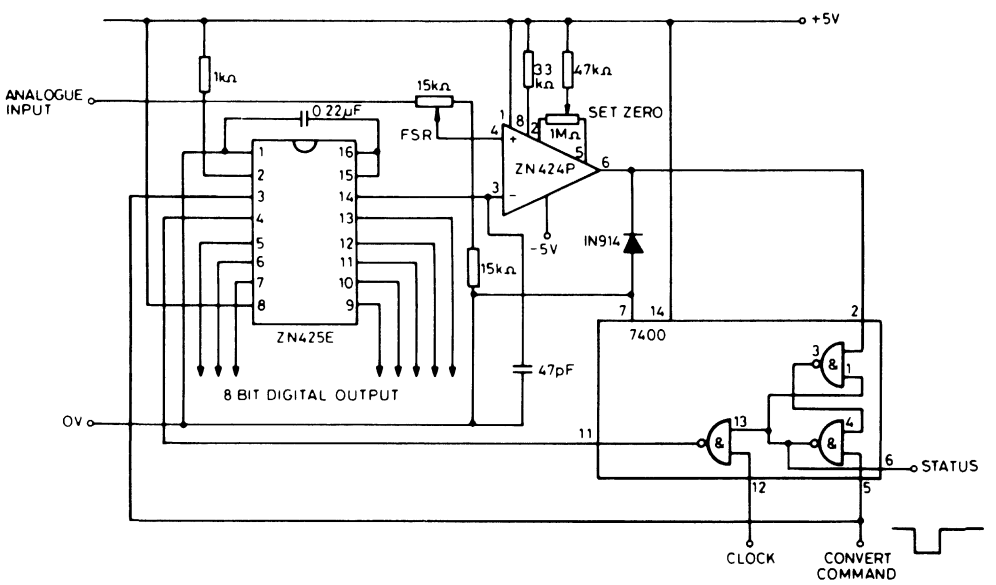


Fig. 5 8-bit A-D converter

3. Precision ramp generator

The inclusion of an 8-bit binary counter on the chip gives the ZN425 a useful ramp generator function. The circuit, Fig. 6, uses the same buffer stages as the D-A converter. The calibration procedure is also the same. Holding pin 2 low will set all bits to ON and if RESET is taken low with pin 2 high all the bits are turned OFF. If the end voltages of the ramp are not required to be set accurately then the buffer stage could be omitted and the voltage ramp will appear directly at pin 14.

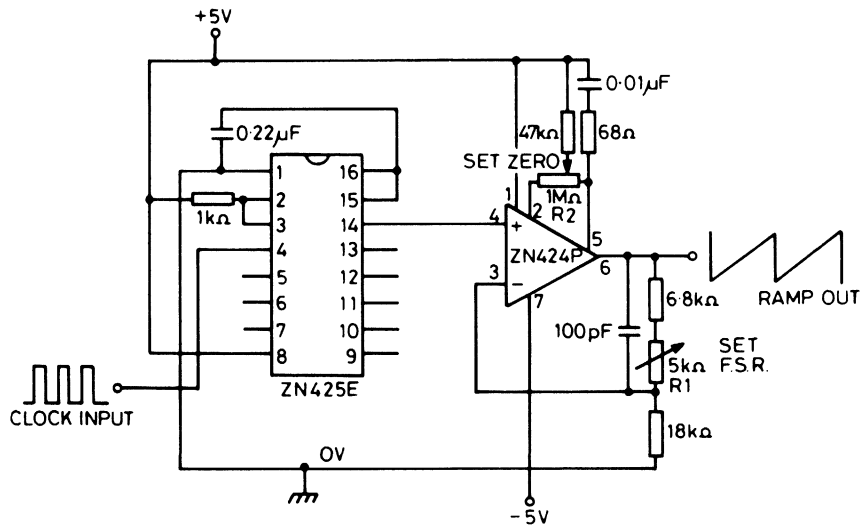


Fig. 6 Precision ramp generator

4. Alternative output buffer using the 741

The following circuit, employing the 741 operational amplifier, may be used as the output buffer for both the 8-bit D-A converter (Fig.4) and the precision ramp generator (Fig.6).

5. Further applications

Details of a wide range of additional applications, described in the Application Notes section.

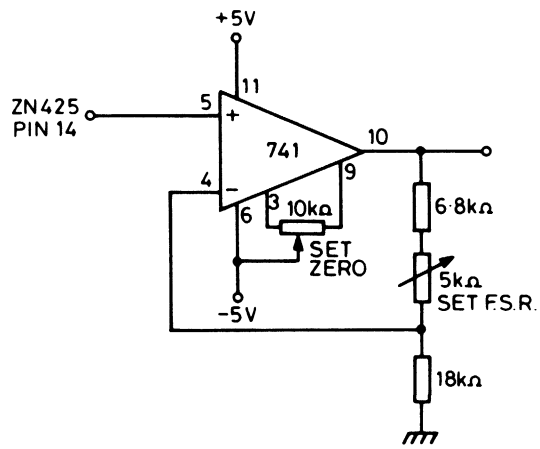


Fig. 7 The ZLD741 as output buffer

ZN426E-8/ZN426J-8/ZN426D

8-BIT D-A CONVERTER

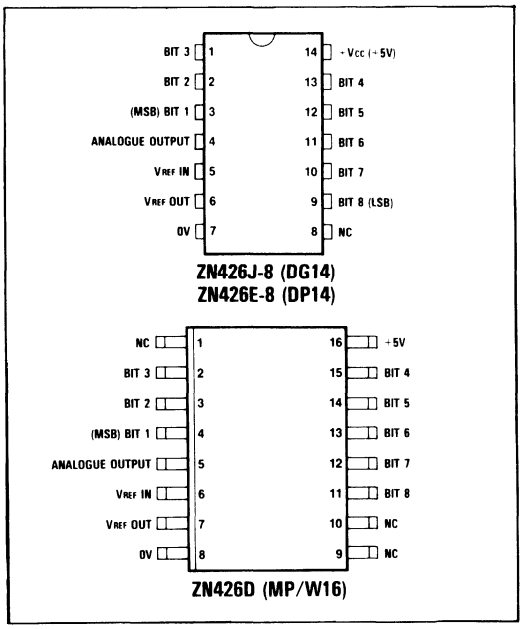
The ZN426 is a monolithic 8-bit D-A converter containing an R-2R ladder network of diffused resistors with precision bipolar switches and a 2.5V precision voltage reference.

FEATURES

- ±½ LSB Linearity Error
- Guaranteed Monotonic over the Full Operating Temperature Range
- 0°C to +70°C (ZN426E-8, ZN426D)
- -55°C to +125°C (ZN426J-8)
- TTL and 5V CMOS Compatible
- Single +5V Supply
- Settling Time 1 microsecond Typical
- Only Reference Capacitor and Resistor Required

ORDERING INFORMATION

Device type	Operating temperature	Package
ZN426D	0°C to +70°C	MP16W
ZN426E-8	0°C to +70°C	DP14
ZN426J-8	-55°C to +125°C	DG14



Pin connections - top view

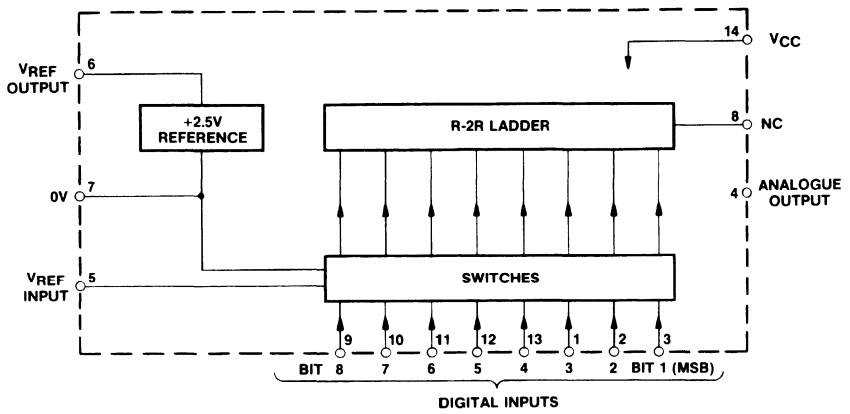


Fig.1 System diagram

INTRODUCTION

The ZN426 is an 8-bit D-A converter. It contains an advanced design of R-2R ladder network and an array of precision bipolar switches plus a 2.5V precision voltage reference all on a single monolithic chip.

The special design of ladder network results in full 8-bit accuracy using normal diffused resistors.

The use of the on-chip reference voltage is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted. In this case there is no need to supply power to the internal reference so R_{REF} and C_{REF} can be omitted

The converter is of the voltage switching type and uses an R-2R resistor ladder network as shown in Fig. 2.

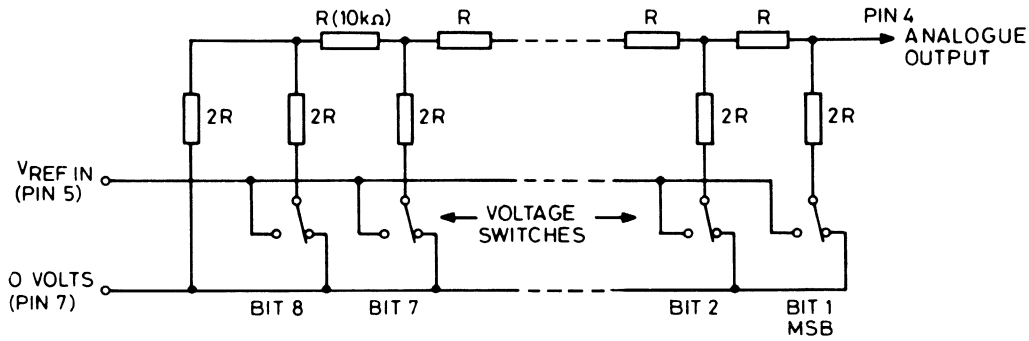


Fig. 2 The R-2R ladder network

Each 2R element is connected either to 0V or V_{REF} by transistor switches specially designed for low offset voltage (typically 1mV).

Binary weighted voltages are produced at the output of the R-2R ladder, the value depending on the digital number applied to the bit inputs.

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+7.0V
Max. voltage, logic and V_{REF} inputs	+5.5V
Operating temperature range	0°C to 70°C (ZN426E-8, ZN426D)
	-55°C to +125°C (ZN426J-8)
Storage temperature range	-55°C to +125°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5V, T_{amb} = 25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Converter Resolution		8	–	–	bits	
Non-linearity		–	–	±0.5	LSB	Note 1
Differential non-linearity		–	±0.5	–	LSB	Note 2
Settling time to 0.5LSB		–	1.0	–	μs	1LSB step
Settling time to 0.5LSB		–	2.0	–	μs	All bits ON to OFF or OFF to ON
Offset voltage ZN426J-8	V_{OS}	–	5.0	8.0	mV	All bits OFF Note 1
ZN426E-8 and ZN426D		–	3.0	5.0	mV	
V_{OS} temperature coefficient		–	5	–	μV/°C	
Full-scale output		2.545	2.550	2.555	V	All bits ON Ext. V_{REF} = 2.560V
Full-scale temp. coefficient		–	3	–	ppm/°C	Ext. V_{REF} = 2.560V
Non-linearity temp. coefficient		–	7.5	–	ppm/°C	Relative to F.S.R.

Notes

1. The ZN426J-8 differs from the ZN426E-8 and ZN426D in the following respects:
   (a) For the ZN426J-8, the maximum linearity error may increase to ±0.4% FSR i.e. ±1 LSB over the temperature ranges -55°C to 0°C and +70°C to +125°C.
   (b) Offset voltage. The difference is due to package lead resistance. This offset will normally be removed by the setting up procedure, and because the offset temperature coefficient is low, the specified accuracy will be maintained.
2. Monotonic over full temperature range.

ELECTRICAL CHARACTERISTICS (cont.)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Analogue output resistance	R_o	–	10	–	kΩ	
External reference voltage		0	–	3.0	V	
Supply voltage	V_{CC}	4.5	–	5.5	V	
Supply current	I_s	–	5	9	mA	
High level input voltage	V_{IH}	2.0	–	–	V	
Low level input voltage	V_{IL}	–	–	0.7	V	
High level input current	I_{IH}	–	–	10	μA	V_{CC} = max. V_I = 2.4V
		–	–	100	μA	V_{CC} = max. V_I = 5.5V
Low level input current	I_{IL}	–	–	−0.18	mA	V_{CC} = max. V_I = 0.3V
Internal voltage reference Output voltage	V_{REF}	2.475	2.55	2.626	V	Note* R_{REF} = 390Ω
Slope resistance	R_s	–	1	2	Ω	R_{REF} = 390Ω
V_{REF} temperature coefficient		–	40	–	ppm/°C	R_{REF} = 390Ω

Note* The internal reference requires a 1μF stabilising capacitor between pins 7 and 6 (C_{REF}) and a 390Ω resistor between pins 14 and 6 (R_{REF}).

APPLICATIONS

8-bit D-A converter

The ZN426 gives an analogue voltage output directly from pin 4 therefore the usual current to voltage converting amplifier is not required. The output voltage drift, due to the temperature coefficient of the analogue output resistance R_o, will be less than 0.004% per °C (or 1LSB/100°C) if R_L is chosen to be $\geqslant$650kΩ.

In order to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary. Fig. 3 shows a typical scheme using the internal reference voltage. To minimise temperature drift in this and similar applications the source resistance to the inverting input of the operational amplifier should be approximately 6kΩ. The calibration procedure is as follows:

i. Set all bits to OFF (low) and adjust R_2 until V_{OUT} = 0.000V.

ii. Set all bits to ON (high) and adjust R_1 until V_{OUT} = Nominal full-scale reading - 1LSB.

iii. Repeat i. and ii.

e.g.

Set F.S.R. to +3.840V − 1LSB = 3.825V

$$(1LSB = \frac{3.84}{256} = 15.0mV)$$

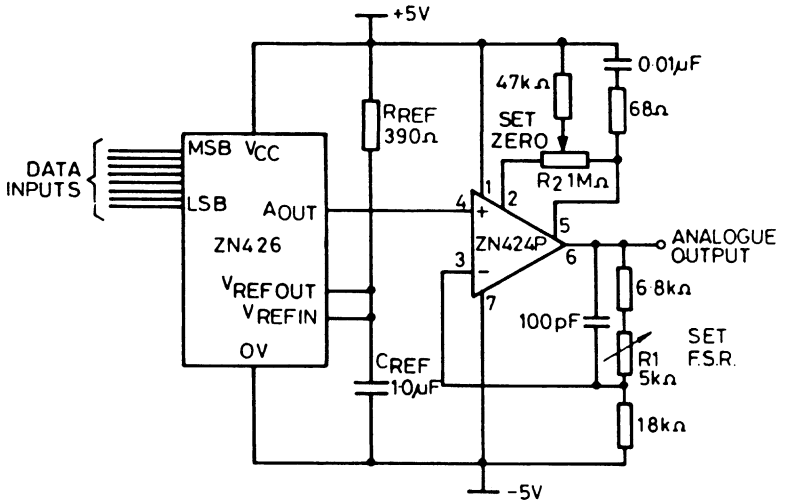


Fig. 3 8-bit D-A converter

Alternative output buffer using the 741

The circuit of Fig.4, employing the 741 operational amplifier, may be used as the output buffer.

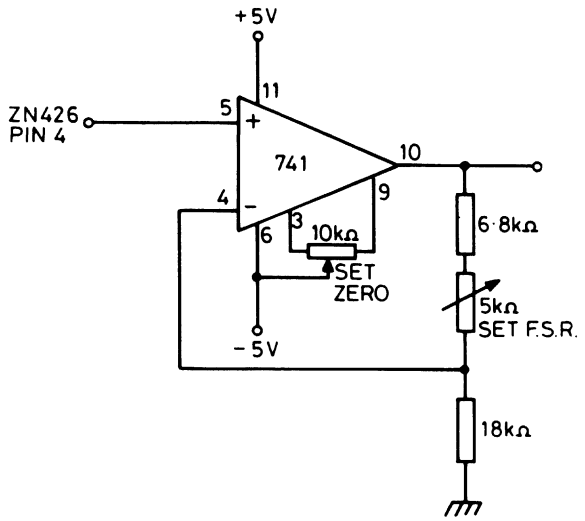


Fig.4 The 741 as output buffer

PLESSEY
Semiconductors

ZN427E-8/ZN427J-8/ZN427D

MICROPROCESSOR COMPATIBLE 8-BIT SUCCESSIVE APPROXIMATION A-D CONVERTER

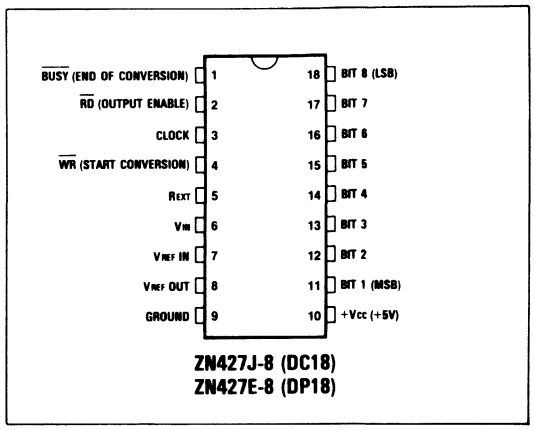
The ZN427 is an 8-bit successive approximation converter with three-state outputs to permit easy interfacing to a common data bus. The IC contains a voltage switching DAC, a fast comparator, successive approximation logic and a 2.56V precision bandgap reference, the use of which is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted, thus allowing ratiometric operation.

Only passive external components are required for operation of the converter.

Insert FEATURES

FEATURES

- Easy Interfacing to Microprocessor, or Operates as a 'Stand-Alone' Converter
- Fast: 10 microseconds Conversion Time Guaranteed
- No Missing Codes over Operating Temperature Range
- Data Outputs Three-State TTL Compatible, other Logic Inputs and Outputs TTL and CMOS Compatible
- Choice of On-Chip or External Voltage Reference
- Ratiometric Operation
- Unipolar and Bipolar Input Ranges
- Complementary to ZN428 DAC
- Commerical or Military Temperature Ranges



Pin connections - top view

ORDERING INFORMATION

Device type	Operating temperature	Package
ZN427D	0°C to +70°C	MP18
ZN427E-8	0°C to +70°C	DP18
ZN427J-8	-55°C to +125°C	DC18

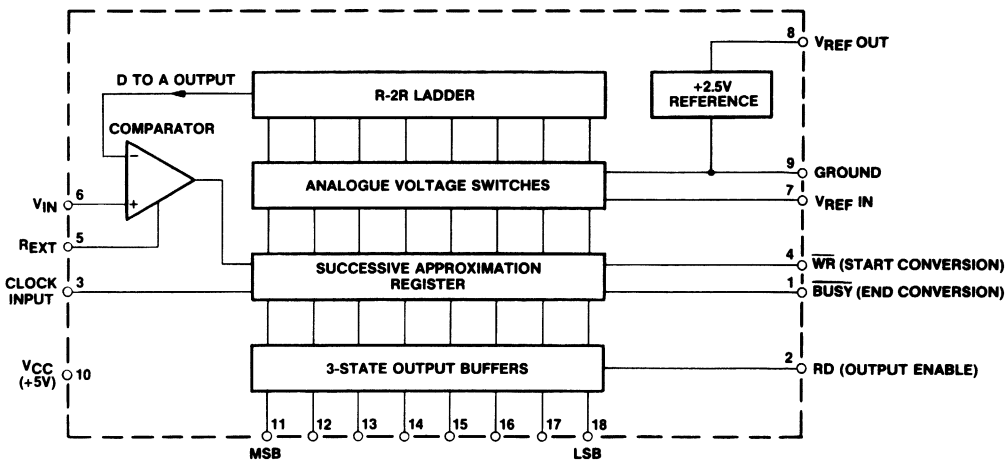


Fig.1 System diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	+7.0V
Max. voltage, logic and V_{REF} inputs	$+V_{CC}$
Operating temperature range	0°C to 70°C (ZN427E-8, ZN427D)
	-55°C to +125°C (ZN427J-8)
Storage temperature range	-55°C to +125°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_{amb} = 25°C unless otherwise specified).

Parameter	Min.	Typ.	Max.	Units	Conditions
Converter					
Resolution	8	–	–	Bits	
Linearity error	–	–	±0.5	LSB	
Differential non-linearity	–	±0.5	–	LSB	
Linearity error T.C.	–	±3	–	ppm/°C	
Differential non-linearity T.C.	–	±6	–	ppm/°C	
Full-scale (gain) T.C.	–	±2.5	–	ppm/°C	External Ref. 2.5V
Zero T.C.	–	±8	–	μV/°C	
Zero transition 00000000 to 00000001	12	15	18	mV	$V_{REF\ IN}$ = 2.560V
F.S. transition 11111110 to 11111111	2.545	2.550	2.555	V	$V_{REF\ IN}$ = 2.560V
Conversion time	–	–	10	μs	See note 1
External reference voltage	1.5	–	3.0	V	
Supply voltage (V_{CC})	4.5	–	5.5	V	
Supply current	–	25	40	mA	
Power consumption	–	125	–	mW	
Comparator					
Input current	–	1	–	μA	V_{IN} = 3V, R_{EXT} = 82kΩ
Input resistance	–	100	–	kΩ	V_- = −5V
Tail current, I_{EXT}	25	–	150	μA	
Negative supply, V−	−3.0	–	−30.0	V	See comparator
Input voltage	−0.5	–	3.5	V	(page 2-26)
Internal voltage reference					
Output voltage	2.475	2.560	2.625	V	R_{REF} = 390Ω, C_{REF} = 4μ7
Slope resistance	–	0.5	2	Ω	
V_{REF} temperature coefficient	–	50	–	ppm/°C	
Reference current	4	–	15	mA	See reference (page 2-25)

ELECTRICAL CHARACTERISTICS (Cont.)

	Min.	Typ.	Max.	Units	Conditions
Logic (over specified operating temperature range)					
High level input voltage V_{IH}	2.0	–	–	V	
Low level input voltage V_{IL}	–	–	0.8	V	
High level input current,	–	–	50	μA	$V_{IN} = 5.5V$, $V_{CC} = max.$
$\overline{WR}$ and RD inputs I_{IH}	–	–	15	μA	$V_{IN} = 2.4V$, $V_{CC} = max.$
High level input current,	–	–	100	μA	$V_{IN} = 5.5V$, $V_{CC} = max.$
Clock input I_{IH}	–	–	30	μA	$V_{IN} = 2.4V$, $V_{CC} = max.$
Low level input current I_{IL}	–	–	−5	μA	$V_{IN} = 0.4V$, $V_{CC} = max.$
High level output current I_{OL}	–	–	−100	μA	
Low level output current I_{OL}	–	–	1.6	mA	
High level output voltage V_{OH}	2.4	–	–	V	$I_{OH} = max.$, $V_{CC} = min.$
Low level output voltage V_{OL}	–	–	0.4	V	$I_{OL} = max.$, $V_{CC} = min.$
Disabled output leakage	–	–	2	μA	$V_O = 2.4V$
Input clamp diode voltage	–	–	−1.5	V	
Read input to data output	–	–	250	ns	See Fig. 8
Enable/disable delay time t_{RD}	–	180	250	ns	
Start pulse width t_{WR}	250	160	–	ns	See Fig. 8
$\overline{WR}$ to $\overline{BUSY}$ propagation delay t_{BD}	–	–	250	ns	
Clock pulse width	500	–	–	ns	
Maximum clock frequency	900	1000	–	kHz	See note 1

Note 1 A 900kHz clock gives a conversion time of 10μs (9 clock periods).

GENERAL CIRCUIT OPERATION

The ZN427 utilises the successive approximation technique. Upon receipt of a negative-going pulse at the $\overline{WR}$ input the $\overline{BUSY}$ output goes low, the MSB is set to 1 and all other bits are set to 0, which produces an output voltage of $V_{REF}/2$ from the DAC. This is compared to the input voltage V_{IN}; a decision is made on the next negative clock edge to reset the MSB to 0 if $\frac{V_{REF}}{2} > V_{IN}$ or leave it set to 1 if $\frac{V_{REF}}{2} < V_{IN}$. Bit 2 is set to 1 on the same clock edge, producing an output from the DAC of $\frac{V_{REF}}{4}$ or $\frac{V_{REF}}{2} + \frac{V_{REF}}{4}$ depending on the state of the MSB. This voltage is compared to V_{IN} and on the next clock edge a decision is made regarding bit 2, whilst bit 3 is set to 1. This procedure is repeated for all eight bits. On the ninth negative clock edge $\overline{BUSY}$ goes high indicating that the conversion is complete.

During a conversion the RD input will normally be held low to keep the three-state buffers in their high impedance state. Data can be read out by taking RD high, thus enabling the three-state outputs. Readout is non-destructive. The $\overline{BUSY}$ output may be tied to the RD input to automatically enable the outputs when the data is valid.

For reliable operation of the converter the start pulse applied to the $\overline{WR}$ input must meet certain timing criteria with respect to the converter clock. These are detailed in the timing diagram of Fig. 2.

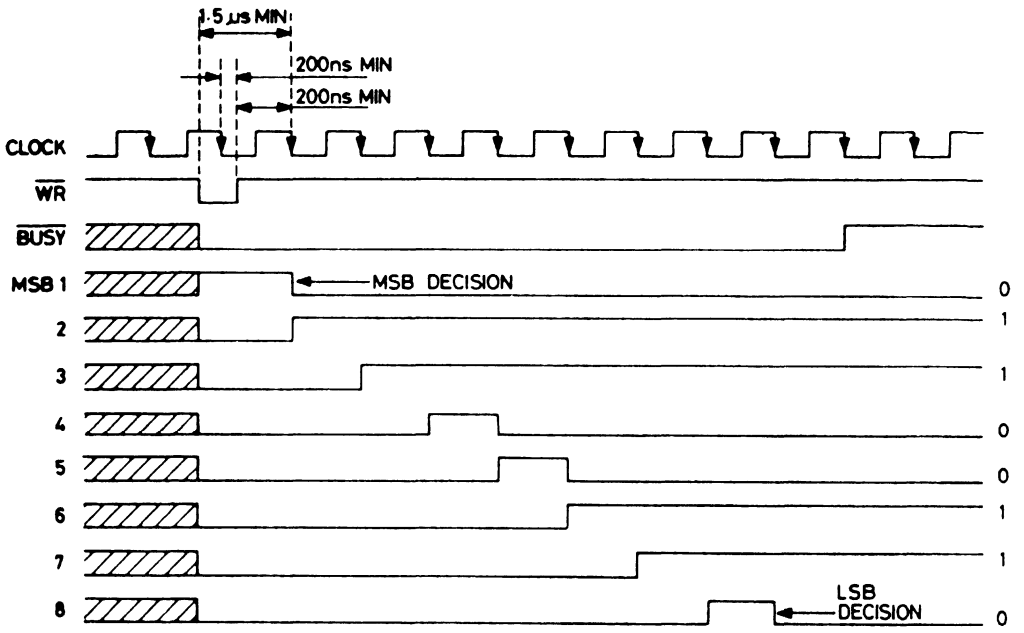


Fig. 2 Timing diagram

NOTES ON TIMING DIAGRAM

1. A conversion sequence is shown for the digital word 01100110. For clarity the three-state outputs are shown as being enabled during the conversion, but normal practice would be to disable them until the conversion was complete.

2. The $\overline{BUSY}$ output goes low during a conversion. When $\overline{BUSY}$ goes high at the end of a conversion the output data is valid. In a microprocessor system the $\overline{BUSY}$ output can be used to generate an interrupt request when the conversion is complete.

3. In the timing diagram cross hatching indicates a 'don't care' condition.

4. The start pulse operates as an asynchronous (independent of clock) reset that sets the MSB output to 1 and sets all other outputs and the end of conversion flag to 0. This resetting occurs on the low-going edge of the start pulse and as long as $\overline{WR}$ is low the converter is inhibited. Conversion commences on the first active (negative going) clock edge after the $\overline{WR}$ input has gone high again, when the MSB decision is made. A number of timing constraints thus apply to the start pulse.

(a) The minimum duration of the start pulse is 250ns, to allow reliable resetting of the converter logic circuits.

(b) There is no limit to the maximum duration of the start pulse.

(c) To allow the MSB to settle at least 1.5μs must elapse between the negative going edge of the start pulse and the first active clock edge that indicates the MSB desicion.

(d) To ensure reliable clocking the positive-going edge of the start pulse should not occur within 200ns of an active (negative-going) clock edge. The ideal place for the positive-going edge of the start pulse is coincident with a positive-going clock edge. As a special case of the above conditions the start pulse may be synchronous with a negative-going clock pulse.

PRACTICAL CLOCK AND SYNCHRONISING CIRCUITS

The actual method of generating the clock signal and synchronising it to the start conversion pulse (or vice versa) will depend on the system in which the ZN427 is incorporated.

When used with a microprocessor the ZN427 can be treated as RAM and can be assigned a memory address using an address decoder. If the μP clock is used to drive the ZN427 and the μP write pulse meets the ZN427 timing criteria with respect to the μP clock then generating the start pulse is simply a matter of gating the decoded address with the microprocessor write pulse. Whilst the conversion is being performed the microprocessor can perform other instructions or No operation (NOP). When the conversion is complete the outputs can be enabled onto the bus by gating the decoded address with the read pulse. A timing diagram for this sequence of operation is given in Fig. 3.

An advantage of using the microprocessor clock is that the conversion time is known precisely in terms of machine cycles. The data outputs may therefore be read after a fixed delay of at least nine clock cycles after the end of the $\overline{WR}$ pulse, when the conversion will be complete.

Alternatively the read operation may be initiated by using the $\overline{BUSY}$ output to generate an interrupt request.

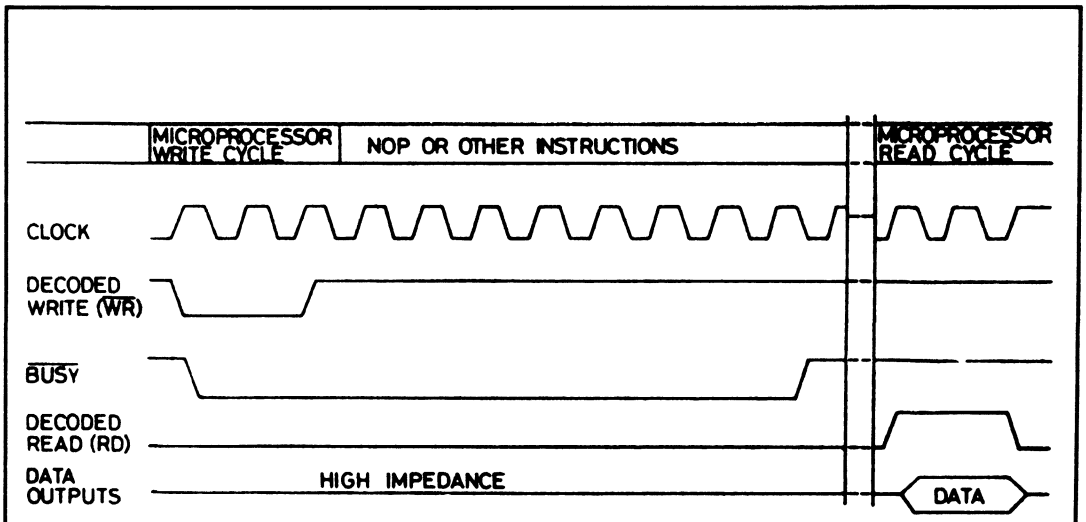


Fig. 3 Typical timing diagram using μP clock and write pulse

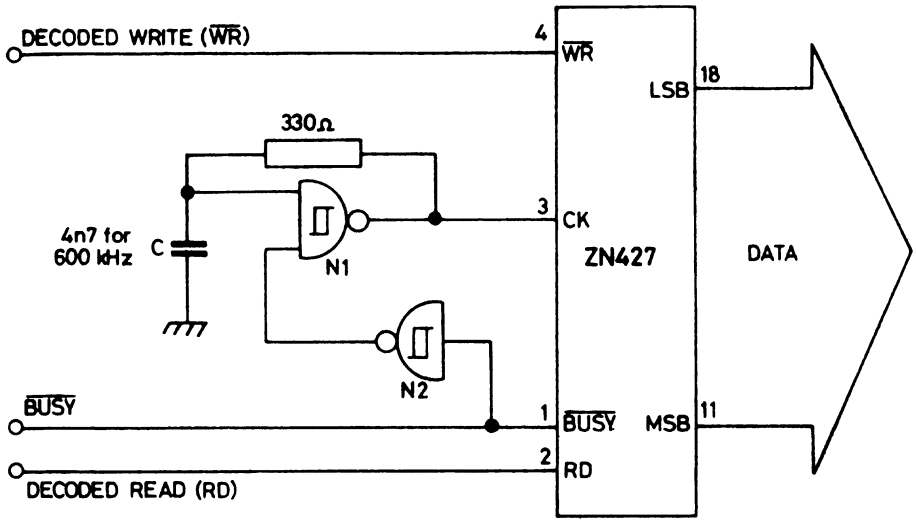
In some systems, for example single-chip microcomputers such as the 8048, this simple method may not be feasible for one or more of the following reasons:

(a) The MPU clock is not available externally.

(b) The clock frequency is too high.

(c) The write pulse timing criteria make it unsuitable for direct use as a start conversion pulse.

If any of these conditions apply then the self-synchronising clock circuit of Fig. 4a is recommended.



N1 N2 = 7413 or ½ 74132 Schmitt trigger

$f_{CK} = \frac{1}{360.C}$ (Hz, F)

Fig. 4a Self-synchronising clock circuit

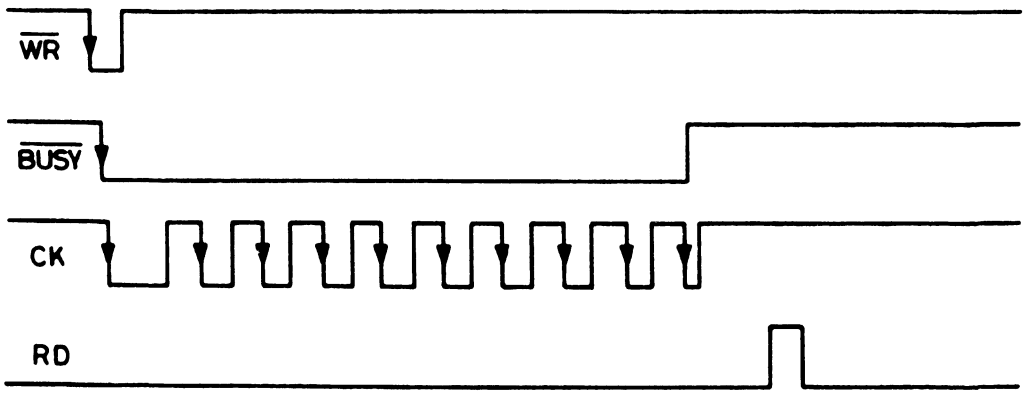


Fig. 4b Timing diagram for circuit of Fig. 4a

N1 is connected as an astable multivibrator which, when the $\overline{\text{BUSY}}$ output is high, is inhibited by the output of N2 holding one of its inputs low. The start conversion pulse resets the $\overline{\text{BUSY}}$ flag and N1 begins to oscillate. When the conversion is complete $\overline{\text{BUSY}}$ goes high and the clock is inhibited.

Since the start pulse starts the clock it may occur at any time. The only constraints on the start pulse are that it must be longer than 250ns but at least 200ns shorter than the first clock pulse. The first clock pulse is in fact longer than the rest since C1 starts from a fully charged condition whereas on subsequent cycles it changes between the upper and lower thresholds (V_{T+} and V_{T-}) of the Schmitt trigger.

LOGIC INPUTS AND OUTPUTS

The logic inputs of the ZN427 utilise the emitter-follower configuration shown in Fig. 5. This gives extremely low input currents for CMOS as well as TTL compatibility.

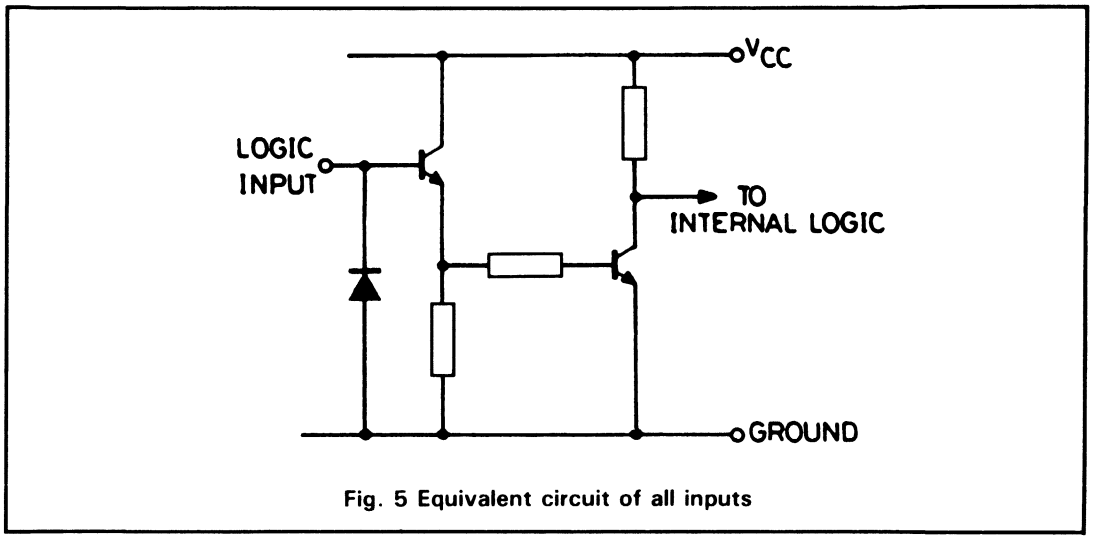
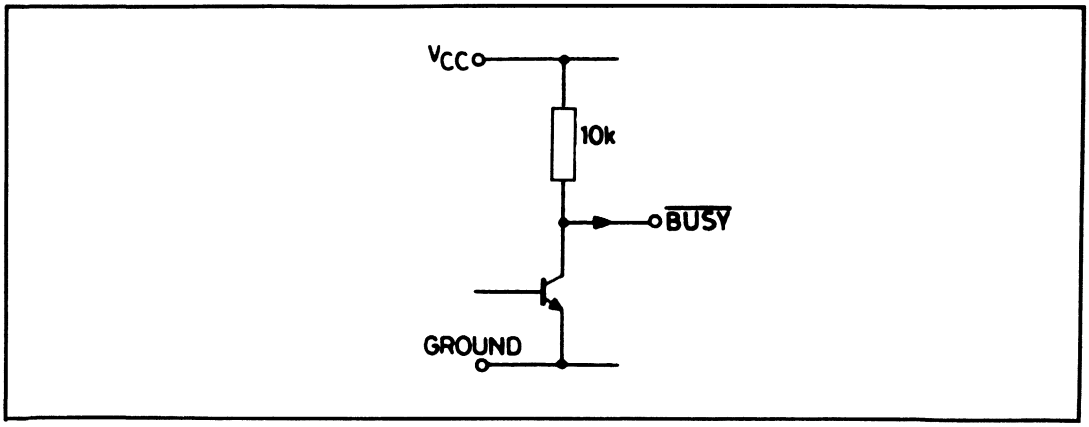


Fig. 5 Equivalent circuit of all inputs

The $\overline{\text{BUSY}}$ output, shown in Fig. 6, utilises a passive pullup for CMOS/TTL compatibility.



The data outputs have three-state buffers, an equivalent circuit of which is shown in Fig. 7. Whilst the RD input is low both output transistors are turned off and the output is in a high impedance state. When RD is high the data output will assume the appropriate logic state (0 or 1).

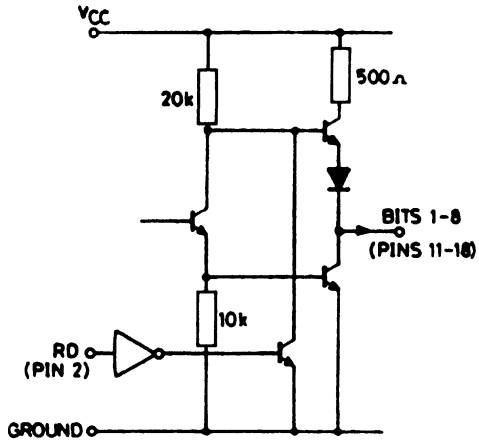


Fig. 7 Equivalent circuit of data outputs

A test circuit and timing diagram for the output enable/disable delays are given in Fig. 8.

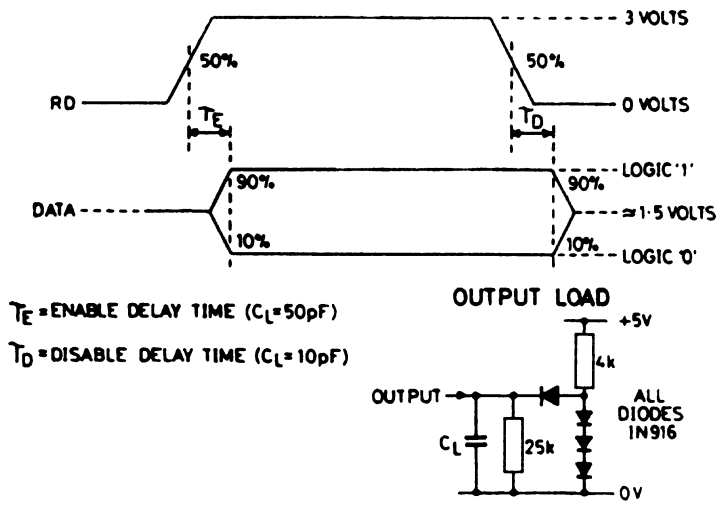


Fig. 8 Output enable/disable waveforms

ANALOGUE CIRCUITS

D-A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 9. Each element is connected to either 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (<1mV).

A binary weighted voltage is produced at the output of the R-2R ladder:

$$\text{D-A output} = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input to the D-A from the successive approximation register.

Vos is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. The value of Vos is typically 2mV for the ZN427E-8 and ZN427D (4mV, ZN427J-8). This offset will normally be removed by the setting up procedure and since the offset temperature coefficient is low (8μV/°C) the effect on accuracy will be negligible.

The D-A output range can be considered to be 8-VREF IN through an output resistance R (4kΩ).

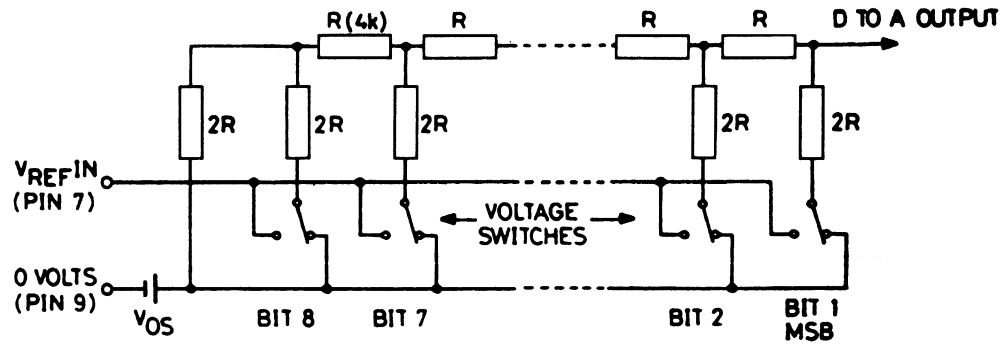


Fig. 9 R-2R ladder network

REFERENCE

(a) Internal reference

The internal reference is an active bandgap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig. 10). A resistor (R_{REF}), should be connected between pins 8 and 10. The recommended value of 390Ω will supply a nominal reference current of (5.0-2.5)/0.39 = 6.4mA. A stabilising/decoupling capacitor C_{REF}(4μ7), is required between pins 8 and 9. For internal reference operation $V_{REF\ OUT}$ (pin 8) is connected to $V_{REF\ IN}$ (pin 7).

Up to five ZN427's may be driven from one internal reference, there being no need to reduce R_{REF}. This useful feature saves power and gives excellent gain tracking between the converters.

Alternatively the internal reference can be used as the reference voltage for other external circuits and can source or sink up to 3mA.

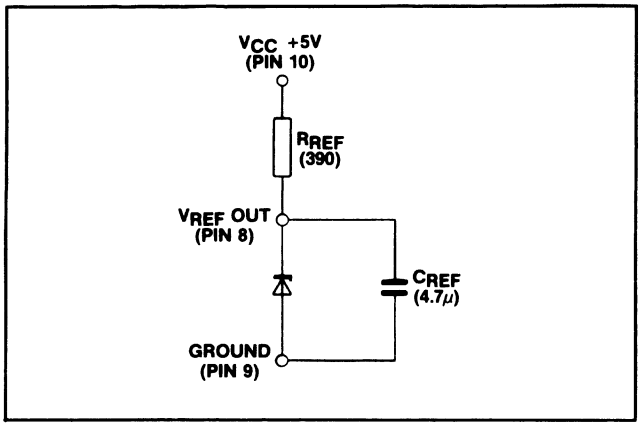


Fig.10 Internal voltage reference

(b) External reference

If required an external reference voltage in the range +1.5 to +3.0V may be connected to $V_{REF\ IN}$. The slope resistance of such a reference source should be less than $\frac{2.5}{n}\ \Omega$, where n is the number of converters supplied.

RATIOMETRIC OPERATION

If the output from a transducer varies with its supply then an external reference for the ZN427 should be derived from the same supply. The external reference can vary from +1.5 to +3.0V. The ZN427 will operate if $V_{REF\ IN}$ is less than +1.5V but reduced overdrive to the comparator will increase its delay and so the conversion time will need to be increased.

COMPARATOR

The ZN427 contains a fast comparator, the equivalent input circuit of which is shown in Fig. 11.

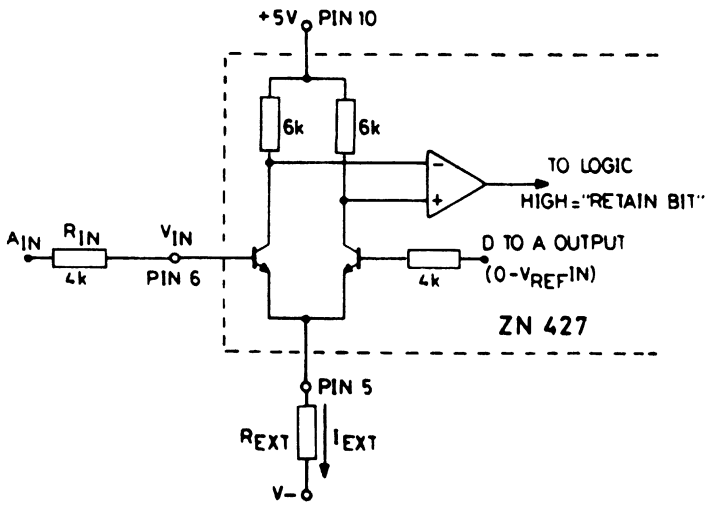


Fig. 11 Comparator equivalent circuit

The comparator derives the tail current, I_{EXT}, for its first stage from an external resistor, R_{EXT}, which is taken to a negative supply V−.

This arrangement allows the ZN427 to work with any negative supply in the range −3 to −30 volts. The ZN427 is designed to be insensitive to changes in I_{EXT} from 25μA to 150μA. The suggested nominal value of I_{EXT} is 65μA and a suitable value for R_{EXT} is given by $R_{EXT} = |V_-|15k\Omega$.

V− (volts)	R_{EXT} (±10%)
−3	47kΩ
−5	82kΩ
−10	150kΩ
−12	180kΩ
−15	220kΩ
−20	330kΩ
−25	390kΩ
−30	470kΩ

The output from the D-A converter is connected through the 4kΩ ladder resistance to one side of the comparator. The analogue input to be converted could be connected directly to the other comparator input (V_{IN}, pin 6) but for optimum stability with temperature the analogue input should be applied through a source resistance ($R_{IN} = 4k\Omega$) to match the ladder resistance.

ANALOGUE INPUT RANGES

The basic connection of the ZN427 shown in Fig. 12 has an analogue input range 0 to $V_{REF\ IN}$, which, in some applications, may be made available from previous signal conditioning/ scaling circuits. Input voltage ranges greater than this are accommodated by providing an attenuator on the comparator input, whilst for smaller input ranges the signal must be amplified to a suitable level.

Bipolar input ranges are accommodated by off-setting the analogue input range so that the comparator always sees a positive input voltage.

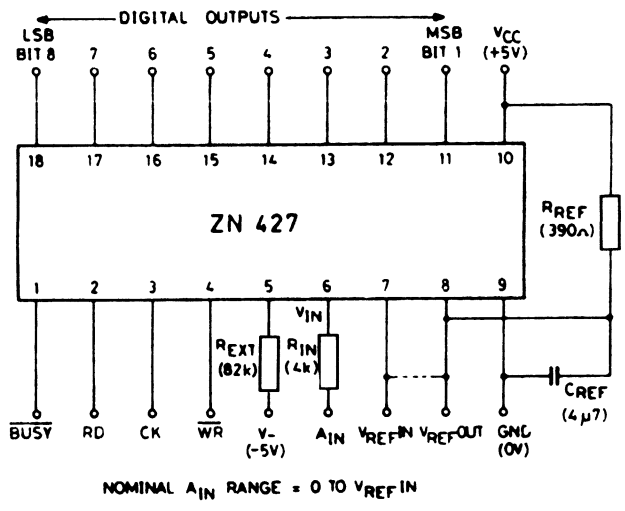


Fig. 12 External components for basic operation

UNIPOLAR OPERATION

The general connection for unipolar operation is shown in Fig. 13.

The values of R_1 and R_2 are chosen so that $V_{IN} = V_{REF\ IN}$ when the Analogue Input (A_{IN}) is at full-scale. The resulting full-scale range is given by

$$A_{IN}\ FS = \left(1 + \frac{R1}{R2}\right) V_{REF\ IN} = G.V_{REF\ IN}$$

To match the ladder resistance R1//R2 ($\approx R_{IN}$) = 4kΩ.

The required nominal values of R_1 and R_2 are given by $R_1 = 4G$ kΩ, $R_2 = \frac{4G}{G-1}$ kΩ

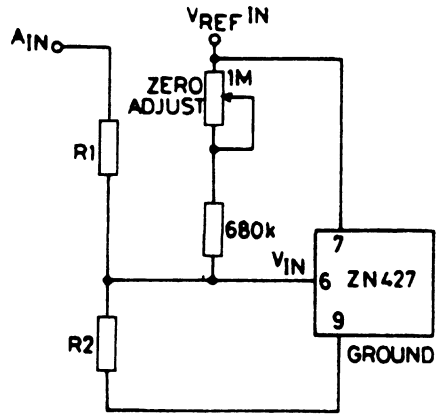


Fig. 13 Unipolar operation - general connection

Using these relationships a table of nominal values of R_1 and R_2 can be constructed for $V_{REF\ IN} = 2.5$ volts.

Input range	G	R_1	R_2
+ 5V	2	8kΩ	8kΩ
+ 10V	4	16kΩ	5.33kΩ

GAIN ADJUSTMENT

Due to tolerances in R_1 and R_2, tolerances in V_{REF} and the gain (full-scale) error of the DAC, some adjustment should be incorporated into R_1 to calibrate the full-scale of the converter. When used with the internal reference and 2% resistors a preset capable of adjusting R_1 by at least + 5% of its nominal value is suggested.

ZERO ADJUSTMENT

Due to offsets in the DAC and comparator the zero (0 to 1) code transition would occur with typically 15mV applied to the comparator input, which corresponds to + 1½LSB with a 2.56V reference.

Zero adjustment must therefore be provided to set the zero transition to its correct value of + ½LSB or 5mV with a 2.56V reference. This is achieved by applying an adjustable positive offset to the comparator input via P2 and R3. The values shown are suitable for all input ranges greater than 1½ times $V_{REF\ IN}$.

Practical circuit values for + 5 and + 10V input ranges are given in Fig. 14, which incorporate both zero and gain adjustments.

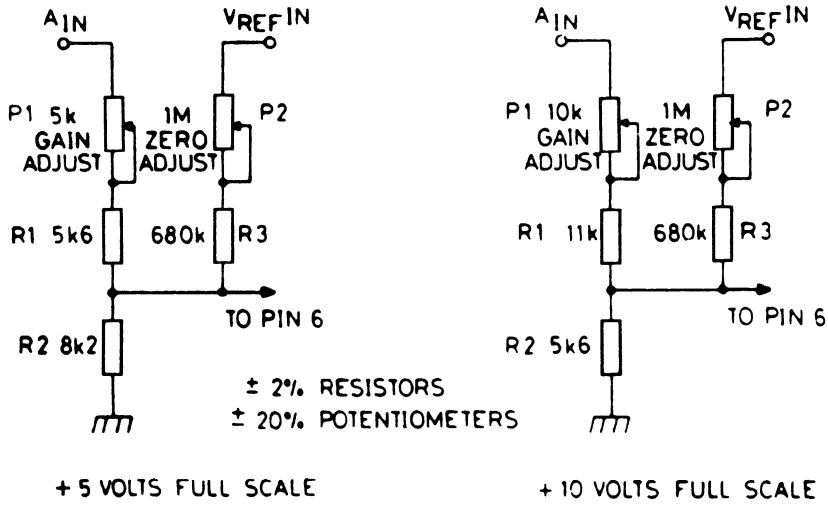


Fig. 14 Unipolar operation - component values

UNIPOLAR ADJUSTMENT PROCEDURE

(i) Apply continuous SC pulses at intervals long enough to allow complete conversion and monitor the digital outputs.

(ii) Apply full-scale minus 1½LSB to A_{IN} and adjust gain until bit 8 (LSB) output just flickers between 0 and 1 with all other bits at 1.

(iii) Apply ½LSB to A_{IN} and adjust zero until bit 8 just flickers between 0 and 1 with all other bits at 0.

UNIPOLAR SETTING UP POINTS

Input range, +FS	½LSB	FS - 1½LSB
+ 5V	9.8mV	4.9707V
+ 10V	19.5mV	9.9414V

$$1LSB = \frac{FS}{256}$$

UNIPOLAR LOGIC CODING

Analogue input (A_{IN}) (Nominal code centre value)	Output code (Binary)
FS - 1LSB	11111111
FS - 2LSB	11111110
¾FS	11000000
½ FS + 1LSB	10000001
½FS	10000000
½FS - 1LSB	01111111
¼FS	01000000
1LSB	00000001
0	00000000

BIPOLAR OPERATION

For bipolar operation the input to the ZN427 is offset by half full-scale by connecting a resistor R_3 between $V_{REF\ IN}$ and V_{IN} (Fig. 15).

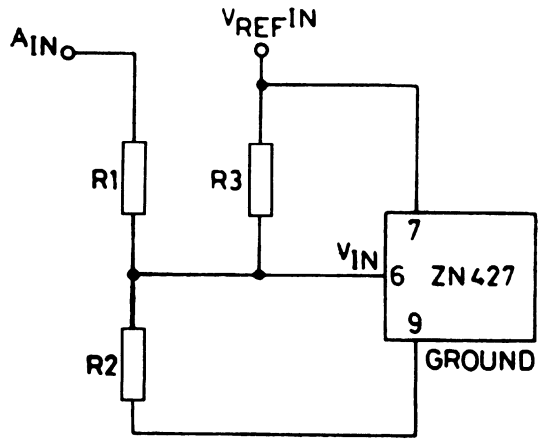


Fig. 15 Bipolar operation - general connection

When $A_{IN} = -FS$, V_{IN} needs to be equal to zero.

When $A_{IN} = +FS$, V_{IN} needs to be equal to $V_{REF\ IN}$.

If full-scale range is $\pm G$. $V_{REF\ IN}$ then $R_1 = (G - 1)$. R_2 and $R_1 = G$. R_3 fulfil the required conditions.

To match the ladder resistance, $R_1/R_2/R_3$ $(= R_{IN}) = 4k\Omega$.

Thus the nominal values of R_1, R_2, R_3 are given by $R_1 = 8\ Gk\Omega$, $R_2 = 8G/(G - 1)k\Omega$, $R_3 = 8k\Omega$.

A bipolar range of $\pm V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $+V_{REF\ IN}$) results if $R_1 = R_3 = 8k\Omega$ and $R_2 = \infty$.

Assuming that $V_{REF\ IN} = 2.5$ volts the nominal values of resistors for ± 5 and $\pm 10V$ input ranges are given in the following table.

Input range	G	R_1	R_2	R_3
±5V	2	16kΩ	16kΩ	8kΩ
±10V	4	32kΩ	10.66kΩ	8kΩ

Minus full-scale (offset) is set by adjusting R_1 about its nominal value relative to R_3. Plus full-scale (gain) is set by adjusting R_2 relative to R_1.

Practical circuit realisations are given in Fig. 16.

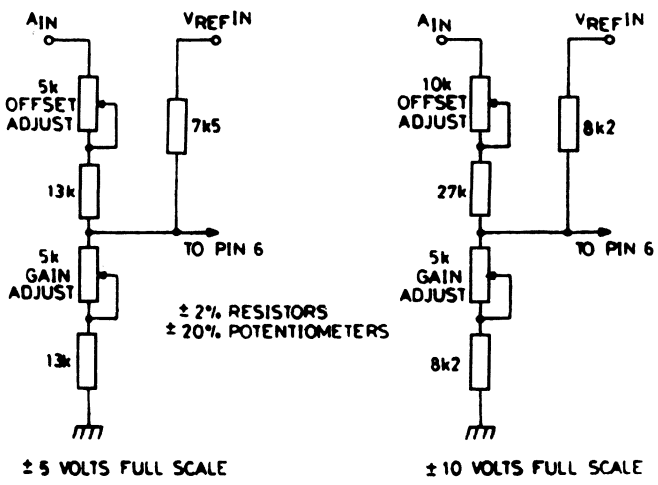


Fig. 16 Bipolar operation - component values

Note that in the ±5V case R_3 has been chosen as 7.5kΩ (instead of 8.2kΩ) to get a more symmetrical range of adjustment using standard potentiometers.

BIPOLAR ADJUSTMENT PROCEDURE

(i) Apply continuous SC pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

(ii) Apply −(FS - ½LSB) to A_{IN} and adjust offset until the bit 8 (LSB) output just flickers between 0 and 1 with all other bits at 0.

(iii) Apply +(FS - 1½LSB) to A_{IN} and adjust gain until bit 8 just flickers between 0 and 1 with all other bits at 1.

(iv) Repeat step (ii).

BIPOLAR SETTING-UP POINTS

Input range, ±FS	−(FS − ½LSB)	+(FS − 1½LSB)
±5V	−4.9805V	+4.9414V
±10V	−9.9609V	+9.8828V

$$1LSB = \frac{2FS}{265}$$

BIPOLAR LOGIC CODING

Analogue input (A_{IN}) (Nominal code centre value)	Output code (Offset binary)
+ (FS - 1LSB)	11111111
+ (FS - 2LSB)	11111110
+ ½FS	11000000
+ 1LSB	10000001
0	10000000
- 1LSB	01111111
- ½FS	01000000
- (FS - 1LSB)	00000001
- FS	00000000

SINGLE 5V SUPPLY RAIL OPERATION

The ZN427 takes very little power from the negative rail and so a suitable negative supply can be generated very easily using a 'diode pump' circuit. The circuit shown in Fig. 17 works with any clock frequency from 10kHz to 1MHz and can supply up to five ZN427's.

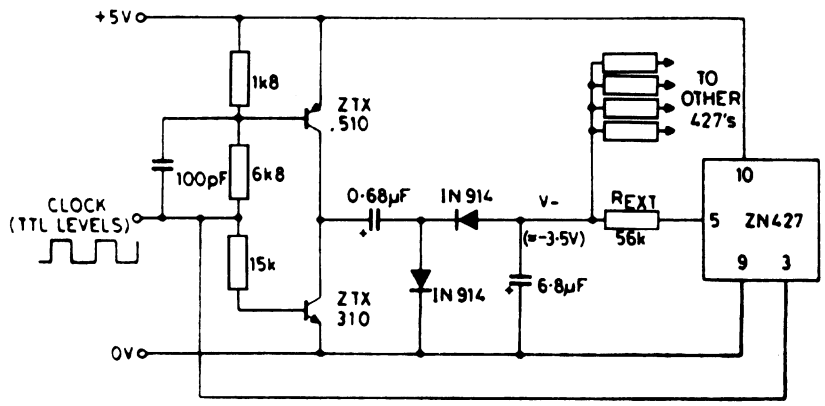


Fig. 17 Single 5V supply operation

PLESSEY
Semiconductors

ZN428E-8/ZN428J-8/ZN428D

8-BIT LATCHED INPUT D-A CONVERTER

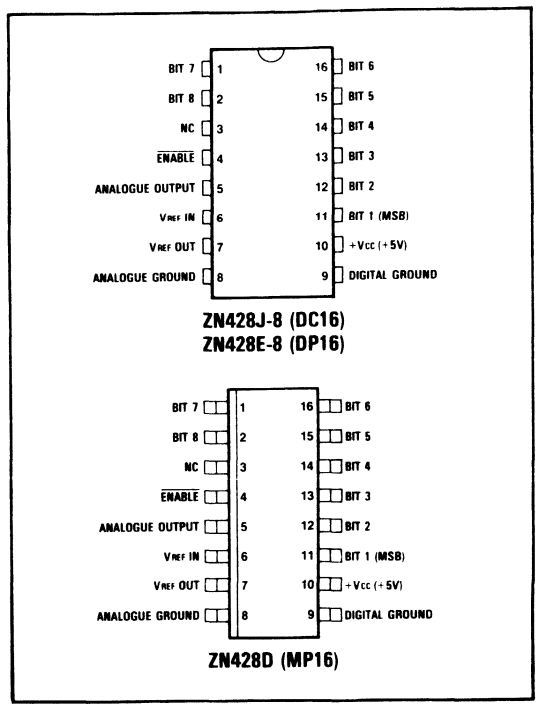
The ZN428 is a monolithic 8-bit D-A converter with input latches to facilitate updating from a data bus. The latch is transparent when enable is LOW and the data is held when enable is taken HIGH. The ZN428 also contains a 2.5V reference the use of which is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.

FEATURES

- Contains DAC with Data Latch and On-Chip Reference
- Guaranteed Monotonic over the Full Operating Temperature Range
- Single +5V Supply
- Microprocessor Compatible
- TTL and 5V CMOS Compatible
- 800ns Settling Time
- Complementary to ZN427 A to D Series
- Commercial or Military Temperature Ranges

ORDERING INFORMATION

Device type	Operating temperature	Package
ZN428D	0°C to +70°C	MP16
ZN428E-8	0°C to +70°C	DP16
ZN428J-8	-55°C to +125°C	DC16



Pin connections - top view

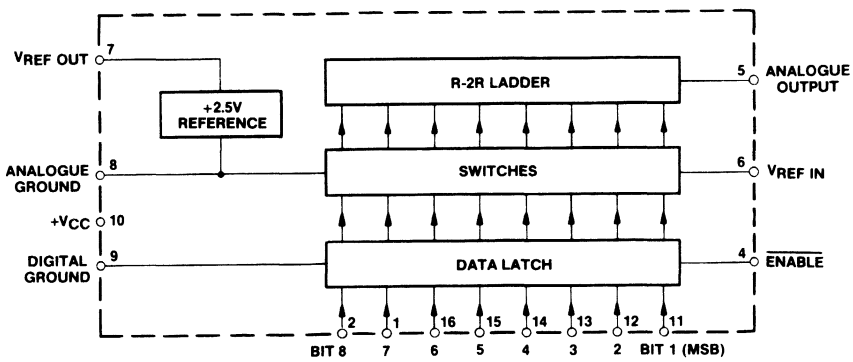


Fig.1 System diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	+7.0V
Max. voltage, logic and V_{REF} inputs	$+V_{CC}$
Operating temperature range	0°C to 70°C (ZN428E-8, ZN428D) -55°C to +125°C (ZN428J-8)
Storage temperature range	-55°C to +125°C
Analogue ground to digital ground	±200mV

ELECTRICAL CHARACTERISTICS (V_{CC} = +5V, T_{amb} = 25°C unless otherwise specified).

Parameter	Min.	Typ.	Max.	Units	Conditions
Internal voltage Reference					
Output voltage	2.475	2.550	2.625	V	R_{REF} = 390Ω, C_{REF} = 1μF
Slope resistance		0.5	2	Ω	
$V_{REF\ OUT}$ T.C.		50		ppm/°C	
Reference current	4		15	mA	Note 1
D-A converter					
Linearity error			±0.5	LSB	2.0V ≤ $V_{REF\ IN}$ ≤ 3.0V
Differential non-linearity		±0.5		LSB	
Linearity error T.C.		±3		ppm/°C	
Differential non-linearity T.C.		±6		ppm/°C	
Offset voltage		2	5	mV	All bits OFF
Offset voltage T.C.		±6		μV/°C	
Full scale output	2.545	2.550	2.555		External reference $V_{REF\ IN}$ = 2.560V, all bits ON
Full scale output T.C.		2		ppm/°C	
Analogue output resistance		4		kΩ	
External reference voltage	0		3.0	V	
Settling time to 0.5 LSB		800		ns	1 LSB major transition (note 2)
		1.25		μs	All bits ON to OFF or OFF to ON (note 2)
Operating temperature range:					
ZN428D and ZN428E-8	0		70	C	
ZN428J-8	-55		125	C	
Supply voltage (V_{CC})	4.5	5.0	5.5	V	

Note 1 See REFERENCE

Note 2 R_L = 10MΩ, C_L = 10pF

ELECTRICAL CHARACTERISTICS (cont.)

Parameter	Min.	Typ.	Max.	Units	Conditions
Supply current		20	30	mA	Note 3
Power consumption		100		mW	
Logic (over specified operating temperature range)					
High level input voltage	2.0			V	
Low level input voltage			0.8	V	
High level input current			60	μA	$V_{IN} = 5.5V$, $V_{CC} = Max.$
			20	μA	$V_{IN} = 2.4V$, $V_{CC} = Max.$
Low level input current			−5	μA	$V_{IN} = 0.4V$, $V_{CC} = Max.$
Input clamp diode voltage		−1.5		V	$I_{IN} = -8mA$
Enable pulse width	100			ns	
Data set-up time	150			ns	Note 4
Data hold time	10			ns	Note 5

Note 3 All inputs HIGH ($V_{IH} = 3.5V$)

Note 4 Set up time before $\overline{\text{enable}}$ goes high

Note 5 Hold time after $\overline{\text{enable}}$ goes high

D-A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 2. Each 2R element is connected to 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (< 1mV). A binary weighted voltage is produced at the output of the R-2R ladder.

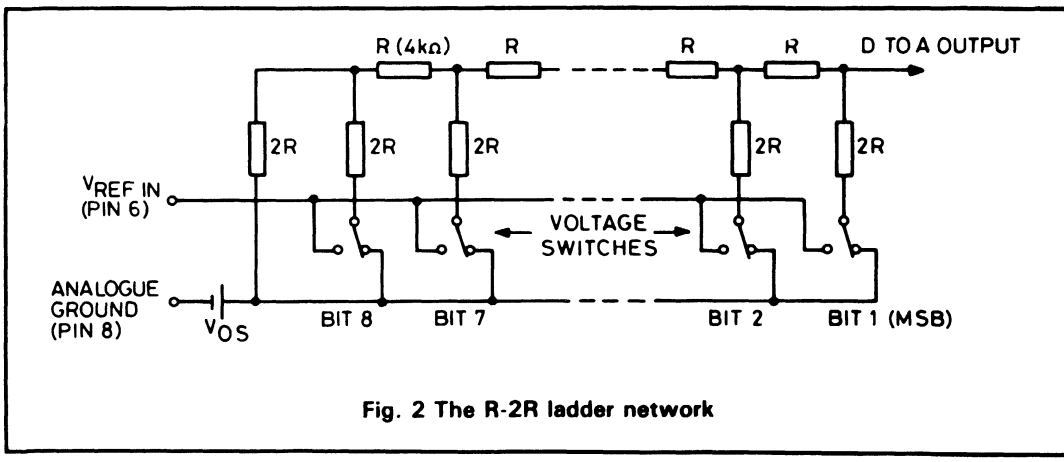


Fig. 2 The R-2R ladder network

Analogue output $= \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$

where n is the digital input to the D-A from the data latch.

V_{OS} is a small offset voltage produced by the D-A switch currents flowing through the package lead resistance. The value of V_{OS} is typically 1mV. This offset will normally be removed by the setting up procedure (see Operating Notes) and because the offset temperature coefficient is low ($\pm 6\mu V/°C$) the effect on accuracy is negligible.

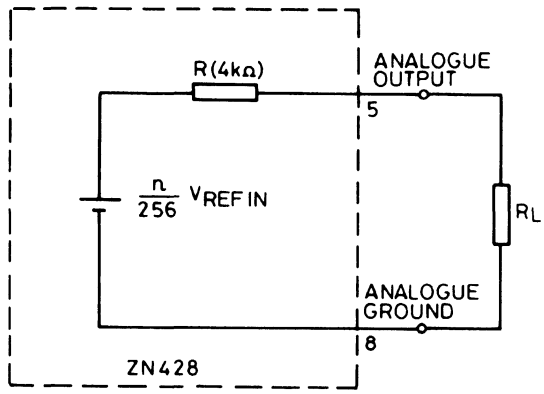


Fig. 3 Analogue output equivalent circuit

Fig. 3 shows an equivalent circuit of the output (ignoring V_{OS}). The output resistance R has a temperature coefficient of +0.2% per °C.

The gain drift due to this is $\frac{0.2R}{R+R_L}$ % per °C

R_L should be chosen as large as possible to make the gain drift small. As an example if R_L = 400kΩ then the gain drift due to the T.C. of R for a 100°C change in ambient temperature will be less than 0.2%. Alternatively the ZN428 can be buffered by an amplifier (see Operating Notes).

REFERENCE

(a) Internal reference

The internal reference is an active bandgap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig. 4). A resistor (R_{REF}), should be connected between $+V_{CC}$ (pin 10) and pin 7. The recommended value of 390Ω will supply a nominal reference current of (5.0-2.5)/0.39 = 6.4mA. A stabilising/decoupling capacitor $C_{REF} = 1\mu F$ is required between pins 7 and 8 for internal reference option, $V_{REF\ OUT}$ (pin 7) being connected to $V_{REF\ IN}$ (pin 6).

Up to five ZN428's may be driven from one internal reference (there is no need to reduce R_{REF}). This useful feature saves power and gives excellent gain tracking between the converters.

(b) External reference

If required an external reference voltage may be connected to $V_{REF\ IN}$. The slope resistance of such a reference source should be less than $\frac{2.5}{n}$ Ω, where n is the number of converters supplied.

$V_{REF\ IN}$ can be varied from 0 to +3V for ratiometric operation. The ZN428 is guaranteed monotonic for $V_{REF\ IN}$ above 2V.

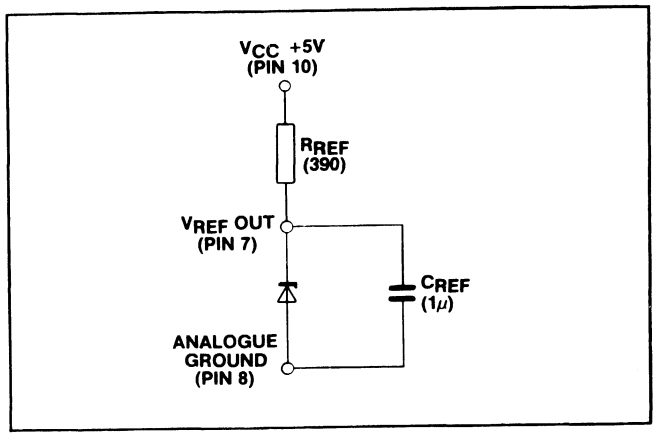


Fig.4 Internal voltage reference

LOGIC

Input coding is binary for unipolar operation and offset binary for bipolar operation. When the enable input is low the data inputs drive the D to A directly. When enable goes high the input data word is held in the data latch.

The equivalent circuit for the data and clock inputs is shown in Fig. 5.

The ZN428 is provided with separate analogue and digital ground connections. The circuit will operate correctly with as much as ±200mV between the two grounds.

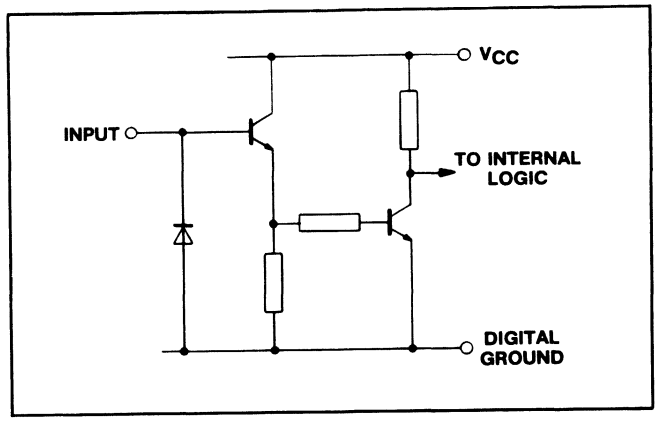


Fig.5 Equivalent circuit of all inputs

OPERATING NOTES

(1) Unipolar D-A converter

The nominal output range of the ZN428 is 0 to $V_{REF\ IN}$ through a 4kΩ resistance. Other output ranges can readily be obtained by using an external amplifier.

The general scheme (Fig. 6) is suitable for amplifiers with input bias currents less than 1.5μA.

The resulting full-scale range is given by

$$V_{OUT}\ FS = \left(1 + \frac{R1}{R2}\right) V_{REF\ IN} = G.V_{REF\ IN}$$

The impedance at the inverting input is R1//R2 and for low drift with temperature this parallel combination should be equal to the ladder resistance (4kΩ). The required nominal values of R1 and R2 are given by $R1 = 4GkΩ$ and $R_2 = 4G/(G-1)kΩ$.

Using these relationships a table of nominal resistance values for R_1 and R_2 can be constructed for $V_{REF\ IN} = 2.5V$.

Output range	G	R_1	R_2
+5V	2	8kΩ	8kΩ
+10V	4	16kΩ	5.33kΩ

For gain setting R_1 is adjusted about its nominal value. Practical circuit realisations (including amplifier stabilising components) for +5 and +10V output ranges are given in Fig. 7. Settling time for a major transistion is 1.5μs typical.

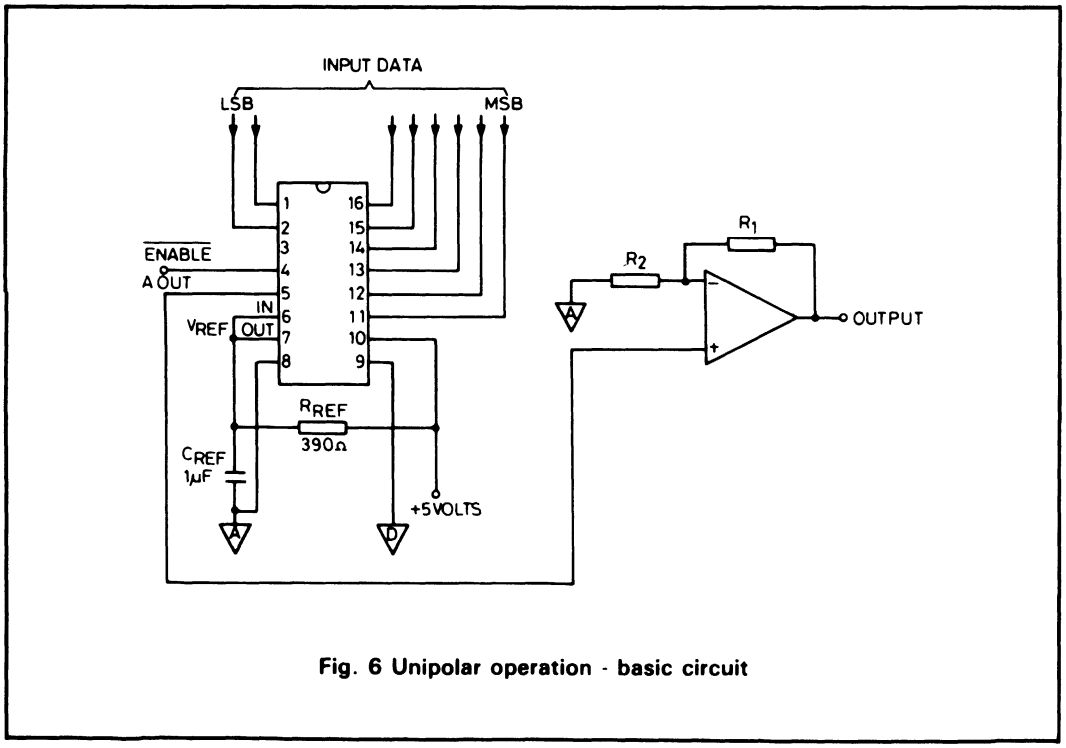


Fig. 6 Unipolar operation - basic circuit

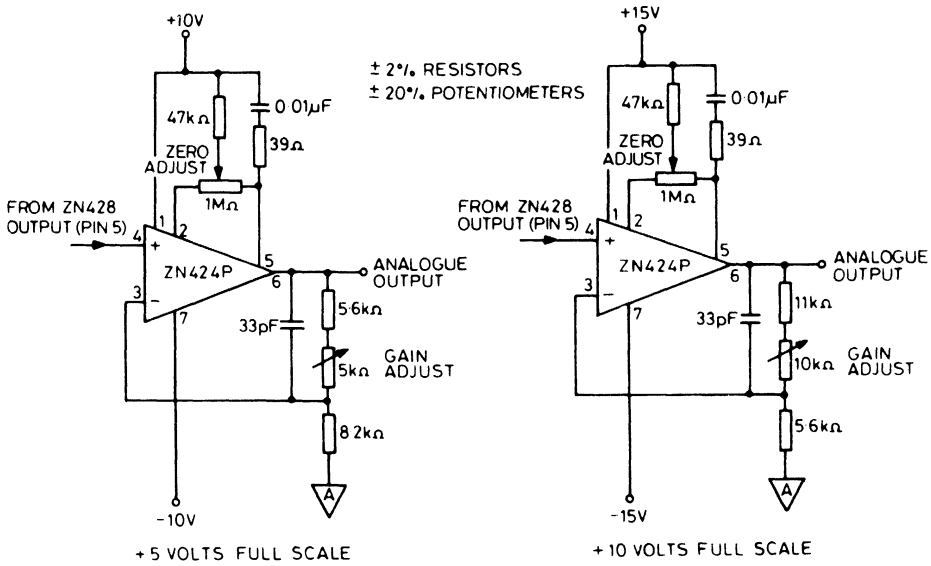


Fig. 7 Unipolar operation - component values

UNIPOLAR ADJUSTMENT PROCEDURE

(i) Set all bits to OFF (low) with $\overline{\text{enable}}$ low and adjust zero until $V_{OUT} = 0.0000V$.

(ii) Set all bits ON (high) and adjust gain until $V_{OUT} = FS - 1LSB$.

UNIPOLAR SETTING UP POINTS

Output range, +FS	LSB	FS - 1LSB
+5V	19.5mV	4.9805V
+10V	39.1mV	9.9609V

$$1LSB = \frac{FS}{256}$$

UNIPOLAR LOGIC CODING

Input code (Binary)	Analogue output (Nominal value)
11111111	FS - 1LSB
11111110	FS - 2LSB
11000000	¾ FS
10000001	½FS + 1LSB
10000000	½FS
01111111	½FS - 1LSB
01000000	¼FS
00000001	1LSB
00000000	0

(2) Bipolar D-A Converter

For bipolar operation the output from the ZN428 is offset by half full scale by connecting a resistor R_3 between $V_{REF\ IN}$ and the inverting input of the buffer amplifier (Fig. 8).

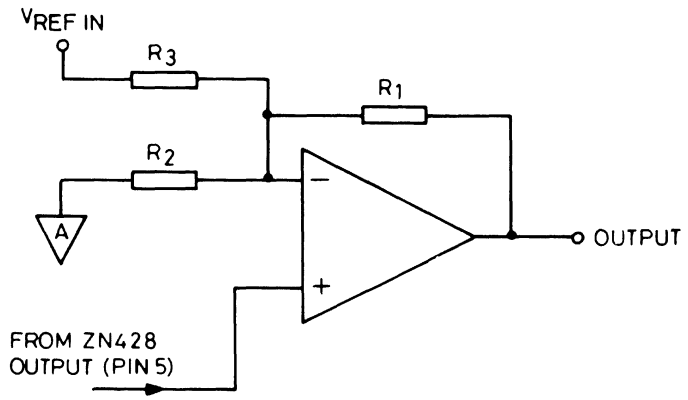


Fig. 8 Bipolar operation - basic circuit

When the digital input to the ZN428 is zero the analogue output is zero and the amplifier output should be −Full scale. An input of all ones to the D-A will give a ZN428 output of $V_{REF\ IN}$ and the amplifier output required is +Full-scale. Also, to match the ladder resistance the parallel combination of R_1, R_2 and R_3 should be 4kΩ.

The nominal values of R_1, R_2 and R_3 which meet these conditions are given by

$R_1 = 8Gk\Omega$, $R_2 = 8G/(G-1)k\Omega$ and $R_3 = 8k\Omega$

where the resultant output range is $\pm G\ V_{REF\ IN}$.

A bipolar output range of $\pm V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $V_{REF\ IN}$) is obtained if $R_1 = R_3 = 8k\Omega$ and $R_2 = \infty$.

Assuming that $V_{REF\ IN} = 2.5V$ the nominal values of resistors for ±5 and ±10V output ranges are given in the following table:

Output Range	G	R_1	R_2	R_3
±5V	2	16kΩ	16kΩ	8kΩ
±10V	4	32kΩ	10.66kΩ	8kΩ

Minus full scale (offset) is set by adjusting R_1 about its nominal value relative to R_3. Plus full-scale (gain) is set by adjusting R_2 relative to R_1.

Practical circuit realisations are given in Fig. 9.

Note that in the ±5V case R_3 has been chosen as 7.5kΩ (instead of 8.2kΩ) to get a more symmetrical range of adjustment using standard potentiometers. Settling time for a major transition is 1.5μs typical.

BIPOLAR ADJUSTMENT PROCEDURE

(1) Set all bits to OFF (low) with $\overline{\text{enable}}$ low and adjust offset until the amplifier output reads −full-scale.

(2) Set all bits ON (high) and adjust gain until the amplifier output reads +(full-scale − 1LSB).

BIPOLAR SETTING UP POINTS

Input range, ±FS	LSB	−FS	+(FS − 1LSB)
±5V	39.1mV	−5.0000V	+4.9609V
±10V	78.1mV	−10.0000V	+9.9219V

$$1\text{LSB} = \frac{2\text{FS}}{256}$$

BIPOLAR LOGIC CODING

Input code (Offset binary)	Analogue output (Nominal value)
11111111	+(FS − 1LSB)
11111110	+(FS − 2LSB)
11000000	+½FS
10000001	+1LSB
10000000	0
01111111	−1LSB
01000000	−½FS
00000001	−(FS − 1LSB)
00000000	−FS

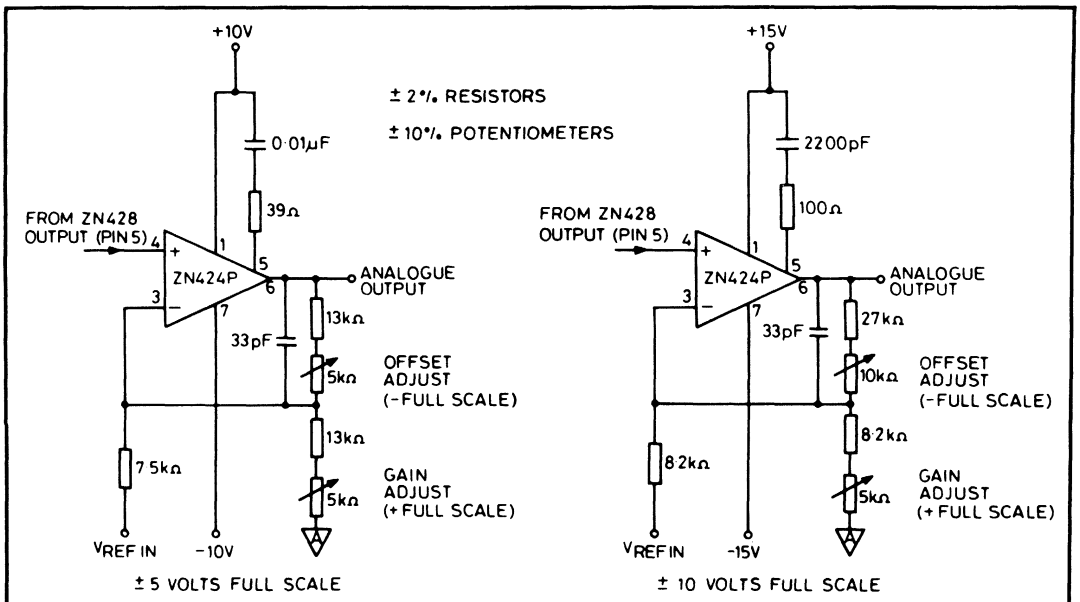


Fig. 9 Bipolar operation - component values

PLESSEY
Semiconductors

ZN429E-8/ZN429J-8/ZN429D

LOW COST 8-BIT D-A CONVERTER

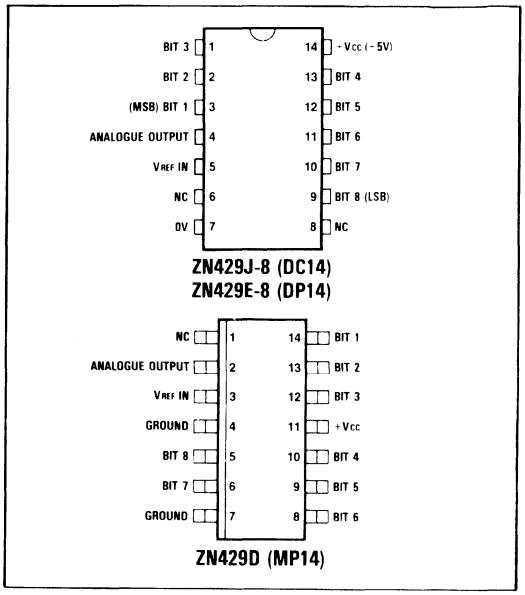
The ZN429 is a monolithic 8-bit D-A converter containing an R-2R ladder network of diffused resistors with precision bipolar switches.

FEATURES

- Linearity Error ± ½ LSB
- Single +5V Supply
- Low Power Consumption 25mW Typical
- Settling Time 1 microsecond Typical
- TTL and 5V CMOS Compatible
- Designed for Low-Cost Applications
- Commercial or Military Temperature Ranges

ORDERING INFORMATION

Device type	Operating temperature	Package
ZN429D	0°C to +70°C	MP14
ZN429E-8	0°C to +70°C	DP14
ZN429J-8	-55°C to +125°C	DC14



Pin connections - top view

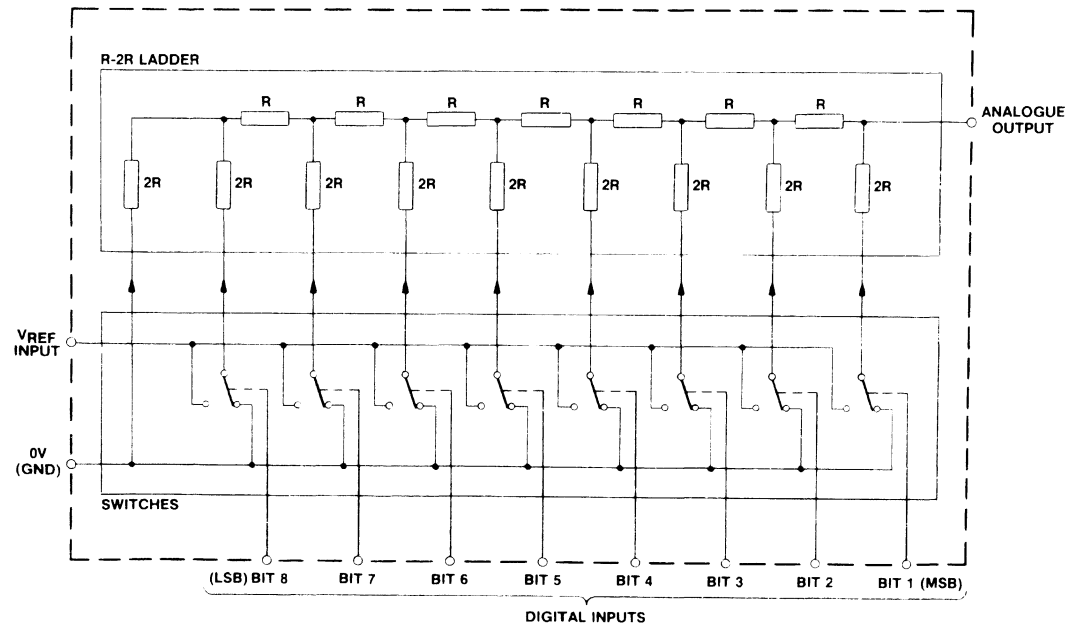


Fig.1 System diagram (see pin connection diagrams above for pin outs)

INTRODUCTION

The ZN429 is an 8-bit D-A converter. It contains an advanced design of R-2R ladder network and an array of precision bipolar switches on a single monolithic chip.

The special design of ladder network results in full 8-bit accuracy using normal diffused resistors.

The converter is of the voltage switching type and uses an R-2R resistor ladder network as shown in Fig. 2.

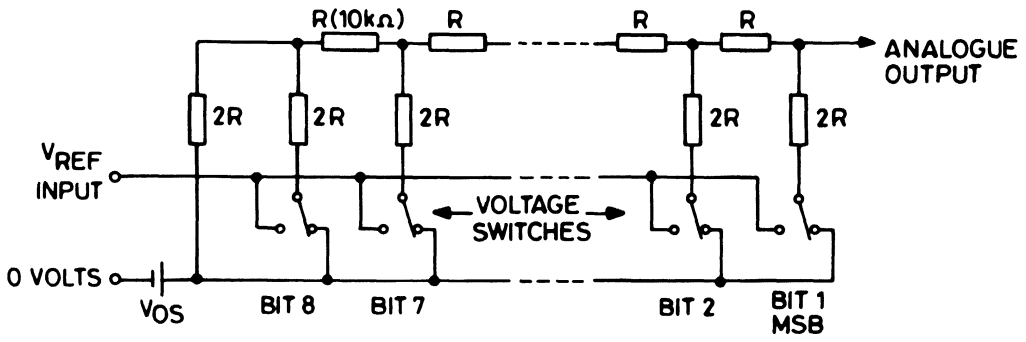


Fig. 2 The R-2R ladder network

Each 2R element is connected either to 0V or V_{REF} by transistor switches specially designed for low offset voltage (typically 1mV).

Binary weighted voltages are produced at the output of the R-2R ladder, the value depending on the digital number applied to the bit inputs.

An external fixed or varying reference is required which should have a slope resistance less than 2Ω.

Suggested external reference sources are the ZN404 or one of the ZN458 range. Each ZN404 is capable of supplying up to five ZN429 circuits and this is increased to ten for the ZN458 range.

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+7V
Max. voltage, logic and V_{REF} inputs	+5.5V
Storage temperature range	−55 to +125°C

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25°C$ and $V_{CC} = +5V$ unless otherwise specified).

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Converter						
Resolution		8	–	–	Bits	
Accuracy		8	–	–	Bits	
Non-linearity		–	–	±0.5	LSB	Note 1
Differential non-linearity		–	±0.5	–	LSB	Note 2
Settling time to 0.5LSB		–	1.0	–	μs	1 LSB step
Settling time to 0.5LSB		–	2.0	–	μs	All bits ON to OFF or OFF to ON
Offset voltage ZN429J-8 ZN429E-8, ZN429D	V_{OS}	– –	5.0 3.0	8.0 5.0	mV mV	All bits OFF note 1
V_{OS} temperature co-efficient		–	5	–	μV/°C	
Full-scale output		2.545	2.550	2.555	V	All bits ON Ext. $V_{REF} = 2.56V$
Full-scale temperature coefficient		–	3	–	ppm/°C	Ext. $V_{REF} = 2.560V$
Non-linearity temp. co-efficient		–	7.5	–	ppm/°C	Relative to F.S.R.
Analogue output resistance	R_O	–	10	–	kΩ	
External reference voltage		0	–	3.0	V	
Supply voltage	V_{CC}	4.5	–	5.5	V	
Supply current	I_S	–	5	9	mA	
High level input voltage	V_{IH}	2.0	–	–	V	
Low level input voltage	V_{IL}	–	–	0.7	V	
High level input current	I_{IH}	– –	– –	10 100	μA μA	$V_{CC} = max$, $V_I = 2.4V$ $V_{CC} = max$, $V_I = 5.5V$
Low level input current	I_{IL}	–	–	−0.18	mA	$V_{CC} = max$, $V_I = 0.3V$

Notes:

1. The ZN429J-8 differs from the ZN429E-8 and the ZN429D in the following respects:
   (a) For the ZN429J-8, the maximum linearity error may increase to ±0.4% FSR i.e. ±1LSB over the temperature ranges −55 to 0°C and +70 to +125°C.
   (b) Offset voltage. The difference is due to package lead resistance. This offset will normally be removed by the setting up procedure, and because the offset temperature coefficient is low, the specified accuracy will be maintained.
2. Monotonic over full temperature range.

APPLICATIONS

(1) Unipolar D-A converter

The nominal output range of the ZN429 is 0 to $V_{REF\ IN}$ through a 10kΩ resistance. Other output ranges can readily be obtained using an external amplifier.

The resulting full-scale range is given by

$$V_{OUT\ FS} = \left(1 + \frac{R1}{R2}\right) V_{REF\ IN} = G.\ V_{REF\ IN}$$

The impedance at the inverting input is R1//R2 and for low drift with temperature this parallel combination should be equal to the ladder resistance (10kΩ). The required nominal values of R1 and R2 are given by

$$R1 = 10Gk\Omega \text{ and } R2 = 10G/(G\text{-}1)\ k\Omega$$

Using these relationships a table of nominal resistance values for R1 and R2 can be constructed for $V_{REF\ IN}$ = 2.5V.

Output range	G	R1	R2
+5V	2	20kΩ	20kΩ
+10V	4	40kΩ	13.33kΩ

For gain setting R1 is adjusted about its nominal value. Practical circuit realisations (including amplifier stabilising components) for +5 and +10V output ranges are given in Fig. 4. Settling time for a major transition is 2.5μs typical.

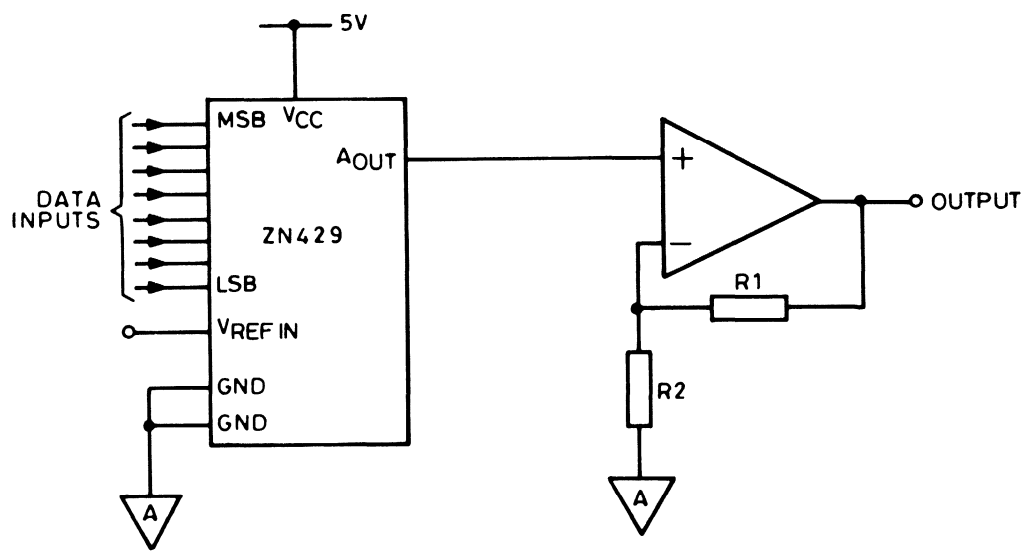


Fig. 3 Unipolar operation - basic circuit

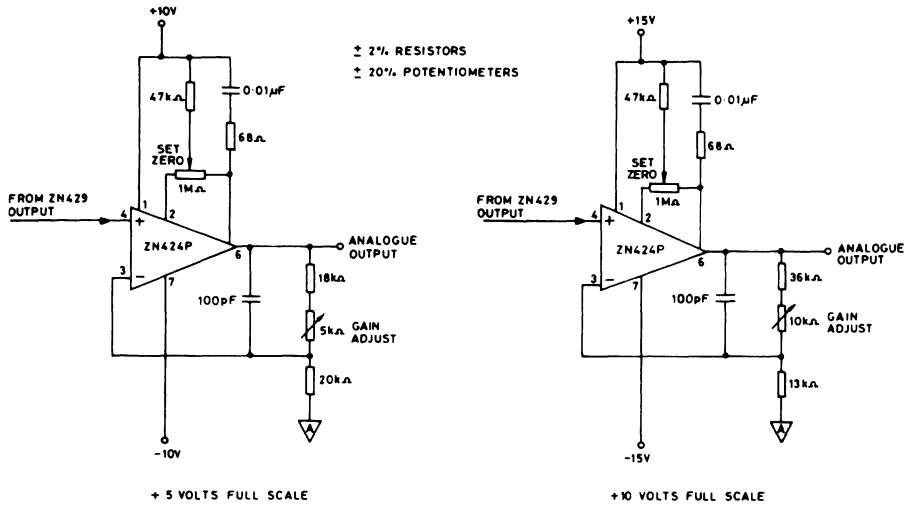


Fig. 4 Unipolar operation - component values

UNIPOLAR ADJUSTMENT PROCEDURE

(i) Set all bits to OFF (LOW) and adjust zero until $V_{OUT} = 0.0000V$

(ii) Set all bits ON (HIGH) and adjust gain until $V_{OUT} = FS - 1LSB$.

UNIPOLAR SETTING UP POINTS

Output range, +FS	LSB	FS – 1LSB
+ 5V	19.5mV	4.9805V
+ 10V	39.1mV	9.9609V

$$1LSB = \frac{FS}{256}$$

UNIPOLAR LOGIC CODING

Input code (Binary)	Analogue output (Nominal value)
11111111	FS – 1LSB
11111110	FS – 2LSB
11000000	¾FS
10000001	½FS + 1LSB
10000000	½FS
01111111	½FS – 1LSB
01000000	¼FS
00000001	1LSB
00000000	0

(2) Bipolar D-A converter

For bipolar operation the output from the ZN429 is offset by half full-scale by connecting a resistor R3 between $V_{REF\ IN}$ and the inverting input of the buffer amplifier (Fig. 5).

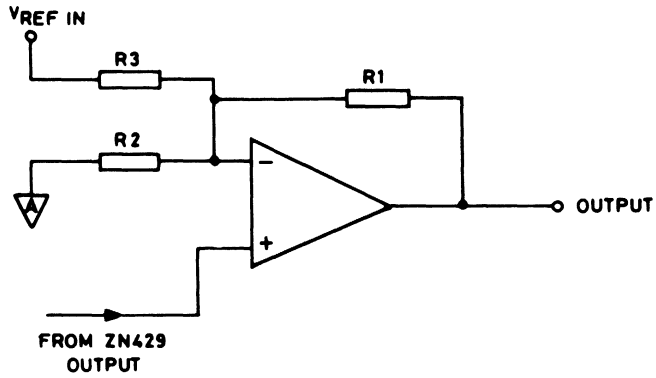


Fig. 5 Bipolar operation - basic circuit

When the digital input of the ZN429 is zero the analogue output is zero and the amplifier output should be – full-scale. An input of all ones to the D-A will give a ZN429 output of $\simeq V_{REF\ IN}$ and the amplifier output required is + full-scale. Also, to match the ladder resistance, the parallel combination of R1, R2 and R3 should be 10kΩ.

The nominal values of R1, R2 and R3 which meet these conditions are given by

R1 = 20GkΩ, R2 = 20G/(G-1)kΩ and R3 = 20kΩ

where the resultant output range is $\pm G.V_{REF\ IN}$.

Assuming that $V_{REF\ IN} = 2.5V$ the nominal values of resistors for ± 5 and ± 10V output ranges are given in the following table.

Output range	G	R1	R2	R3
± 5V	2	40kΩ	40kΩ	20kΩ
± 10V	4	80kΩ	26.67kΩ	20kΩ

Minus full-scale (OFFSET) is set by adjusting R1 about its nominal value relative to R3. Plus full-scale (GAIN) is set by adjusting R2 relative to R1

Settling time for a major transition is 2.5μs typical.

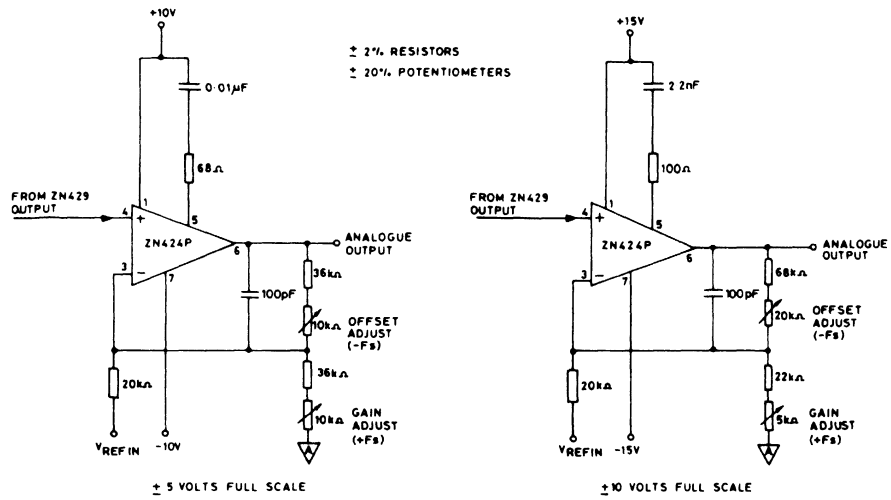


Fig. 6 Bipolar operation component values

BIPOLAR ADJUSTMENT PROCEDURE

(i) Set all bits to OFF (LOW) and adjust OFFSET until the amplifier output reads −FULL-SCALE.

(ii) Set all bits ON (HIGH) and adjust gain until the amplifier reads +(FULL-SCALE - 1LSB).

BIPOLAR SETTING UP POINTS

Input range, ±FS	LSB	−FS	+(FS - 1LSB)
±5V	39.1mV	−5.0000V	+4.9609V
±10V	78.1mV	−10.0000V	+9.9219V

$$1LSB = \frac{2FS}{256}$$

BIPOLAR LOGIC CODING

Input code (Offset binary)	Analogue output (Nominal value)
11111111	+(FS − 1LSB)
11111110	+(FS − 2LSB)
11000000	+½FS
10000001	+ 1LSB
10000000	0
01111111	− 1LSB
01000000	−½FS
00000001	−(FS - 1LSB)
00000000	−FS

For both unipolar and bipolar operation, an alternative output buffer, employing the 741 operational amplifier, or any other suitable op-amp, may be used.

The feedback resistors chosen are as indicated in the relevant sections.

The following circuit shows the use of the 741 in the unipolar operation mode for a voltage output range of 0→5V with a 2.5V reference.

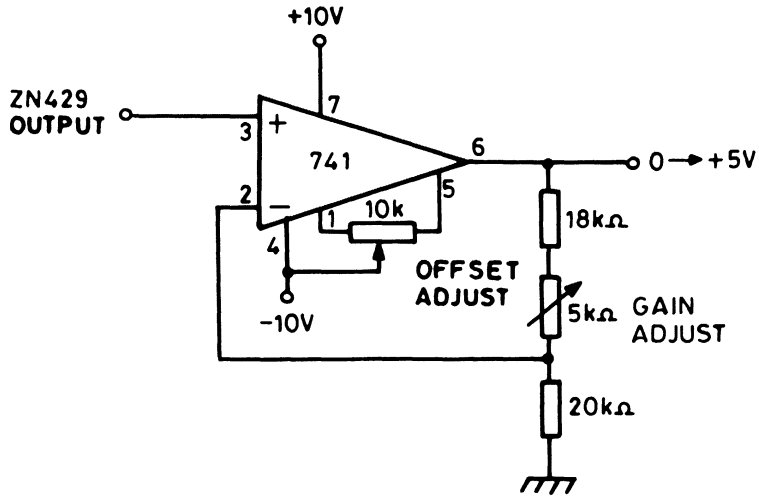


Fig. 7 Unipolar operation (+5V full-scale) using 741 op-amp

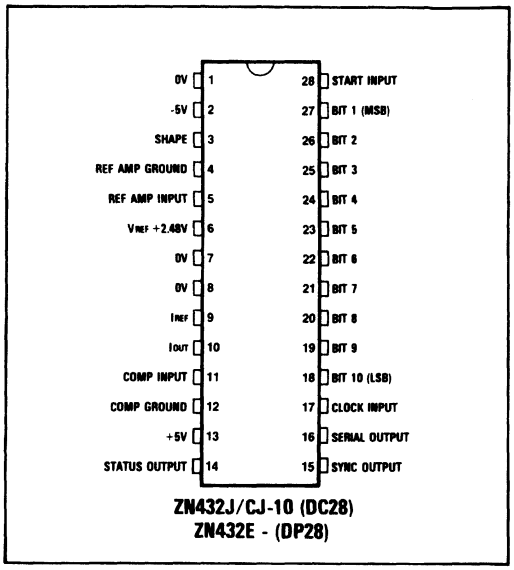
ZN432

10-BIT SUCCESSIVE APPROXIMATION A-D CONVERTER

The ZN432 range of successive approximation analogue to digital converters combine several innovations to provide this function on a fully monolithic silicon integrated circuit. The chip contains a current switching array using a matrix of diffused resistors (no trim required), successive approximation logic with TTL interfacing. 2.5V precision voltage reference with reference amplifier, and fast comparator with good overload recovery. The overall accuracy of the A-D system is sufficient to guarantee no missing codes over the operating temperature range.

FEATURES

- Choice of Linearity Error
- 3 Operating Temperature Ranges
- 20 microseconds Conversion Time Guaranteed
- Input Range as Desired
- ±5V Supplies, TTL/CMOS Compatible
- Parallel and Serial Outputs
- Bipolar Monolithic Construction



ZN432J/CJ-10 (DC28)
ZN432E - (DP28)

Pin connections - top view

ORDERING INFORMATION

Device type	Operating temperature	Package
ZN432E	0°C to +70°C	DP28
ZN432J-10	-55°C to +125°C	DC28
ZN432CJ-10	0°C to +70°C	DC28

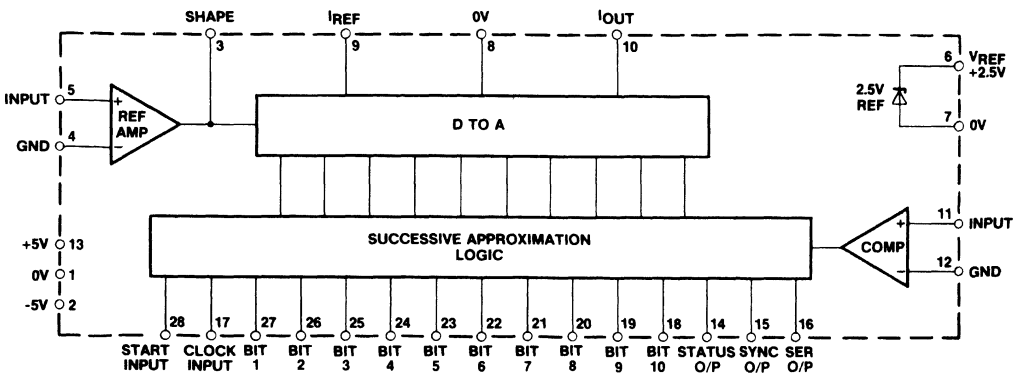


Fig.1 System diagram

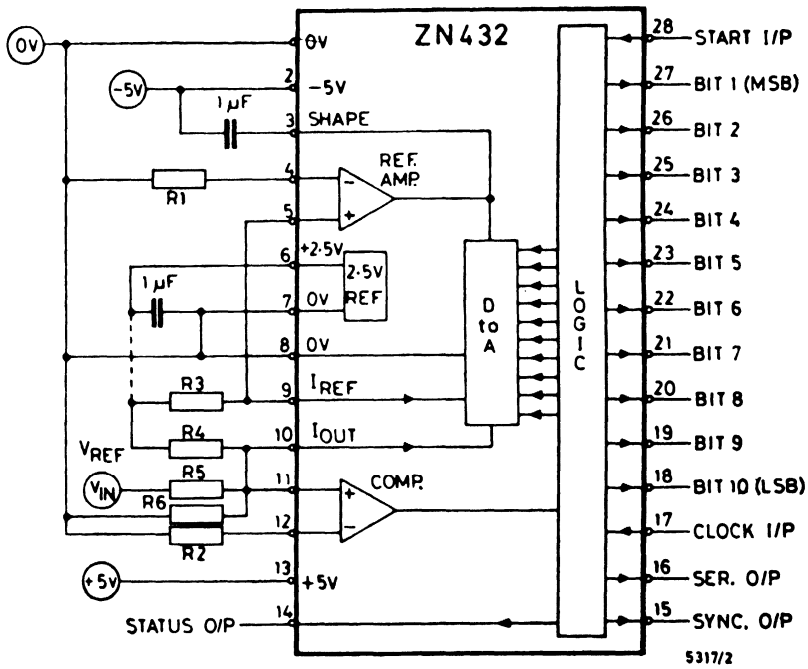


Fig. 2 Typical external components

ABSOLUTE MAXIMUM RATINGS

Supply voltage	± 7V
Logic input voltage	+ V_{CC} and 0V
Storage temperature range	− 55 to + 125°C

CHARACTERISTICS (at ±5V supplies and internal reference unless otherwise specified).

Parameter	Version	t_{amb} = +25°C			Over Spec. Temp. range		Units	Conds.
		Min.	Typ.	Max.	Min.	Max.		
Converter Resolution		10			10		Bits	Note 1
Linearity error	ZN432J-10			±0.5		±0.5	LSB	
	ZN432CJ-10							
	ZN432E			±1		±1	LBS	
Differential linearity error	All types		±0.5				LSB	Note 1
DAC reference current, I_{REF}	All types	0.25	0.5	1	0.25	1	mA	Note 2
Conversion time	All types		15	20		20	µs	Note 3
Nominal analogue input range	All types	−2.5		+2.5			V	Note 4
Supply rejection	All types		0.1				%/V	
Gain error	All types		±0.05				%	Note 5
Gain T.C.	ZN432J-10		10				ppm/°C	
	ZN432CJ-10							
	ZN432E		20				ppm/°C	
Zero T.C.	ZN432J-10		7				ppm/°C	
	ZN432CJ-10							
	ZN432E		15				ppm/°C	
Supply voltage	All types	±4.5	±5	±5.5	±4.5	±5.5	V	
Supply current	All types		35				mA	
Power consumption	All types		350				mW	

CHARACTERISTICS (Cont.)

Parameter	Version	t_{amb} = +25°C			Over Spec. Temp. range		Units	Conditions
		Min.	Typ.	Max.	Min.	Max.		
Internal voltage reference								
Output voltage	ZN432J-10	2.44	2.48	2.52			V	Note 6
	ZN432CJ-10							
	ZN432E	2.38	2.46	2.54			V	
Slope impedance	All types		0.75				Ω	
Max. load current	All types		±2				mA	
Logic	**All types**							
High level input voltage		2.0			2.0		V	
Low level input voltage				0.8		0.8	V	
High level input current			7				μA	$V_S = \pm 5.5V$ $V_I = 2.4V$
			50				μA	$V_S = \pm 5.5V$ $V_I = 5.5V$
Low level input current			1				μA	$V_S = \pm 5.5V$ $V_I = 0.4V$
High level output voltage		2.4			2.4		V	$I_{load} = 40\mu A$
Low level output voltage				0.4		0.4	V	$I_{load} = 1.6mA$

Note 1 No missing codes over full temperature range at resolution appropriate to accuracy.

Note 2 The full-scale D-A output current $I_{OUT} = 4$ times I_{REF}. For optimum performance $I_{REF} = 0.5mA$.

Note 3 This corresponds to a maximum clock rate of 550kHz based on 11 clock periods per conversion cycle (see timing diagram, page 2-41). This provides an update rate of 45kHz.

Note 4 Single polarity and other input ranges may be provided by different input resistor values. (see page 2-42)

Note 5 Excluding reference

Note 6 For typical temperature performance see Fig. 6, page 2-42.

TEST CIRCUIT

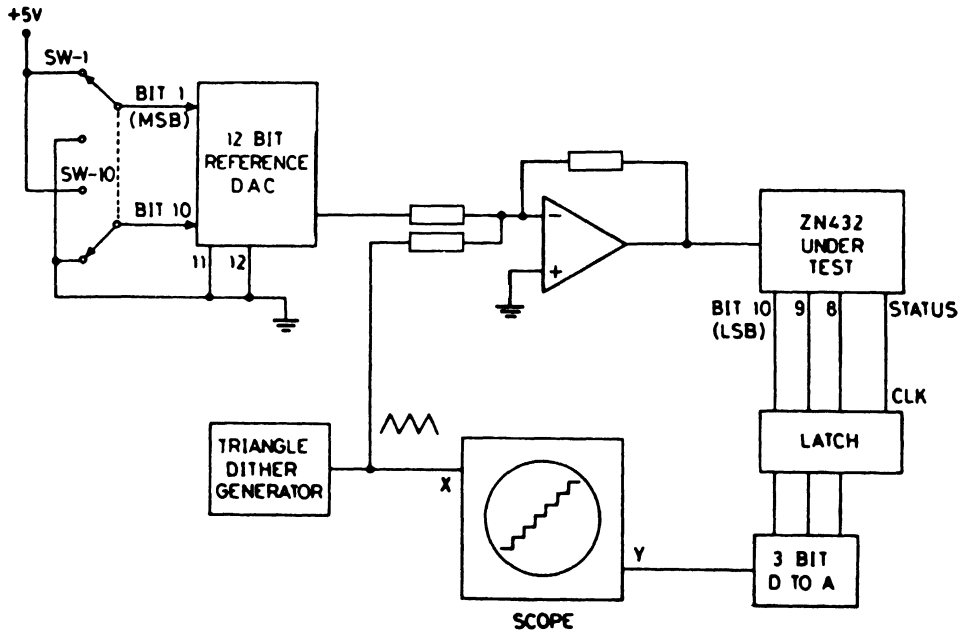


Fig. 3 Dynamic crossplot accuracy test

Switches SW-1 to SW-10 are set to the appropriate digital code to select the point on the characteristic to be displayed. For example, code 10000 00000 would select half full-scale, i.e. the major transition.

The output from the dither generator (suggested peak to peak amplitude = $\pm 4 \times$ LSB) is used as the X deflection for the scope and is also superimposed on the analogue output from the reference DAC in the summing amplifier. The resulting analogue signal including dither is used as V_{IN} for the ZN432 under test.

Bit 10, 9 and 8 outputs are fed to the inputs of a 3-bit DAC of at least 6-bit accuracy and the analogue output used as the Y deflection of the scope. Differential non-linearity is shown by horizontal lines which are longer or shorter than the rest.

CALCULATION OF EXTERNAL RESISTORS (See Fig. 2, page 2-36)

1. R_3, R_4, R_5 can affect gain and offset stability and thus require to be of high quality.
2. R_1 and R_2 are to allow for the bias current of the reference amplifier and comparator, thus:

$$R_1 = R_3$$

And R_2 = parallel combination of R_4, R_5, and R_6.

3. I_{REF} should be 0.5mA

Therefore $$R_3 = \frac{V_{REF}}{0.5mA}$$

I_{outFS} is four times I_{REF}, i.e., 2mA

4. Analysing the network yields the following:

$$R_4 = \frac{-V_{REF}\, R_5}{V_{in}\ min}$$

$$R_5 = \frac{V_{in}\ max - V_{in}\ min}{I_{out\ FS}}$$

Where V_{in} max is the voltage for the logic output to be all 1's.
V_{in} min is the voltage for the logic output to be all 0's.

5. R_6 should be chosen such that the parallel combination of R_4, R_5 and R_6 is about 1.25kΩ as this determines the D-A time constant and hence conversion time.
6. The following is a table of values to give examples of the above equations.

V_{in} max	V_{in} min	V_{REF}	R_1[1]	R_2[1]	R_3	R_4	R_5	R_6[1]
+2.5	2.5	2.5	5kΩ	1.25kΩ	5kΩ	2.5kΩ	2.5kΩ	∞
+2.5	2.5	5*	10kΩ	1.25kΩ	10kΩ	5kΩ	2.5kΩ	5kΩ
+2.5	0	2.5	5kΩ	1.25kΩ	5kΩ	∞	1.25kΩ	∞
+5	0	2.5	5kΩ	1.25kΩ	5kΩ	∞	2.5kΩ	2.5kΩ
+4	2	2.5	5kΩ	1.25kΩ	5kΩ	3.75kΩ	3kΩ	5kΩ
+4	2	12*	24kΩ	1.25kΩ	24kΩ	3.75kΩ	3kΩ	5kΩ
+10	10	2.5	5kΩ	1.25kΩ	5kΩ	2.5kΩ	10kΩ	3.33kΩ

Note 1 Nearest prefered value may be used for R_1, R_2 and R_6.

*Note 2 External reference.

7. For setting up R_4 will adjust the offset.
R_3 will adjust the gain.

For unipolar operation where R_4 approaches ∞ and a zero adjustment is required, the following offset circuit is suggested in place of R_4 (Typical values only).

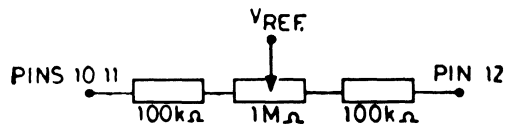


Fig. 4 Offset circuit with unipolar operation

TIMING DETAILS

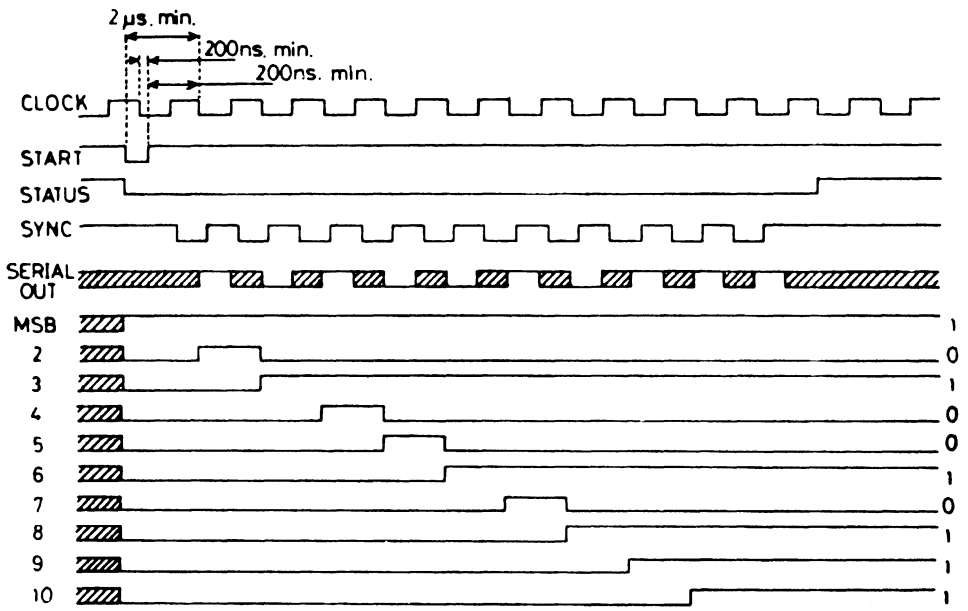


Fig. 5 Timing diagram

NOTES ON TIMING DIAGRAM

1. Conversion is initiated by a 'START' pulse which sets the MSB to 1 and all other bits to 0.

2. The first active (negative going) edge of clock after the trailing edge of the 'START' pulse should not occur until at least 2μs after the leading edge of the 'START' pulse to allow for MSB settling.

3. A negative going edge of clock must not occur within 200ns either side of the trailing edge of the 'START' pulse.

4. As a special case of conditions (2) and (3) the 'START' pulse may be coincident with, and of the same duration as, a negative going clock pulse.

5. Serial data is available during conversion at the Serial Output.

Ten SYNC pulses are provided to facilitate data transmission.

The serial output data is valid on the positive going edge of the SYNC pulse.

6. Cross hatching indicates a 'don't care' condition or, in the case of serial output, invalid data.

7. The conversion sequence shown is for the digital word 1010010111.

8. The parallel output data is valid when the status output goes HIGH.

LOGIC CODING

Table 1 Unipolar operation

Analogue input Notes 1, 2	Digital output code MSB LSB
FS – 1LSB	1111111111
FS – 2LSB	1111111110
¾FS	1100000000
½FS + 1LSB	1000000001
½FS	1000000000
½FS – 1LSB	0111111111
¼FS	0100000000
1LSB	0000000001
0	0000000000

Table 2 Bipolar operation

Analogue input Notes 1, 2	Digital output code MSB LSB
+ (FS – 1LSB)	1111111111
+ (FS – 2LSB)	1111111110
+ (½FS)	1100000000
+ (1LSB)	1000000001
0	1000000000
– (1LSB)	0111111111
– (½FS)	0100000000
– (FS – 1LSB)	0000000001
– FS	0000000000

NOTES:

1. Analogue inputs shown are nominal centre values of code.
2. "FS" is full-scale.

OFFSET AND GAIN SETTING

For unipolar, supply an input of ½LSB for transition 0000000000 to 0000000001, and of (full-scale – 1½LSB) for transition 1111111111 to 1111111110.

For bipolar, supply an input of – (full-scale – ½LSB) for transition 0000000000 to 0000000001, and of (full-scale – 1½LSB) for transition 1111111111 to 1111111110.

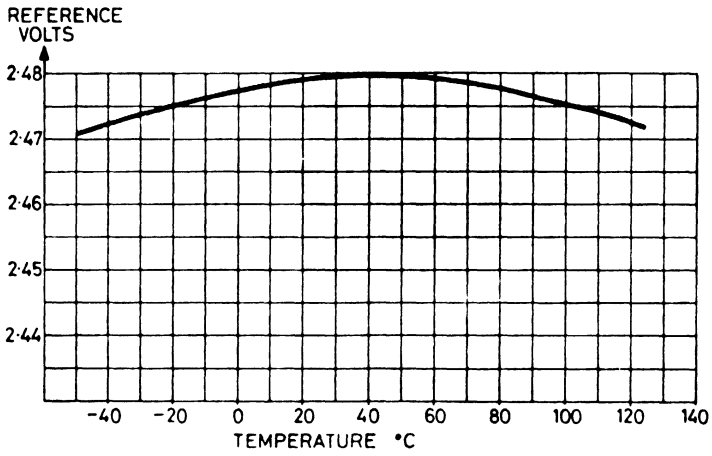


Fig. 6 Typical reference voltage v temperature (all types)

ZN433

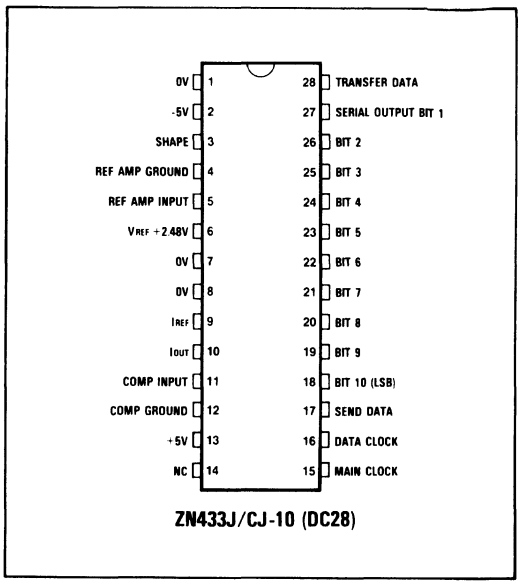
10-BIT TRACKING A-D CONVERTER

The ZN433 range of tracking A-D converters combine several innovations to provide this function on a fully monolithic silicon integrated circuit. The chip contains a current switching array using a matrix of diffused resistors (no trim required), tracking logic with TTL interfacing, 2.5V precision voltage reference with reference amplifier, and fast window comparator with good overload recovery.

The tracking principle ensures continuous up to date conversion data. This is suitable for single channel conversion, e.g. digital transducers, and often obviates the need for sample and hold.

FEATURES

- ±½ LSB Linearity Error
- 1 microsecond Conversion Time (Assuming Continuous Tracking)
- Input Range as Desired
- ±5V Supplies, TTL/CMOS Compatible
- Parallel and Serial Outputs
- Bipolar Monolithic Construction
- No Missing Codes over Full Operating Temperature Range



Pin connections - top view

ORDERING INFORMATION

Device type	Operating temperature	Package
ZN433J-10	-55°C to +125°C	DC28
ZN433CJ-10	0°C to +70°C	DC28

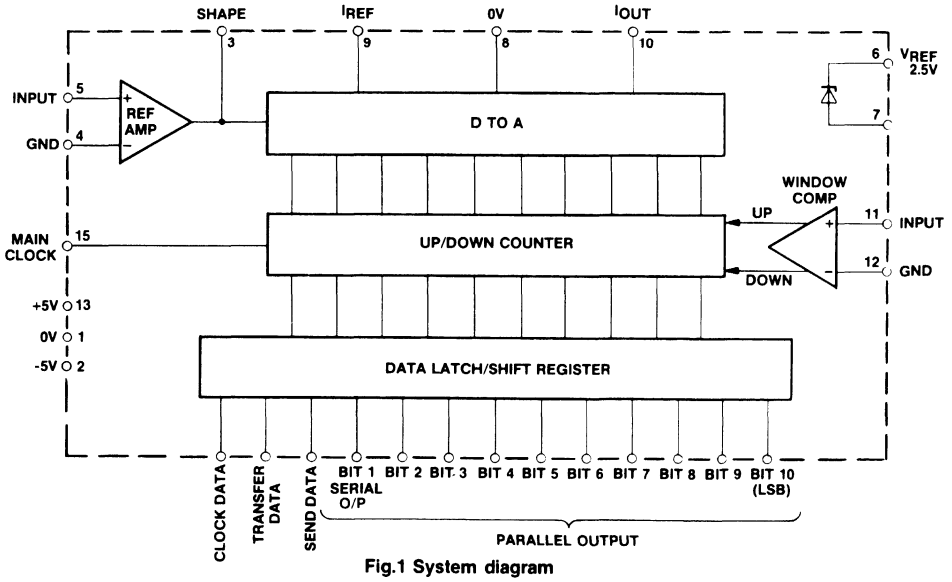


Fig.1 System diagram

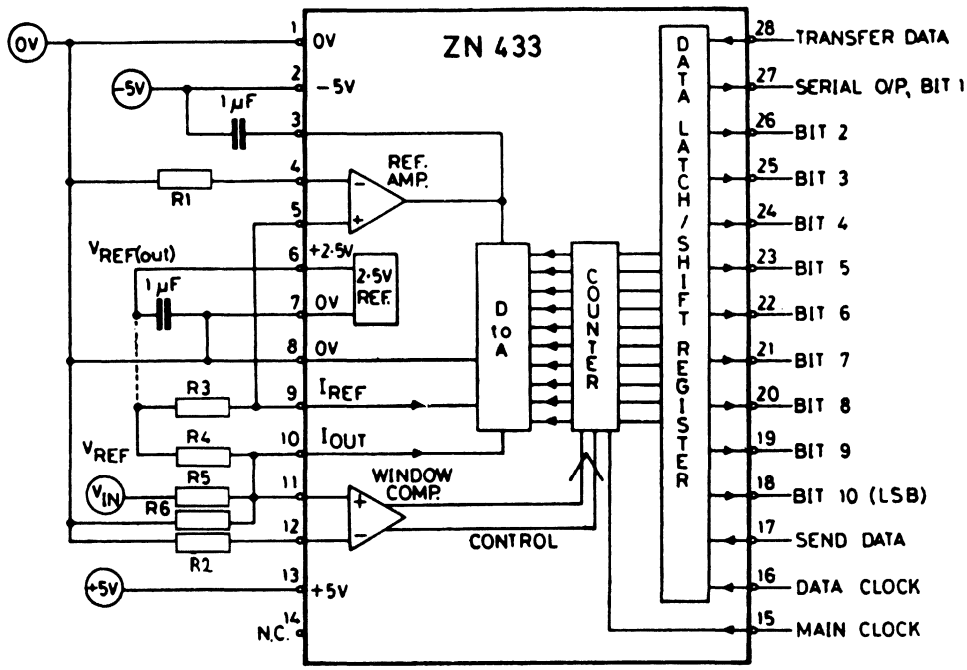


Fig. 2 Typical external components

See page 179 for calculation of resistor values. When the internal reference is used, $V_{REF(out)}$ (pin 6) is connected to R3 and R4 as shown. An external reference may also be used, which for ratiometric operation can vary by ±20% of nominal.

ABSOLUTE MAXIMUM RATINGS

Supply voltage	±7V
Logic input voltage	$+V_{CC}$ and 0V
Storage temperature range	−55 to +125°C

CHARACTERISTICS (at ±5V supplies and internal reference unless otherwise specified).

Parameter	t_{amb} = +25°C			Over Spec. Temp. range		Units	Conds.
	Min.	Typ.	Max.	Min.	Max.		
Converter							
Resolution	10			10		Bits	Note 1
Non-linearity			±0.5			LSB	
Differential non-linearity		±0.5				LSB	Note 1
D-A reference current, I_{REF} (pin 9)	0.8		1.2	0.8	1.2	mA	Note 2
Max. clock rate	1	1.2		1		MHz	Note 3
Nominal analogue input range	−2.5		+2.5			V	Note 4
Supply rejection		0.1				%/V	
Gain T.C. (note 5)		10				ppm/°C	
Zero T.C.		7				ppm/°C	
Supply voltage	±4.5	±5	±5.5	±4.5	±5.5	V	
Supply current		50				mA	
Power consumption		500				mW	
Internal voltage reference							
Output voltage		2.480				V	
Output voltage tolerance (note 6)			±1.5			%	
Slope impedance		0.75				Ω	
Maximum reference load current		±4				mA	

CHARACTERISTICS (Cont.)

Parameter	t_{amb} = +25°C			Over Spec. Temp. range		Units	Conditions
	Min.	Typ.	Max.	Min.	Max.		
Logic							
High level input voltage	2.0			2.0		V	
Low level input voltage			0.8		0.8	V	
High level input current		7				μA	$V_S = \pm 5.5V$, $V_I = 2.4V$
		50				μA	$V_S = \pm 5.5V$, $V_I = 5.5V$
Low level input current		1				μA	$V_S = \pm 5.5V$, $V_I = 0.4V$
High level output voltage	2.4			2.4		V	$I_{load} = -40\mu A$
Low level output voltage			0.4		0.4	V	$I_{load} = 1.6mA$

NOTES

1. **No missing codes over full temperature range.**
2. **The full-scale D-A output current I_{OUT} = 4 times I_{REF}. For optimum performance I_{REF} = 1.0mA.**
3. **For main clock waveform see Fig.5. Input signals which do not change by more than 1 LSB/μs may be tracked continuously without the need for a sample and hold. This corresponds to a full-scale bandwidth of 300Hz. Higher frequencies may be tracked if the amplitude is reduced, e.g. the half full-scale bandwidth is 600Hz.**
4. **Single polarity and other input ranges may be provided by different input resistor values.**
5. **Excluding reference.**
6. **For typical temperature performance see Fig.6.**

TEST CIRCUIT

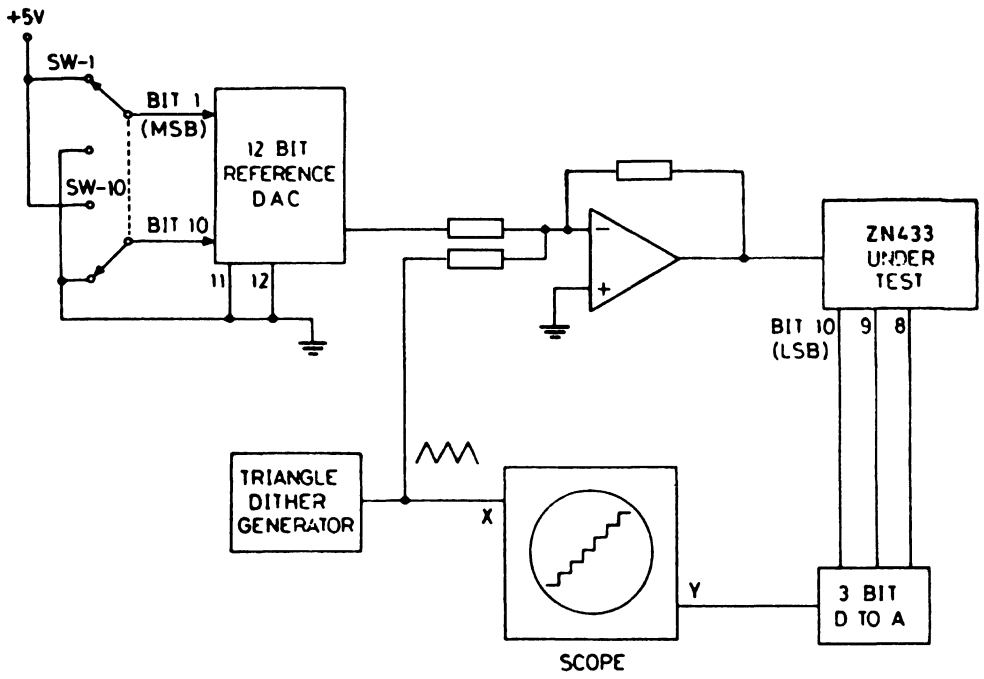


Fig. 3 Dynamic crossplot accuracy test

Switches SW-1 to SW-10 are set to the appropriate digital code to select the point on the charactristic to be displayed. For example, code 10000 00000 would select half full-scale, i.e. the major transition.

The output from the dither generator (suggested peak to peak amplitude = $\pm 4 \times$ LSB) is used as the X deflection for the scope and is also superimposed on the analogue output from the reference DAC in the summing amplifier. The resulting analogue signal including dither is used as V_{IN} for the ZN433 under test.

Bit 10, 9 and 8 outputs are fed to the inputs of a 3-bit DAC of at least 6-bit accuracy and the analogue output used as the Y deflection of the scope. Differential non-linearity is shown by horizontal lines which are longer or shorter than the rest.

CALCULATION OF EXTERNAL RESISTORS

1. R_3, R_4, R_5 can affect gain and offset stability and thus require to be of high quality.
2. R_1 and R_2 are to allow for the bias current of the reference amplifier and comparator which both operate in a virtual earth mode. Thus: $R_1 = R_3$

   And R_2 = parallel combination of R_4, R_5, and R_6.
3. I_{REF} should be 1.0mA, though it may be varied from 0.8 to 1.2mA.

   Therefore $$R_3 = \frac{V_{REF}}{1.0mA}$$

   $I_{out\ FS}$ is four times I_{REF}, i.e., 4mA (I_{out} for zero reading is 0mA).
4. Analysing the network yields the following:

$$R_4 = \frac{-V_{REF}\ R_5}{V_{in}\ min}$$

$$R_5 = \frac{V_{in}\ max - V_{in}\ min}{I_{outFS}}$$

   Where V_{in} max is the voltage for the logic output to be all 1's.
   V_{in} min is the voltage for the logic output to be all 0's.
5. R_6 should be chosen such that the parallel combination of R_4, R_5 and R_6 is about 625Ω as this determines the D-A time constant and hence conversion time.
6. The following is a table of values to give examples of the above equations.

V_{in} max	V_{in} min	V_{REF}	R_1[1]	R_2[1]	R_3	R_4	R_5	R_6[1]
+2.5	−2.5	2.5	2.5kΩ	625Ω	2.5kΩ	1.25kΩ	1.25kΩ	∞
+2.5	−2.5	5*	5kΩ	625Ω	5kΩ	2.5kΩ	1.25kΩ	2.5kΩ
+2.5	0	2.5	2.5kΩ	625Ω	2.5kΩ	∞	625Ω	∞
+5	0	2.5	2.5kΩ	625Ω	2.5kΩ	∞	1.25kΩ	1.25kΩ
+4	−2	2.5	2.5kΩ	625Ω	2.5kΩ	1.875kΩ	1.5kΩ	2.5kΩ
+4	−2	12*	12kΩ	625Ω	12kΩ	1.875kΩ	1.5kΩ	2.5kΩ
+10	−10	2.5	2.5kΩ	625Ω	2.5kΩ	1.25kΩ	5kΩ	1.67kΩ

Note 1 Nearest prefered value may be used for R_1, R_2 and R_6.

*Note 2 External reference.

7. For setting up R_4 will adjust the offset.
   R_3 will adjust the gain.

For unipolar operation where R_4 approaches ∞ and a zero adjustment is required, the following offset circuit is suggested in place of R_4 (Typical values only).

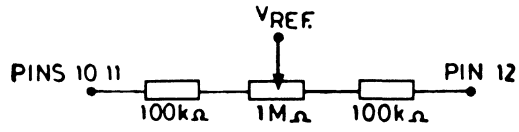


Fig. 4 Offset circuit with unipolar operation

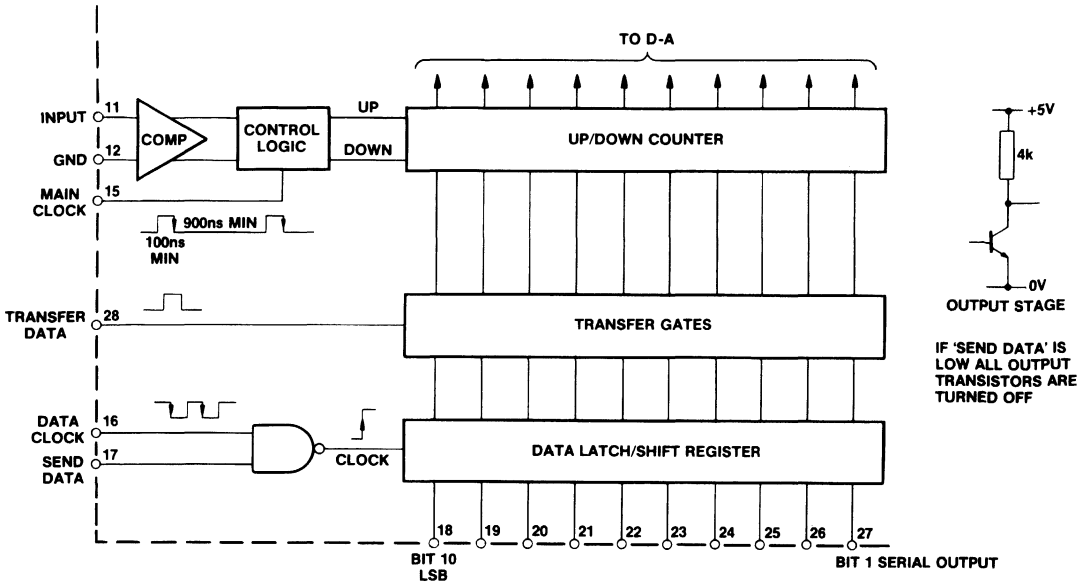


Fig.5 Logic system

NOTES ON LOGIC DIAGRAM

1. The Window comparator and control logic determine whether the counter will clock up or down or keep the same value on an active (negative going) edge of the main clock.

2. Parallel data from the up/down counter will be loaded into the output data latch/shift register when the TRANSFER DATA input is HIGH. TRANSFER DATA should not be taken HIGH until 150ns after the MAIN CLOCK edge and should go LOW before the next MAIN CLOCK edge. The minimum TRANSFER DATA pulse width is 50ns.

If TRANSFER DATA is held permanently HIGH then the counter outputs will appear directly at the bit outputs.

3. Serial output data (MSB first) can be obtained from the MSB output (pin 27) by applying a DATA CLOCK (pin 16, 1MHz maximum, 100ns minimum pulse width).

4. A LOW on SEND DATA (pin 17) disables the DATA CLOCK and turns off all the output transistors so that all the bit outputs are HIGH (see diagram of output).

LOGIC CODING

Table 1 Unipolar operation

Analogue input Notes 1, 2	Digital output code MSB LSB
FS – 1LSB	1111111111
FS – 2LSB	1111111110
¾FS	1100000000
½FS + 1LSB	1000000001
½FS	1000000000
½FS – 1LSB	0111111111
¼FS	0100000000
1LSB	0000000001
0	0000000000

Table 2 Bipolar operation

Analogue input Notes 1, 2	Digital output code MSB LSB
+ (FS – 1LSB)	1111111111
+ (FS – 2LSB)	1111111110
+ (½FS)	1100000000
+ (1LSB)	1000000001
0	1000000000
– (1LSB)	0111111111
– (½FS)	0100000000
– (FS – 1LSB)	0000000001
– FS	0000000000

Notes:

1. Analogue inputs shown are nominal centre values of code.
2. "FS" is full-scale.

OFFSET AND GAIN SETTING

For unipolar operation, supply an input of ½LSB for transition 0000000000 to 0000000001, and of (full-scale – 1½LSB) for transition 1111111111 to 1111111110.

For bipolar operation, supply an input of – (full-scale – ½LSB) for transition 0000000000 to 0000000001, and of (full-scale – 1½LSB) for transition 1111111111 to 1111111110.

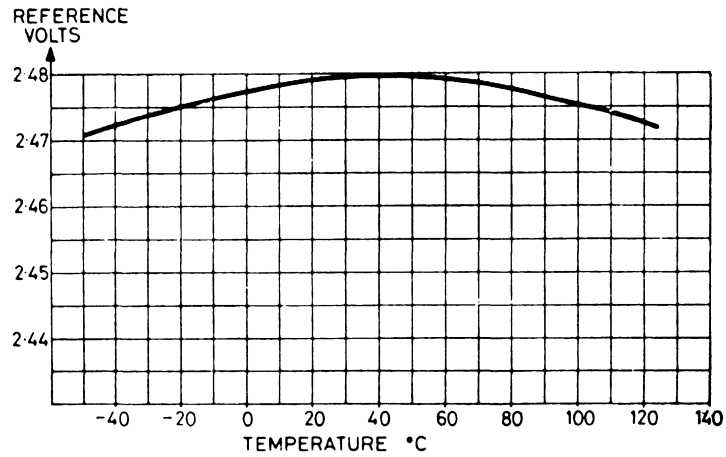


Fig. 6 Typical reference voltage v temperature (all types)

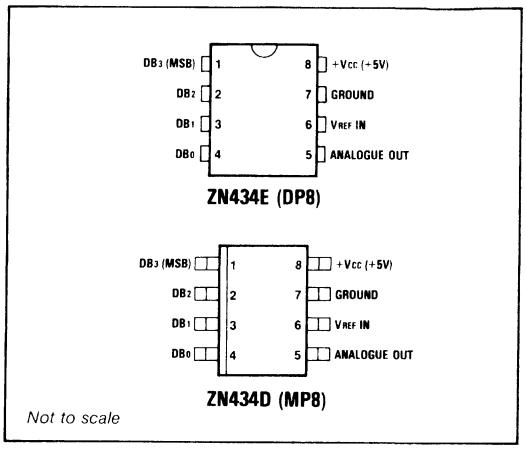
ZN434

LOW COST 4-BIT D-A CONVERTER

The ZN434 is a 4-bit D-A converter containing an R-2R ladder network of diffused resistors and precision bipolar switches. An on-chip reference amplifier and attenuator provide a reference voltage of $\frac{V_{CC}}{2}$, allowing the IC to function with no external components.

FEATURES

- 4-Bit Resolution
- ¼ LSB Linearity
- Voltage Output
- 300ns Settling Time
- TTL and CMOS Compatible
- Single +5V Supply
- On-Chip $\frac{V_{CC}}{2}$ Reference



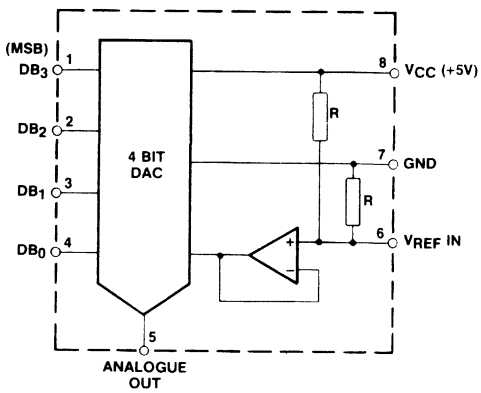
Pin connections - top view

ORDERING INFORMATION

Device type	Operating temperature	Package
ZN434E	-40°C to +85°C	DP8
ZN434D	-40°C to +85°C	MP8

ABSOLUTE MAXIMUM RATINGS

Supply voltage	+7V
Logic and V_{REF} inputs	0V to V_{CC}
Operating temperature range	-40°C to +85°C
Storage temperature range	-55°C to +125°C



ZN434 system diagram

ELECTRICAL CHARACTERISTICS (V_{CC} = +5V, T_{amb} = 25°C unless otherwise specified).

Parameter	Min.	Typ.	Max.	Units	Conditions
D-A converter resolution	4	–	–	Bits	
Linearity error	–	–	±0.25	LSB	$1.5V < V_{REFin} < 3V$
Differential linearity error	–	–	±0.25	LSB	
Linearity error T.C.	–	±30	–	ppm/°C	Relative to FSR
Differential linearity error T.C.	–	±11	–	ppm/°C	Relative to FSR
Zero error	–	3.0	5.0	mV	
Zero error T.C.	–	+6	–	μV/°C	
Full-scale output	2.235	2.345	2.456	V	
Full-scale output (external reference)	0.922	0.938	0.954	V_{ref}in	$1.5V < V_{REFin} < 3V$
Full-scale T.C.	–	±30	–	ppm/°C	External V_{REF} = 2.56V
Analogue output resistance	1.75	2.5	3.25	kΩ	
Analogue output capacitance	–	15	–	pF	
Settling time to 0.5 LSB	–	200	300	ns	Code transition 0000 1111 or 1111 0000
	–	100	150	ns	1 LSB step
Supply voltage	+4.5	+5	+5.5	V	
Supply current	–	10	15	mA	

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	Min.	Typ.	Max.	Units	Conditions
On-chip reference amplifier					
Output voltage	$\frac{V_{CC}}{2} \times 0.97$	$\frac{V_{CC}}{2}$	$\frac{V_{CC}}{2} \times 1.03$		
Input current	–	1	–	μA	
Offset voltage		± 10		mV	
Input resistance at pin 6	9	18	27	kΩ	Note 1
Logic inputs					
High level input voltage V_{IH}	2.0	–	–	V	
Low level input voltage V_{IL}	–	–	0.8	V	
High level input current I_{IH}	–	–	10	μA	$V_{CC} = 5.5V$, $V_I = 2.4V$
	–	–	100	μA	$V_{CC} = V_I = 5.5V$
Low level input current I_{IL}	–	–	180	μA	$V_{CC} = 5.5V$, $V_I = 0.3V$

Note 1: Includes on-chip attenuator. Nominal value of R is 36kΩ.

CIRCUIT DESCRIPTION

D-A converter

The ZN434 is a 4-bit D-A converter consisting of an R-2R ladder of diffused resistors and precision bipolar switches designed for low offset voltage.

The ladder operates in the voltage switching mode and produces an output voltage $V_{out} = \frac{n}{16}(V_{REF\ IN} - V_{OS}) + V_{OS}$, where n is the digital code set at the bit inputs and V_{OS} is a small offset voltage caused by the supply current flowing through the lead resistance of the ground pin.

On-chip reference amplifier

The ZN434 contains a reference amplifier and attenuator that provides a reference voltage of nominally $\frac{V_{CC}}{2}$ without any external components. Taking into account the attenuator error, input current and offset voltage of the amplifier and gain error of the D-A converter the full-scale output will be within ± ½LSB of the nominal value of $0.469 \times V_{CC}$.

By maintaining an accurate and stable supply voltage the ZN434 may thus be used without an external reference. Where several ZN434's are used in a system the V_{REF} inputs may be joined together to improve V_{REF} matching.

If a reference voltage other than $\frac{V_{CC}}{2}$ is required then the on-chip attenuator may be overridden, either by connecting a lower resistance attenuator in parallel or by using an active reference such as a bandgap reference source.

PLESSEY
Semiconductors

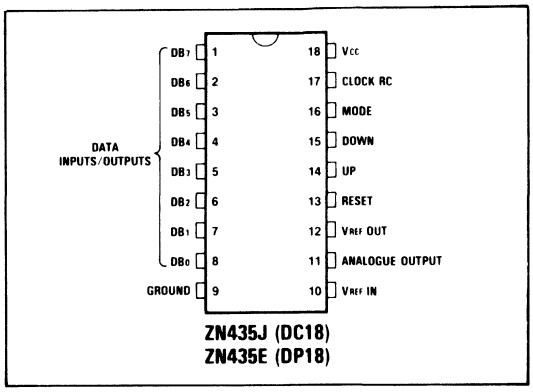
ZN435

8-BIT MULTIFUNCTION DATA CONVERTER

The ZN435 is a versatile, multifuction 8-bit data conversion system. A voltage output DAC, 8-bit up/down counter, stable 2.5V bandgap reference and clock generator are contained on a single chip.

FEATURES

- Multimode Device Operates as:
  - DAC
  - ADC
  - Tracking ADC
  - Voltage to Frequency Converter
  - Ramp and Sawtooth Generator
  - Nonlinear Waveform Generator
  - Voltage-Controlled Oscillator
  - Track-and-Hold Circuit
- 8-Bit Accuracy
- 800ns D-A Converter Settling Time
- On-Chip Up/Down Counter
- On-Chip Clock
- On-Chip Voltage Reference
- Single +5V Supply
- Commercial or Military Temperature Range



Pin connections - top view

ORDERING INFORMATION

Device type	Operating temperature	Package
ZN435E	0°C to +70°C	DP18
ZN435J	-55°C to +125°C	DC18

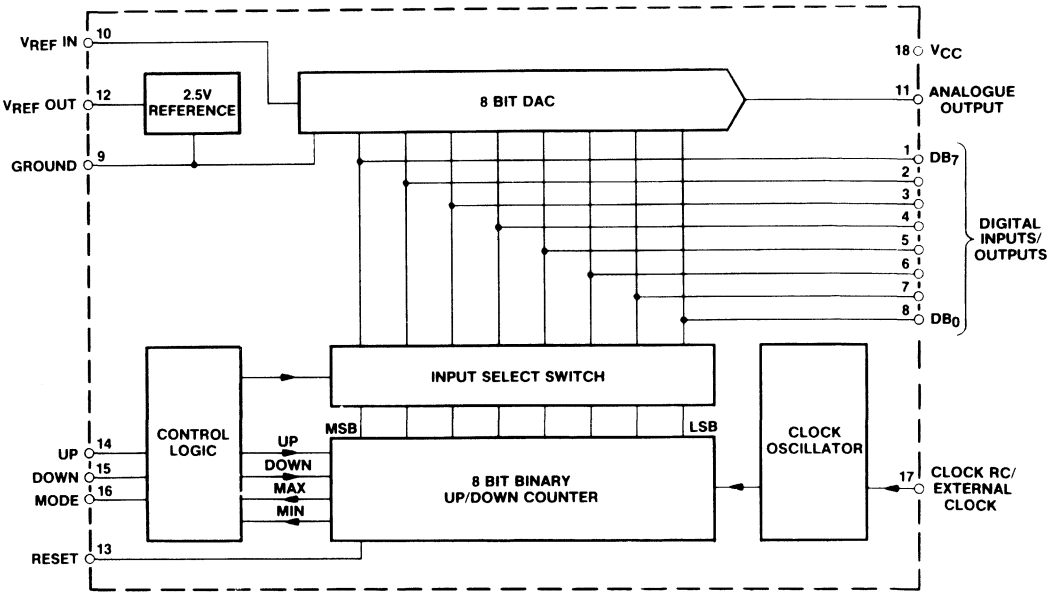


Fig.1 System diagram

ABSOLUTE MAXIMUM RATINGS

		Min.	Max.
Supply voltage		+7.0V	
Max. voltage, logic and V_{REF} inputs		V_{CC}	
Operating temperature range	ZN435E	0°C	+70°C
	ZN435J	−55°C	+125°C
Storage temperature range		−55°C	+125°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5V, V_{REF} = 1.5-3.0V, T_{amb} = +25°C unless otherwise specified).

Parameter	Min.	Typ.	Max.	Units	Conditions
D-A converter					
Resolution	8	–	–	Bits	
Linearity error	–	±0.25	±0.5	LSB	T_{min} T_{amb} T_{max}
Differential linearity error	±0.25		±1	LSB	
Zero error	–	5.0	10.0	mV	ZN435E All bits OFF
	–	5.0	10.0	mV	ZN435J
Settling time to 0.5LSB	–	500	–	ns	All bits OFF to ON
	–	800	–	ns	or vice versa
Full-scale output	2.545	2.550	2.555	V	All bits ON V_{REF} = 2.56V
Output resistance	–	4	–	kΩ	
Full-scale temperature coefficient	–	4	–	ppm/°C	Ext. V_{REF} = 2.56V
Reference voltage	0	–	3	V	

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	Min.	Typ.	Max.	Units	Conditions
On-chip voltage reference					
Output voltage	2.4	2.59	2.7	V	$R_{REF} = 390\Omega$
Slope resistance	–	2	4	Ω	$C_{REF} = 220nF$
Temperature coefficient of V_{REF}	–	50	–	ppm/°C	
Reference current	4	–	15	mA	
Counter (with external clock)					
High level threshold voltage V_{T+}	–	–	2.3	V	
Low level threshold voltage V_{T-}	1.7	–	–	V	
Maximum clock frequency	1	–	–	MHz	Note 1
On-chip clock					
Maximum frequency	500	–	–	kHz	
Clock frequency T.C.	–	100	–	ppm/°C	
Clock resistor	3.3	–	100	kΩ	
Clock capacitor	100	–	–	pF	
High level threshold voltage V_{T+}	–	4.6	–	V	
Low level threshold voltage V_{T-}	–	1.5	–	V	
Supply rejection	–	0.8	–	%/V	
Logic circuits					
BIT INPUTS					
High level input voltage V_{IH}	2.0	–	–	V	
Low level input voltage V_{IL}	–	–	0.8	V	
High level input current I_{IH}	–	–	−100	μA	$V_{IN} = 2.4V$
Low level input current I_{IL}	–	–	−220	μA	$V_{IN} = 0.4V$
BIT OUTPUTS					
High level output voltage V_{OH}	–	5.0	–		No load
Low level output voltage V_{OL}	–	0.1	–		
High level output voltage V_{OH}	2.4	–	–	V	$I_{IH} = -40\mu A$
Low level output voltage V_{OL}	–	–	0.4	V	$I_{IL} = 2.5mA$

Note 1: Speeds of up to 1.7MHz may be obtained by reducing the mark space ratio of the clock.

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	Min.	Typ.	Max.	Units	Conditions
CONTROL INPUTS					
High level input voltage V_{IH}	2	–	–	V	
Low level input voltage V_{IL}	–	–	0.8	V	
High level input current I_{IH}	–	–	–25	μA	$V_{IN} = 2.4V$
Low level input current I_{IL}	–	–	–95	μA	$V_{IN} = 0.4V$
Reset pulse width	200	–	–	ns	
Power supply					
Supply voltage	4.5	5	5.5	V	
Supply current	–	35	45	mA	$V_{CC} = 5.5V$

GENERAL CIRCUIT OPERATION

The ZN435 incorporates an 8-bit DAC based on a voltage switching R-2R ladder network. The reference voltage for this ladder may be derived from the on-chip precision bandgap reference, or an external reference voltage may be supplied.

The ZN435 also contains an 8-bit up/down counter and control logic. The DAC may receive its digital input data from the counter, the counter outputs being simultaneously available at an 8-bit I/O port. Alternatively the counter outputs may be inhibited and the I/O port used to feed data direct to the DAC inputs.

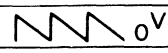
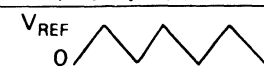
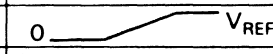
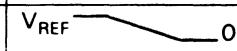
An on-chip oscillator is provided to drive the clock input of the up/down counter. The on-chip clock may be overridden by an external clock signal.

UP/DOWN COUNTER AND CONTROL LOGIC

The counter is a high-speed, synchronous up/down type, whose operation is determined by four control pins. The functions of the UP, DOWN and RESET inputs are fairly self explanatory, the MODE input determines the behaviour of the counter at zero and full-scale. When the MODE input is high the counter will reset to zero if it is clocked past full-scale in the UP direction and will reset to 255 if it is clocked past zero in the DOWN direction. When the MODE input is low the counter will stop on reaching full-scale or zero.

The normally invalid state of UP and DOWN inputs low simultaneously is also utilised in the ZN435. With the MODE input high and UP and DOWN inputs low the counter will cycle up and down continuously, reversing at full-scale and zero. With all three control inputs low the counter outputs are disabled and the DAC inputs accessible from the I/O port.

A truth table for the control inputs is given in Table 1.

Reset	Mode	Down	Up	Digital function	Analogue waveform
1	1	1	1	Counter stopped.	
1	1	1	0	Count up continuously.	
1	1	0	1	Count down continuously.	
1	1	0	0	Count up, reverse at F.S., count down, reverse at zero.	
1	0	1	1	Counter stopped.	
1	0	1	0	Count up, stop at F.S.	
1	0	0	1	Count down, stop at zero.	
X	0	0	0	DAC mode, counter output disabled. Counter can still be reset by taking reset input low.	
0	X	X	X	Counter reset. Does not affect analogue output in DAC mode.	

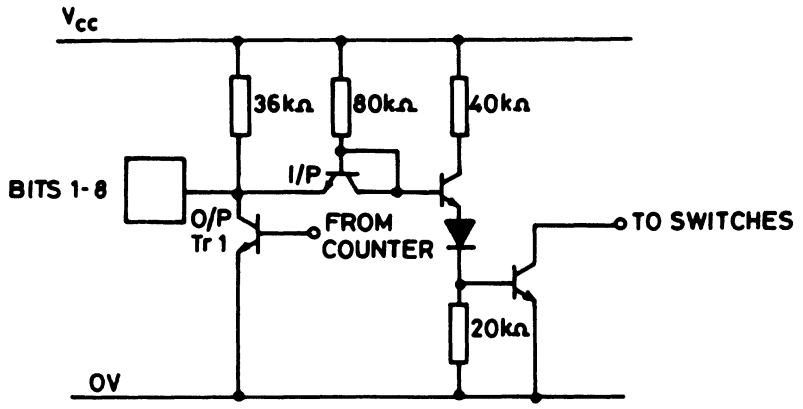


Fig. 2 Bit inputs/outputs

DATA PORT

One bit of the data port is shown in Fig. 2. The input/output pin is the junction of the counter output buffer and the DAC input buffer.

Normally the DAC is driven from the counter and the counter data is also available at the port. However, when the counter outputs are disabled the output transistors are turned off and the DAC inputs may be accessed from the data port.

The data port can drive or be driven from B-series CMOS and all TTL families.

CLOCK CIRCUIT

The on-chip clock circuit of the ZN435 is shown in Fig. 3.

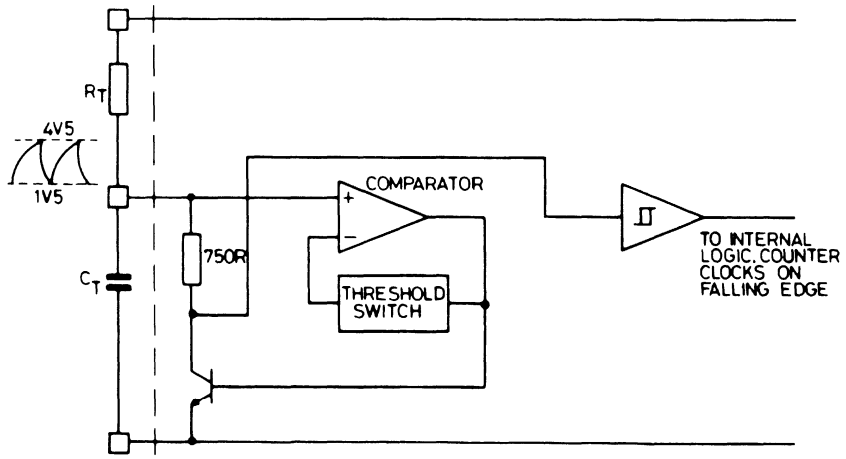


Fig. 3

The frequency of the clock is given by $f_{CLK} \simeq \frac{1}{2R_TC_T}$ (Hz, Ω, F)

Typical graphs of oscillator frequency versus resistor and capacitor values are given in Fig. 4.

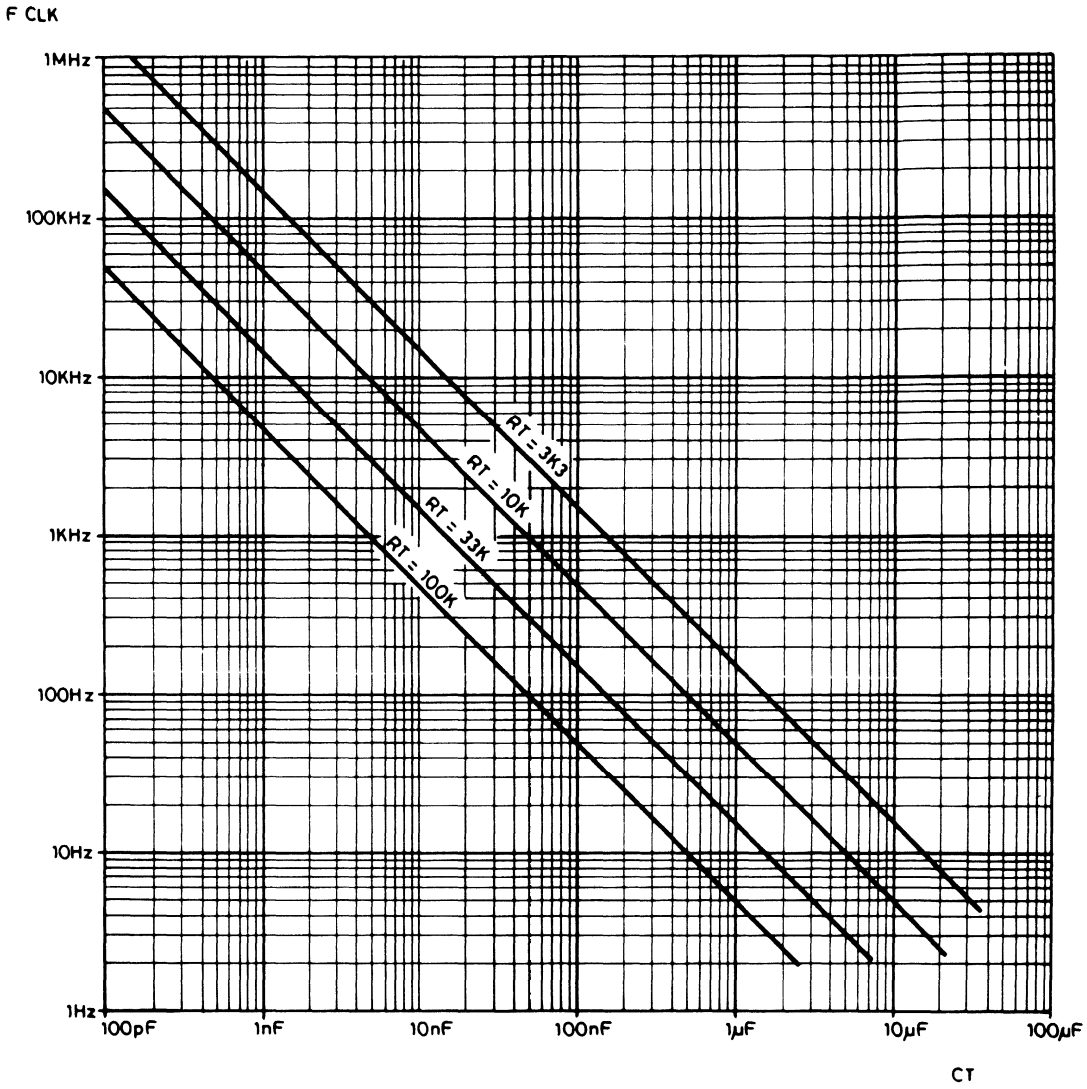


Fig. 4

The external capacitor C_T is charged via the external resistor R_T to the upper threshold of the comparator (about +4.5V with V_{CC} = +5V). The comparator turns on the discharge transistor to discharge C_T and switches its threshold to the lower value of about 1.5V. When the voltage on C_T has fallen to this level the comparator turns off the discharge transistor and the cycle repeats.

The clock can be overdriven from either a TTL totem-pole output (Fig. 5a), an open collector output (Fig. 5b), or a CMOS gate (Fig. 5c). In all three cases the V_{OH} of the driving gate must be attenuated to below 4.5V so that the internal discharge transistor is not turned on.

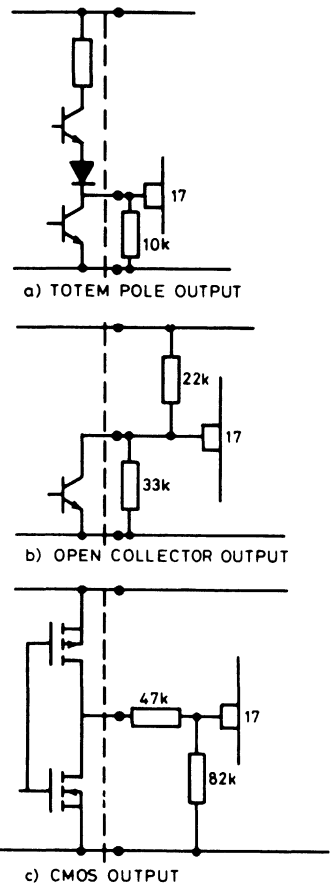


Fig. 5 Overdriving the clock input

ANALOGUE CIRCUITS

D-A converters

The DAC is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 6.

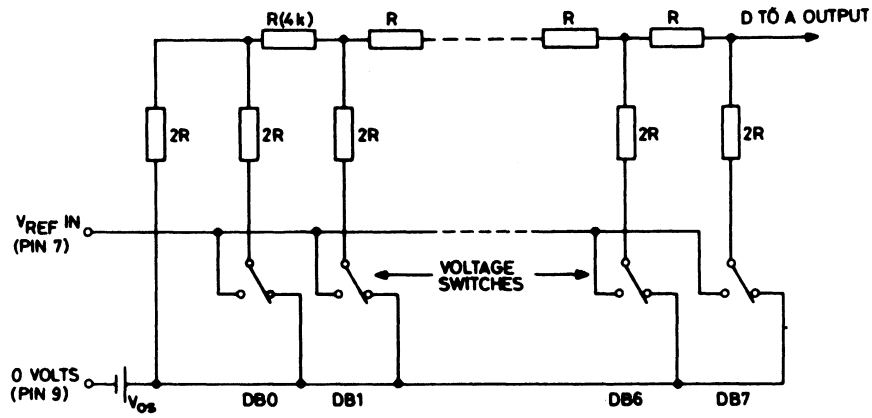


Fig. 6 R-2R ladder network

Each 2R element is connected to either 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (< 1mV). A binary weighted voltage is produced at the output of the R-2R ladder.

$$V_{OUT} = \frac{n}{256} (V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input from the counter or data port.

V_{OS} is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. The value of V_{OS} is typically 5mV for both the ZN435E and ZN435J. This offset will normally be removed by the setting up procedure and since the offset temperature coefficient is small the zero drift will be small. The DAC output range can be considered to be 0V to $V_{REF\ IN}$ with an output resistance R (4kΩ).

REFERENCE

On-chip reference

The internal reference is an active bandgap circuit which is equivalent to a 2.5V zener diode with a very low slope impedance (Fig. 7).

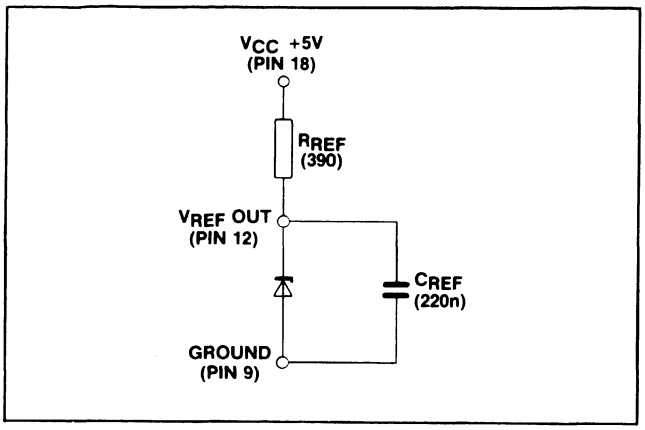


Fig. 7 Internal voltage reference

An external resistor (R_{REF}) should be connected between pins 12 and 18 to bias up the on-chip reference, whilst a stabilising/decoupling capacitor (C_{REF}) is required between pins 12 and 9.

To use the internal reference $V_{REF\ OUT}$ (pin 12) is connected to $V_{REF\ IN}$ (pin 10).

The recommended reference resistor of 390Ω will supply a nominal reference current of 6.4mA which is sufficient to drive the reference inputs of up to five ZN435's. Where several ZN435's are used in a system this useful feature can save up to four resistors and capacitors as well as reducing power consumption and giving excellent gain tracking.

APPLICATIONS

The applications of the ZN435 are too many and varied to detail in this data sheet. However a few basic configurations are illustrated. It should be noted that there is a danger of obtaining incorrect codes if the up/down control lines change at the same time as the active negative edge of the clock. Therefore if these control lines are changing asynchronously then extra circuitry should be used to prevent them changing at the negative edge of the clock. This is best achieved by latching these signals using positive edge triggered D-type flip-flops as is demonstrated in the circuit diagrams of Figs. 9 and 10.

WAVEFORM GENERATOR

The circuit of a low frequency waveform generator is illustrated in Fig. 8.

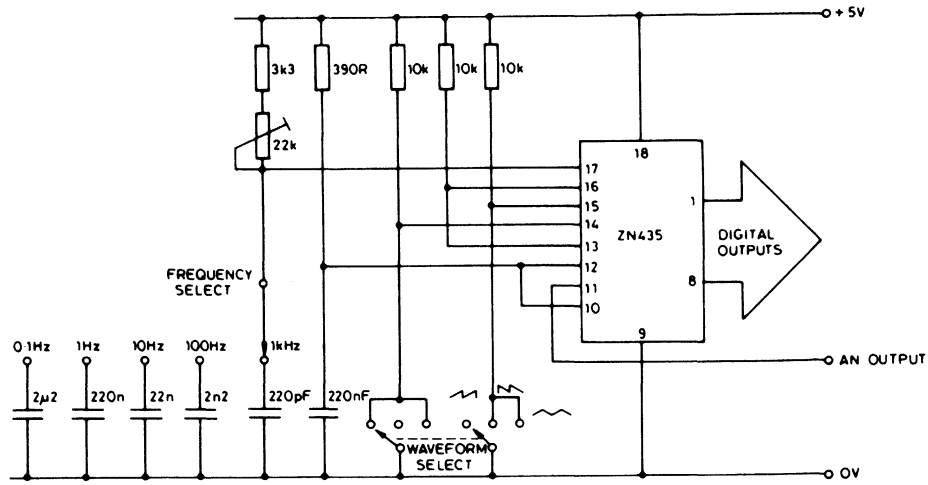


Fig. 8 Waveform generator

Note: The frequencies given above apply to the sawtooth waveforms. For the triangular waveforms divide the frequencies above by two.

This will produce stable, linear, sawtooth and triangle waveforms.

RAMP AND COMPARE A-D CONVERTER

A simple ramp and compare A-D converter can be constructed using the ZN435 as shown below.

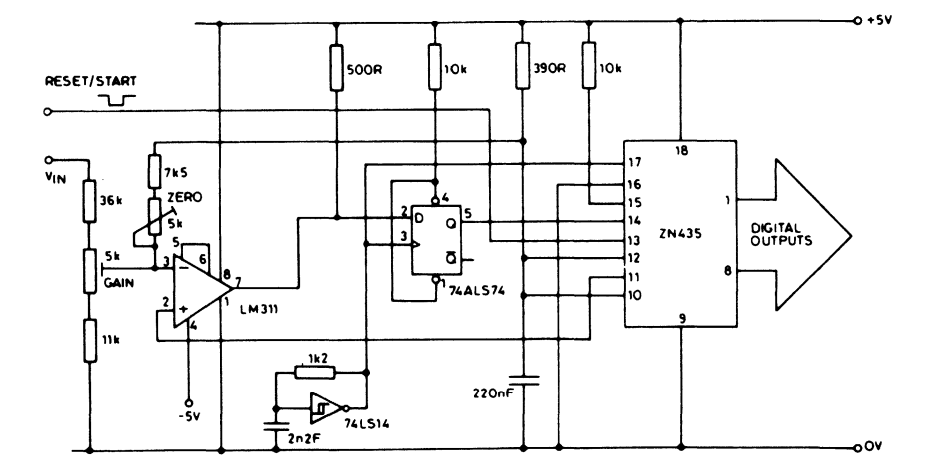


Fig. 9 Ramp and compare ADC

The counter is set to count up from zero, producing a positive going ramp at the analogue output. When the ramp voltage exceeds the analogue input the comparator output will go high, inhibiting the clock and stopping the counter. The converter can be reset and re-started by applying a low going pulse to the reset input. As the counter is constrained to count up only this circuit could also be used as an analogue peak detector. The analogue output of the ZN435 will hold indefinitely a voltage directly proportional to the highest applied input voltage.

The analogue input range is ± 10V. Other ranges may be accommodated by suitable choice of input resistors. Note that in this circuit the mode input is tied low to make the counter stop at full-scale. This prevents the counter cycling in the event of an overrange input.

Both this circuit and the following tracking converter circuit use high gain comparators. Therefore the usual precautions should be taken when constructing either circuit to prevent oscillation about the threshold, e.g. supply decoupling, careful track layout.

TRACKING A-D CONVERTER

The on-chip up/down counter allows the ZN435 to be configured as a tracking A-D converter, as shown in Fig. 10.

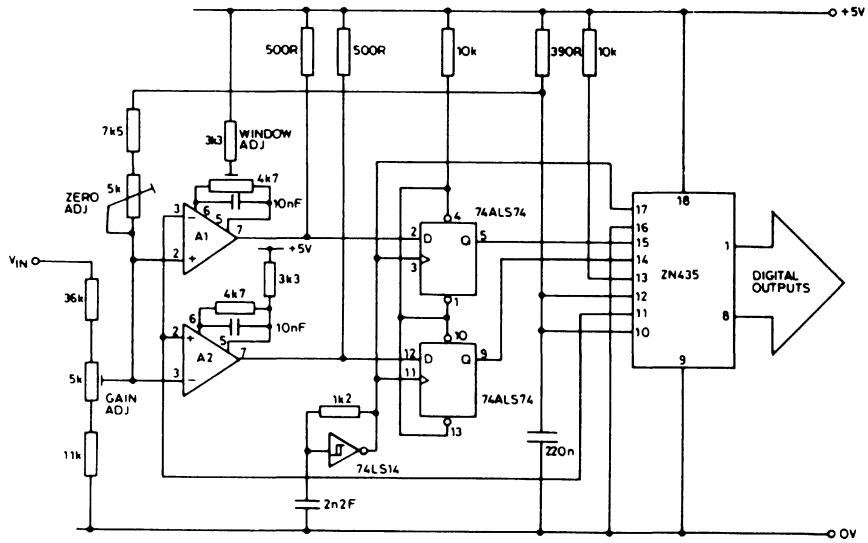


Fig. 10 Tracking ADC

In this circuit two LM311 op-amps are used to make a window comparator. This has a dead-band equal to one LSB of the DAC output (10mV), which is set by adjusting the offset of A1 until its threshold is 10mV above that of A2. This is easily achieved by applying a stable voltage at the input. Then with the ZN435 removed, applying a variable voltage to pin 11 on the ZN435 socket. By varying this voltage and monitoring the op-amp outputs the window can be adjusted so that the threshold of A1 is 10mV above that of A2.

Whenever the analogue voltage is above the threshold of A2 the counter will count up so that the DAC output increases to follow the analogue voltage. Whenever the analogue voltage is below the threshold of A1 the counter will count down so that the DAC output decreases to follow the analogue voltage. When the analogue voltage is between the two thresholds the outputs of A1 and A2 will be high and the counter will be stopped. Again the input voltage range is $\pm$ 10V, other ranges being possible by suitable choice of input resistors.

ZN436

LOW COST 6-BIT D-A CONVERTER

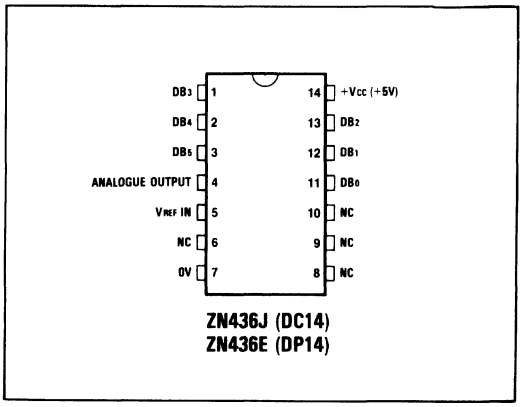
The ZN436 is a monolithic 6-bit D-A converter containing an R-2R ladder network of diffused resistors with precision bipolar switches.

FEATURES

- 6-Bit Accuracy
- TTL and 5V CMOS Compatible
- Single +5V Supply
- Settling Time 1 microsecond Typical
- Designed for Low-Cost Applications
- Commercial and Military Temperature Ranges

ORDERING INFORMATION

Device type	Operating temperature	Package
ZN436E	0°C to +70°C	DP14
ZN436J	-55°C to +125°C	DC14



Pin connections - top view

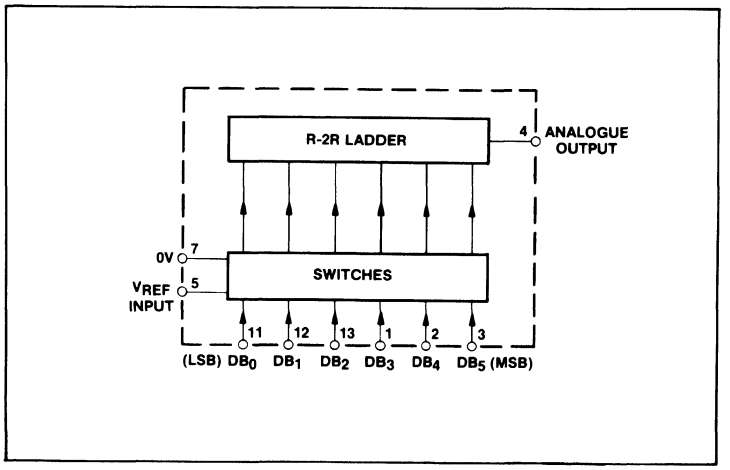


Fig.1 System diagram

INTRODUCTION

The ZN436 is an 6-bit D-A converter. It contains an advanced design of R-2R ladder network and an array of precision bipolar switches on a single monolithic chip.

The special design of ladder network results in full 6-bit accuracy using normal diffused resistors.

The converter is of the voltage switching type and uses an R-2R resistor ladder network as shown in Fig. 2.

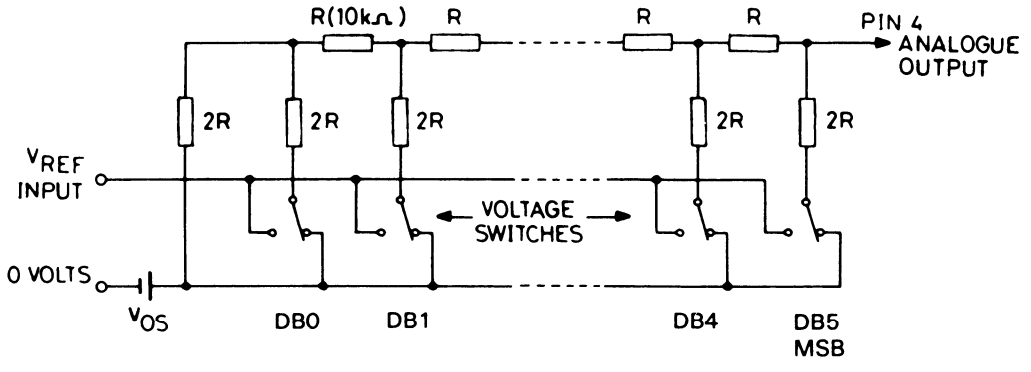


Fig. 2 The R-2R ladder network

Each 2R element is connected either to 0V or V_{REF} by transistor switches specially designed for low offset voltage (typically 1mV).

Binary weighted voltages are produced at the output of the R-2R ladder, the value depending on the digital number applied to the bit inputs.

An external fixed or varying reference is required which should have a slope resistance less than 2Ω

Suggested external reference sources are the ZN404 or one of the ZN458 range. Each ZN404 is capable of supplying up to five ZN436 circuits and this is increased to ten for the ZN458 range.

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC} . . . . . +7.0V
Max. voltage, logic and V_{REF} inputs . . . . . +5.5V
Storage temperature range . . . . . −55 to +125°C

CHARACTERISTICS (at $T_{amb} = 25°C$ and $V_{CC} = +5V$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Accuracy (useful resolution)						
ZN436J		6	–	–	bits	V_{REF} input = 2.0 to 3.0V
ZN436E		6	–	–	bits	
Non-linearity		–	–	±0.5	L.S.B.	Note 1
Differential non-linearity		–	±0.5	–	L.S.B.	Note 2
Settling time to 0.5 L.S.B.		–	1.0	–	μs	1 L.S.B. step
Settling time to 0.5 L.S.B.		–	2.0	–	μs	All bits ON to OFF or OFF to ON
Offset voltage ZN436J	V_{OS}	–	5.0	8.0	mV	All bits OFF note 1
ZN436E		–	3.0	5.0	mV	
V_{OS} temperature coefficient		–	5.0	–	μV/°C	
Full-scale output		2.510	2.520	2.530	V	All bits ON Ext. $V_{REF} = 2.560V$
Full-scale temp. coefficient		–	3.0	–	ppm/°C	Ext. $V_{REF} = 2.560V$
Non-linearity temp. coefficient		–	7.5	–	ppm/°C	Relative to F.S.R.

Notes:

1. The ZN436J differs from the ZN436E in the following respects:
   (a) For the ZN436J, the maximum linearity error may increase to ± 1LSB over the temperature ranges −55 to 0°C and +70 to +125°C.
   (b) Offset voltage. The difference is due to package lead resistance. This offset will normally be removed by the setting up procedure, and because the offset temperature coefficient is low, the specified accuracy will be maintained.
2. Monotonic over the full operating temperature range.

CHARACTERISTICS (cont.)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Analogue output resistance	R_o	–	10	–	kΩ	
External reference voltage		0	–	3.0	V	
Supply voltage	V_{CC}	4.5	–	5.5	V	
Supply current	I_S	–	5	9	mA	
High level input voltage	V_{IH}	2.0	–	–	V	
Low level input voltage	V_{IL}	–	–	0.7	V	
High level input current	V_{IH}	–	–	10	μA	V_{CC} = max., V_I = 2.4V
		–	–	100	μA	V_{CC} = max., V_I = 5.5V
Low level input current	I_{IL}	–	–	−0.18	mA	V_{CC} = max., V_I = 0.3V

APPLICATIONS

1. 6-bit D-A converter

The ZN436 gives an analogue voltage output directly from pin 4 therefore the usual current to voltage converting amplifier is not required. The output voltage drift, due to the temperature coefficient of the analogue output resistance R_O, will be less than 0.004% per °C (or 1LSB/100°C) if R_L is chosen to be $\geqslant$650kΩ.

In order to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary. Fig. 3 shows a typical scheme. To minimise temperature drift in this and similar applications the source resistance to the inverting input of the operational amplifier should be approximately 6kΩ. The calibration procedure is as follows:

i. Set all bits to OFF (low) and adjust R_2 until V_{OUT} = 0.000V.
ii. Set all bits to ON (high) and adjust R_1 until V_{OUT} = Nominal full-scale reading - 1LSB.
iii. Repeat i. and ii.

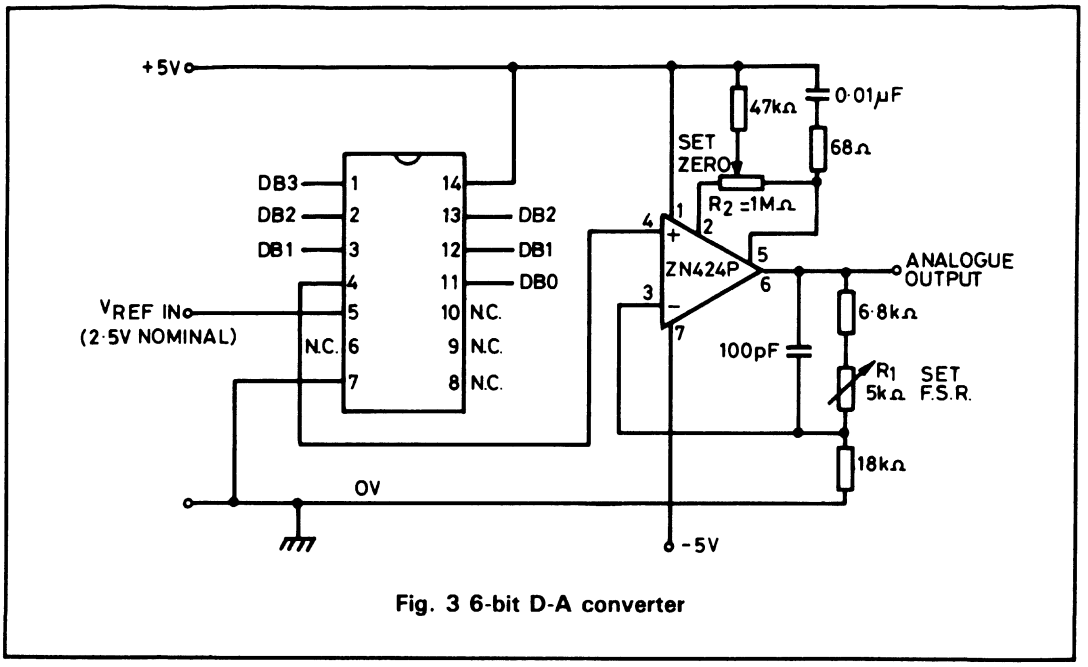


Fig. 3 6-bit D-A converter

Alternative output buffer using the 741

The following circuit, employing the 741 operational amplifier, may be used as the output buffer (Fig. 3).

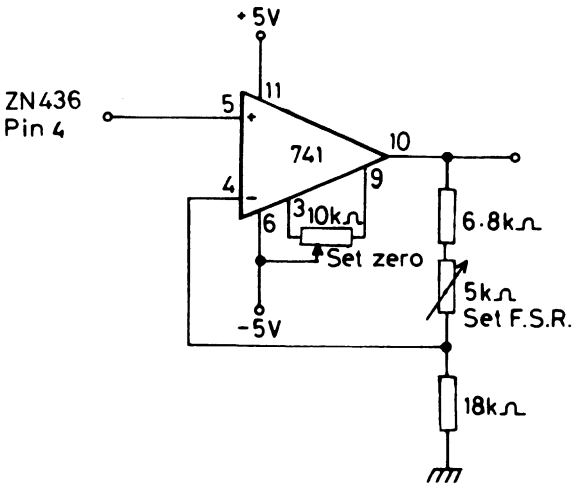


Fig.4 The 741 as output buffer

PLESSEY
Semiconductors

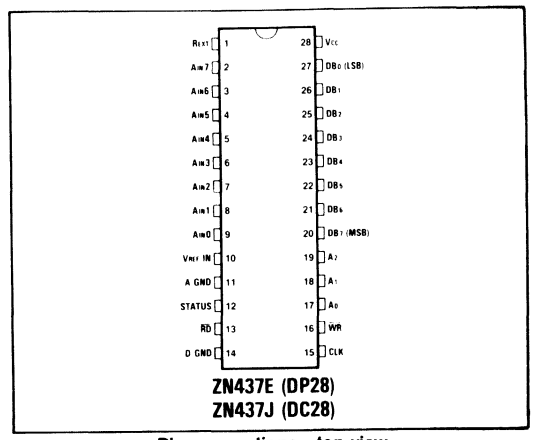
ZN437

MICROPROCESSOR-COMPATIBLE 8-BIT, 8 CHANNEL DATA ACQUISITION SYSTEM

The ZN437 is an 8-bit, 8 channel data acquisition system designed to easily interface to most popular microprocessors. It consists of an 8-bit successive approximation A-D converter, an 8 channel multiplexer, 8 x 8 bit RAM, clock pre-divider, control logic and double buffered latches with 3-state outputs.

The ZN437 can be programmed for any one of four possible conversion modes: 'single shot' conversion on a named channel; 'continuous conversion' on a named channel; a 'single shot' conversion on all channels; and continuous conversion on all channels.

Using the successive approximation technique, the result of each channel conversion is loaded into the correct location of the 8 x 8 bit RAM. The address bus ($A_2 \rightarrow A_0$) is used to select the channel data to be read with the double buffered output latches allowing data to be read at any time irrespective of the conversion status.



ZN437E (DP28)
ZN437J (DC28)

Pin connections - top view

FEATURES

- Choice of Linearity: ±0.5, ±1 LSB
- 16 microseconds Conversion Time
- 8 Analogue Inputs
- On-Chip 8 x 8 RAM
- Four Possible Conversion Modes
- Versatile Microprocessor Interfacing with Double Buffered Output Latch
- Microprocessor, TTL and CMOS Compatible
- Accepts Microprocessor Clocks up to 4MHz
- ROM Type Operation
- Commercial or Military Temperature Ranges

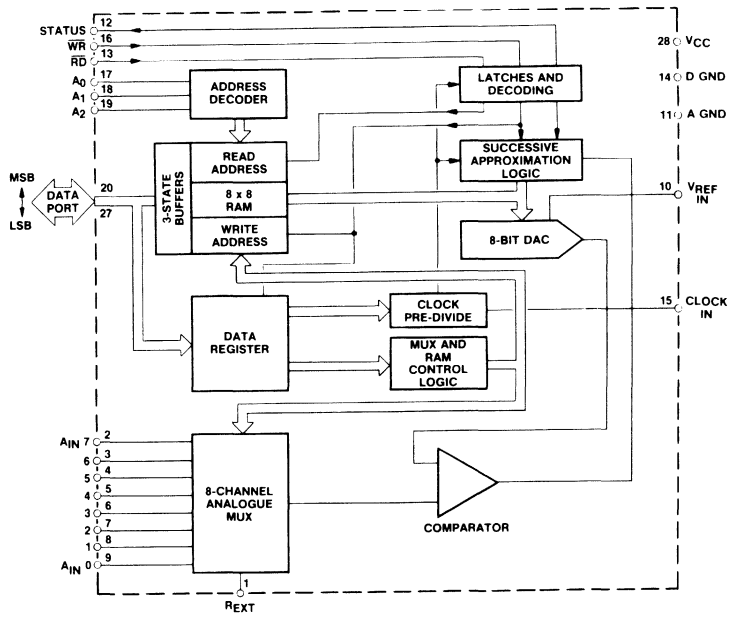


Fig.1 System diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	+7V
Maximum voltage, logic and V_{REF} inputs	V_{CC}
Operating temperature range	0°C to +70°C (ZN437E)
	-55°C to +125°C (ZN437J)
Storage temperature range	-55°C to +125°C

ELECTRICAL CHARACTERISTICS (at V_{CC} = 5V, T_{amb} = 25°C and f_{CLK} = 500KHz unless otherwise stated).

Parameter	T_{amb} = +25°C			Over specified Temp. range		Units	Conditions
	Min.	Typ.	Max.	Min.	Max.		
ZN437-8							
Linearity error	–	–	±0.5	–	±0.5	LSB	
Differential linearity error	–	–	±0.75	–	±0.75	LSB	
ZN437-7							
Linearity error	–	–	±1	–	±1	LSB	
Differential linearity error	–	–	±1	–	±1	LSB	
ALL TYPES							
Zero transition	–	10	–	–	–	mV	ZN437E, Ext.
(00000000→00000001)	–	10	–	–	–	mV	ZN437J, Ref.
Full-scale transition	–	2.550	–	–	–	V	ZN437E, =
(11111110→11111111)	–	2.550	–	–	–	V	ZN437J, 2.56V
Linearity temperature coefficient		±3 typ.				ppm/°C	Ext. Ref. = 2.50V
Differential linearity temperature coefficient		±6 typ.				ppm/°C	
Gain temperature coefficient		±10 typ.				ppm/°C	
Offset temperature coefficient		±7 typ.				ppm/°C	
Resolution	8	–	–	–	–	Bits	
Conversion time	16	–	–	–	–	μs	per channel
Supply rejection	–	0.2	–	–	–	%/V	
Supply voltage	4.5	5.0	5.5	4.5	5.5	V	
Supply current	–	45	–	–	–	mA	Outputs in high impedance state
Power consumption	–	225	–	–	–	mW	
Reference input range	1.5	–	3.0	–	–	V	
Ladder output impedance	–	2.7	–	–	–	KΩ	
MULTIPLEXED INPUTS							
Input current	–	10	–	–	–	nA	V_{in} = +3V, R_{ext} = 1.8KΩ
Input resistance	–	10	–	–	–	MΩ	
Tail current	–	1.1	–	–	–	mA	R_{ext} = 1.8KΩ, V_{EE} = -5V
Negative supply	-3	-5	-30	-3	-30	V	
Input voltage, V_{in}	-0.5	–	+3.5	-0.5	+3.5	V	

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	$T_{amb} = +25°C$			Over specified temp. range		Units	Conditions
	Min.	Typ.	Max.	Min.	Max.		
EXTERNAL VOLTAGE REFERENCE							
Output voltage	1.5	–	3.0	–	–	V	
Slope impedance	–	0.75	–	–	–	Ω	
ZN437 current drain from $V_{REF\ IN}$	–	–	1.0	–	–	mA	Note 1
Output voltage temperature coefficient	–	50	–	–	–	ppm/°C	
EXTERNAL CLOCK							
Clock frequency	–	–	4.0	–	4.0	MHz	Pre-divide set to ÷8
High level I/P voltage V_{IH}	2.0	–	–	2.0	–	V	
Low level I/P voltage V_{IL}	–	–	0.8	–	0.8	V	
High level I/P current I_{IH}	–	200	–	–	–	μA	$V_{CC} = 5.5V$ $V_{IN} = 4V$
Low level I/P current I_{IL}	–	−160	–	–	–	μA	$V_{CC} = 5.5V$ $V_{IN} = 0.8V$
LOGIC $\overline{WR}$, $\overline{RD}$, A_2, A_1, A_0 INPUTS							
High level I/P voltage V_{IH}	2.0	–	–	2.0	–	V	
Low level I/P voltage V_{IL}	–	–	0.8	–	0.8	V	
High level I/P current I_{IH}	–	220	–	–	–	μA	$V_{CC} = +5.5V$ $V_{IN} = +5.5V$
High level I/P current I_{IH}	–	35	–	–	–	μA	$V_{CC} = +5.5V$ $V_{IN} = +2.4V$
Low level I/P current I_{IL}	–	−200	–	–	–	μA	$V_{CC} = +5.5V$ $V_{IN} = +0.4V$
DATA INPUTS/OUTPUTS							
High level I/P voltage V_{IH}	2.0	–	–	2.0	–	V	
Low level I/P voltage V_{IL}	–	–	0.8	–	0.8	V	
High level I/P current I_{IH}	–	40	–	–	–	μA	$V_{CC} = +5.5V$ $V_{IN} = +5.5V$
High level I/P current I_{IH}	–	10	–	–	–	μA	$V_{CC} = +5\ 5V$ $V_{IN} = +2.4V$
Low level I/P current I_{IL}	–	−100	–	–	–	μA	$V_{CC} = +5.5V$ $V_{IN} = +0.4V$
High level output voltage V_{OH}	2.4	–	–	2.4	–	V	$I_{OH\ MAX}$
Low level output voltage V_{OL}	–	–	0.4	–	0.4	V	$I_{OL\ MAX}$
High level output current I_{OH}	–	–	−800	–	–	μA	
Low level output current I_{OL}	–	–	2.0	–	–	mA	

Note 1: When bipolar operation is employed , the external component connections will present an additional load to the reference. See section on bipolar operation.

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	T_{amb} = +25°C			Over specified temp. range		Units	Conditions
	Min.	Typ.	Max.	Min.	Max.		
Enable/disable delay times							
TE1	90	–	220	–	–	ns	see fig.9
TE0	60	–	120	–	–	ns	
TD1	80	–	160	–	–	ns	
TD0	60	–	110	–	–	ns	
Write pulse width	135	–	–	–	–	ns	
$\overline{WR}$ I/P to STATUS O/P high	–	280	360	–	–	ns	
Read pulse width	220	–	–	–	–	ns	
$\overline{RD}$ high to STATUS high	–	240	400	–	–	ns	
Data set up prior to $\overline{WR}$ going low	−55	–	–	–	–	ns	
Data hold after $\overline{WR}$ going high	10	–	–	–	–	ns	
Address inputs stable prior to $\overline{RD}$ going low	10	–	–	–	–	ns	
Address inputs stable after $\overline{RD}$ going high	10	–	–	–	–	ns	

GENERAL CIRCUIT DESCRIPTION

The ZN437 accepts eight analogue inputs and by using an eight bit 'Control Word', can be programmed to convert in any one of four different operational modes: 'Single shot' conversion on a named channel; 'continuous conversion' on a named channel; a 'single shot' conversion on all channels; and continuous conversion on all channels. Each channel can be converted into an eight bit binary word using the successive approximation technique with the result of the conversion being loaded into the correct location of the 8 × 8 bit RAM. The 'Control Word' is loaded into the device on the negative edge of the $\overline{WR}$ input pulse. The conversion mode, input channel (modes 1 and 2 only) and clock pre-divide are selected. The STATUS output goes high to indicate the beginning of the conversion and the DAC input is set to the MSB. The multiplexer selects one input channel at a time (dependent on the Control Word) on which a conversion is to be performed. The output of the DAC is compared to the unknown analogue signal be means of the comparator. If the analogue input is larger, the MSB is left in the circuit and if not the MSB is removed. On the second clock pulse this sequence is repeated for the next most significant bit and so on until all eight bits have been compared. On the 8th negative clock edge the STATUS goes low indicating that the conversion is complete and the RAM is updated.

Data can be read from the ZN437 by placing the correct channel address on pins A_0, A_1, A_2 and by taking $\overline{RD}$ low. The negative edge of the $\overline{RD}$ pulse powers up the required channel's RAM location and enables the 3-state outputs. The RAM is kept in a low power standby mode when not being accessed. Double buffered latches on-chip allow the outputs to be enabled at any time, irrespective of the conversion status and valid data will always be presented to the data bus, this data will be the result of the most recent conversion on that channel, therefore the $\overline{RD}$ signal can be completely asynchronous with respect to the STATUS. The data port (bi-directional input/output port) dictates that $\overline{WR}$ and $\overline{RD}$ must never be active at the same time as this will lead to conflict on the bus.

CONTROL LOGIC

For the ZN437 to function correctly when powered up, an 'Initialisation' word must be sent to the device with $\overline{START}$, SQ and CY set high. This will set up the device for immediate operation.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Control Word	$\overline{START}$	CLOCK PRE-DIVIDER		$\overline{CY}$	$\overline{SQ}$	ANALOGUE INPUT		
'Initialisation' word	1	X	X	1	1	X	X	X

X = do not care

The device is now set up for initiating the first conversion.

All operations of the ZN437 are controlled by the 'Control Word'. (See above).

ANALOGUE INPUT: 3-bit code for Analogue Input selection. Used only when doing a conversion on a named input.

SEQUENCE $\overline{SQ}$: Active low, indicates a sequencing action through all eight channels.

CYCLING $\overline{CY}$: Active low, indicates a continuous conversion of one or all channels

CLOCK PRE-DIVIDER: Two bit code enables ÷ 1, ÷ 2, ÷ 4 and ÷ 8 of the clock frequency.

$\overline{START}$: Initiates a conversion by a high to low transition.

The $\overline{WR}$ signal is used by the device to latch in the Control Word currently sat on the data bus, data being latched on the rising edge of the $\overline{WR}$ signal.

Note that a $\overline{WR}$ signal is always required to change or input a new Control Word.

DB6	DB5	DIVISION RATIO
1	1	1
1	0	2
0	1	4
0	0	8

CLOCK PRE-DIVIDE SELECTION

CONVERSION TIMING

The ZN437 will accept a low going $\overline{WR}$ pulse, which will load in the 'Control Word' and start the conversion sequence. The $\overline{WR}$ pulse can be completely asynchronous with respect to the clock and will produce valid data between 8 and 9 clock cycles later depending on the relative timing of the clock and convert signals. Timing diagrams for a conversion are shown in Fig. 2.

The $\overline{WR}$ pulse can be as short as 150ns, there is no maximum limit, but the control word should not be changed and $\overline{RD}$ should not be taken low whilst $\overline{WR}$ is low. The MSB must be allowed to settle for at least 2.0μs before the MSB decision is made. To ensure that this criterion is met even with short write pulses the converter waits for a falling clock edge before commencing with the conversion. This ensures that the MSB is allowed to settle for at least a full clock period or 2.0μs at maximum 500KHz clock frequency.

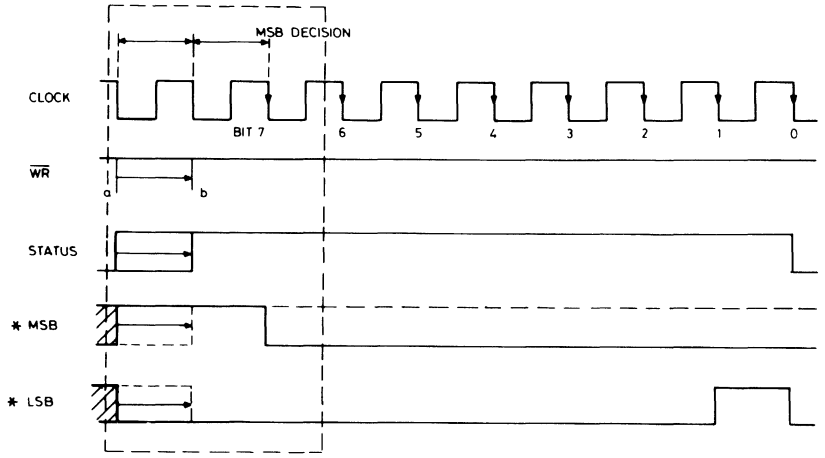


Fig. 2a

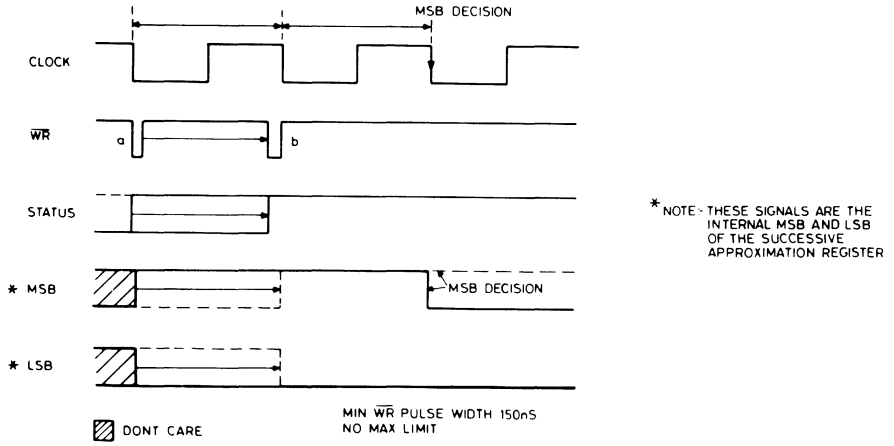


Fig. 2b

Fig. 2 Timing diagram

CONVERSION MODES

The ZN437 has four possible conversion modes:

1. A single conversion on a specified analogue input.
2. A continuous conversion on a specified analogue input.
3. A single conversion of all eight channels.
4. A continuous conversion of all eight channels.

Any of the four modes can be selected by the $\overline{SQ}$ and $\overline{CY}$ bits in the control word.

1. A single conversion on a specified analogue input.

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	CLOCK PRE-DIVIDER		1	1	ANALOGUE INPUT		
$\overline{START}$	SELECT DIVISION RATIO		$\overline{CY}$	$\overline{SQ}$	SELECT CHANNEL		

Control Word for Mode 1

One conversion is initiated on the specified channel by $\overline{START}$ (DB7) going low. STATUS output is forced high and the internal clock started. At the end of the conversion the STATUS output returns low, on-chip logic detects that $\overline{SQ}$ and $\overline{CY}$ are high and stops the internal clock. Note at this point the Control Word is automatically reset to all 1's (because a 1→0 transistion is required on DB7 to start the device). Hence the device is all set up waiting for a new Control Word.

A timing diagram for this mode is shown in Fig. 3.

2. A continuous conversion on a specified analogue input.

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	CLOCK PRE-DIVIDER		0	1	ANALOGUE INPUT		
$\overline{START}$	SELECT DIVISION RATIO		$\overline{CY}$	$\overline{SQ}$	SELECT CHANNEL		

Control Word for Mode 2

A continuous conversion is initiated on the specified channel by $\overline{START}$ (DB7) going low. The STATUS output is forced high and the internal clock started. At the end of each conversion, internal logic checks to see if $\overline{CY}$ is still 0, if it is, it will continue with the next conversion. To stop the conversion process, a new Control Word must be written to the device which has $\overline{SQ}$ and $\overline{CY}$ both high. This can occur at any time in the conversion cycle with the device completing the current conversion before stopping.

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	CLOCK PRE-DIVIDER		1	1	ANALOGUE INPUT		
$\overline{START}$	NO CHANGE		$\overline{CY}$	$\overline{SQ}$	NO CHANGE		

Stop Control Word for Mode 2

At the end of the conversion the control word is again automatically reset to all 1's.

A timing diagram for this mode is shown in Fig. 4.

3. A single conversion of all eight channels.

DB7	DB6 DB5	DB4	DB3	DB2 DB1 DB0
0	CLOCK PRE-DIVIDER	1	0	ANALOGUE INPUT
$\overline{START}$	SELECT DIVISION RATIO	$\overline{CY}$	$\overline{SQ}$	NOT USED IN THIS MODE

Control Word for Mode 3

Conversions are initiated by $\overline{START}$ (DB7) going low. The STATUS output is forced high and the internal clock started. $\overline{SQ}$ being low causes the device to sequence through all eight channels starting at channel 0 going through to channel 7. After the conversion on channel 7 the device automatically stops, resetting the Control Word to all 1's ready for the next Control Word.

A timing diagram for this mode is shown in Fig. 5.

4. Continuous conversion of all eight channels.

DB7	DB6 DB5	DB4	DB3	DB2 DB1 DB0
0	CLOCK PRE-DIVIDER	0	0	ANALOGUE INPUT
$\overline{START}$	SELECT DIVISION RATIO	$\overline{CY}$	$\overline{SQ}$	NOT USED IN THIS MODE

Start Control Word for Mode 4

Conversions are initiated by $\overline{START}$ (DB7) going low. The STATUS output is forced high. In this mode we sequence through each channel starting at channel 0. After the conversion on channel 7 the device goes back to channel 0 and starts again.

There are two ways to stop the conversion mode:

A. A new Control Word is written to the device with $\overline{SQ}$, $\overline{START}$ and $\overline{CY}$ high. This will force the device to stop converting at the end of the current channel conversion.

DB7	DB6 DB5	DB4	DB3	DB2 DB1 DB0
1	CLOCK PRE-DIVIDER	1	1	ANALOGUE INPUT
$\overline{START}$	NO CHANGE	$\overline{CY}$	$\overline{SQ}$	NOT USED IN THIS MODE

Stop Control Word A for Mode 4

B. A new Control Word is written to the device with $\overline{SQ} = 0$, $\overline{START} = 1$, and $\overline{CY} = 1$. In this case the device will contine until it has completed channel 7 then it will stop automatically (similar operation to mode 3) resetting the Control Word to all 1's ready for the next Control Word.

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	CLOCK PRE-DIVIDER		1	0	ANALOGUE INPUT		
$\overline{START}$	NO CHANGE		$\overline{CY}$	$\overline{SQ}$	NOT USED IN THIS MODE		

Stop Control Word B for Mode 4

A timing diagram for this mode is shown in Fig. 6.

READ CHANNEL SELECTION

The following table shows the truth table for the address inputs (A_2, A_1, A_0). The input address is used when $\overline{RD}$ goes low. When $\overline{RD}$ is high the input address is locked out.

A_2	A_1	A_0	CHANNEL TO BE READ
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

ANALOGUE INPUT CHANNEL SELECTION

The following table shows how to select an Analogue Input channel using DB2,DB1 & DB0.

DB2	DB1	DB0	CHANNEL SELECTED
0	0	0	0
1	0	0	1
0	1	0	2
1	1	0	3
0	0	1	4
1	0	1	5
0	1	1	6
1	1	1	7

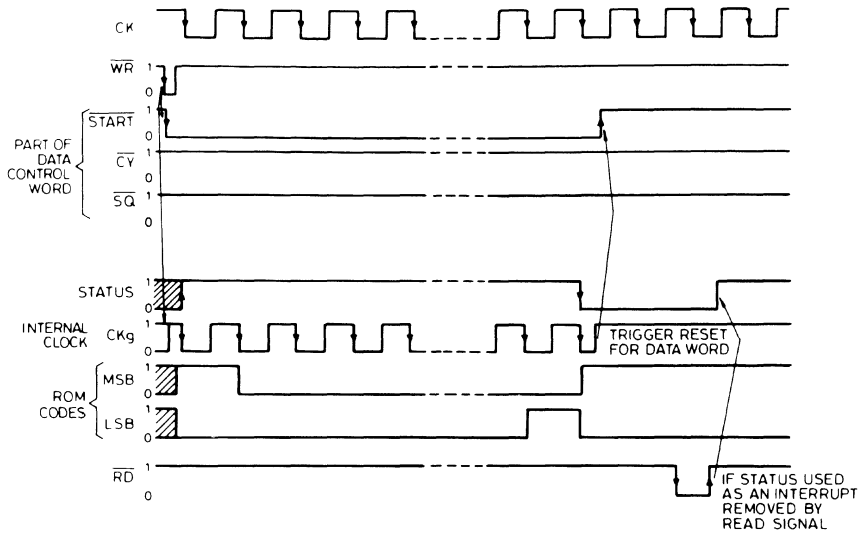


Fig. 3 Single conversion on a named channel

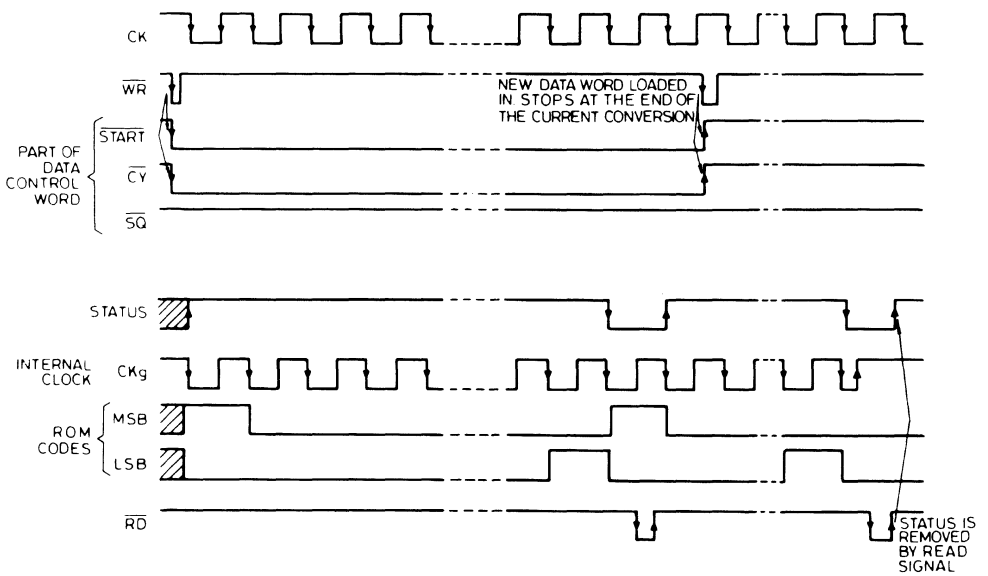


Fig. 4 Continuous conversion on a named channel

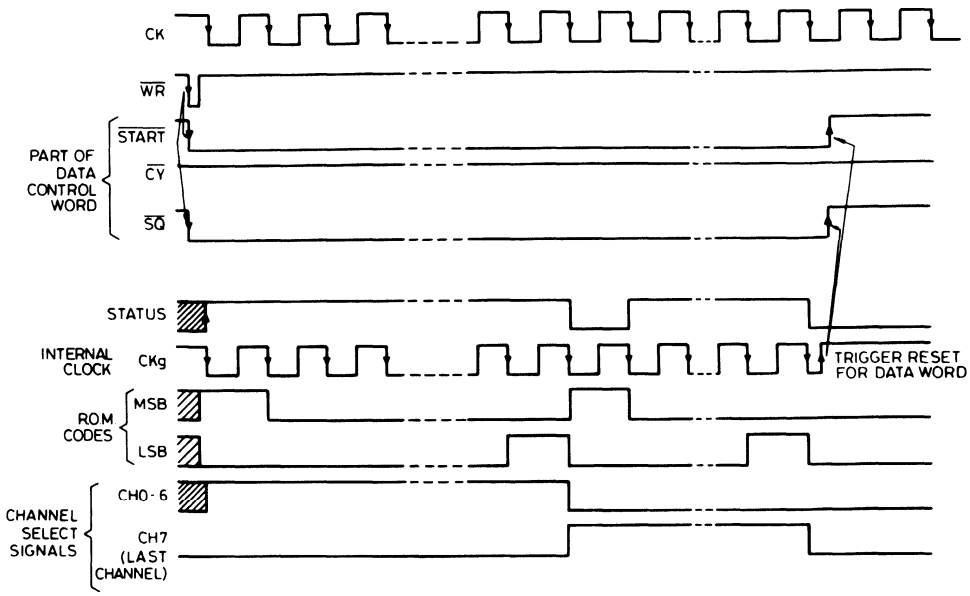


Fig.5 A single conversion of all channels

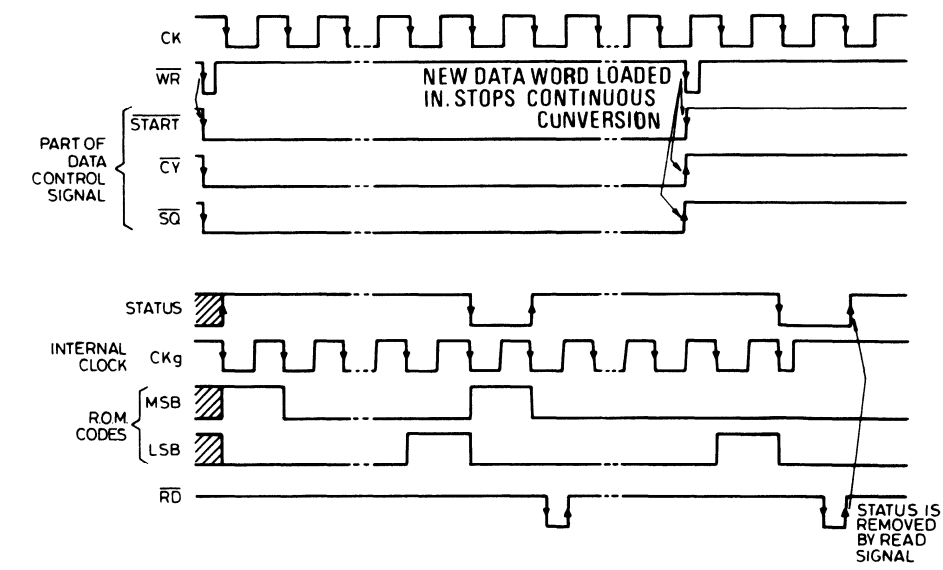


Fig. 6 Continuous conversion of all channels

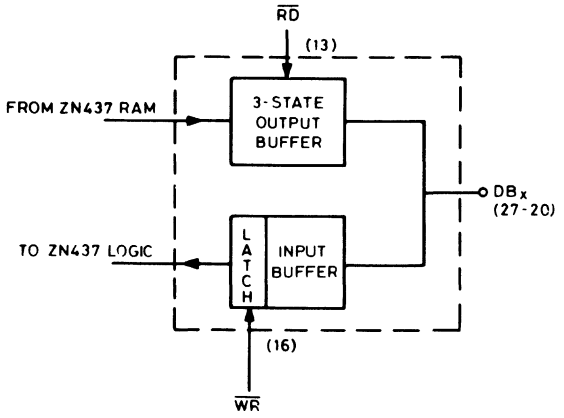


Fig. 7 ZN437 data port

DATA PORT

The ZN437 has eight data ports. These are bi-directional input/output ports, see Fig. 7.

The data outputs are provided with 3-state buffers to allow connection to a common data bus. An equivalent circuit is shown in Fig. 8.

Whilst the $\overline{RD}$ input is high both output transistors are off.

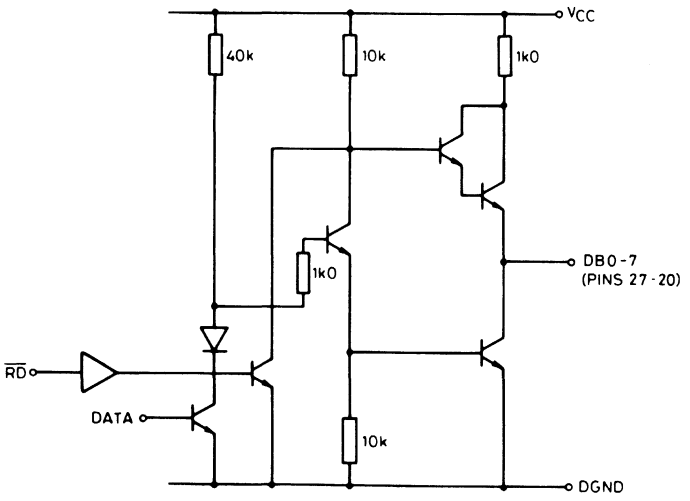
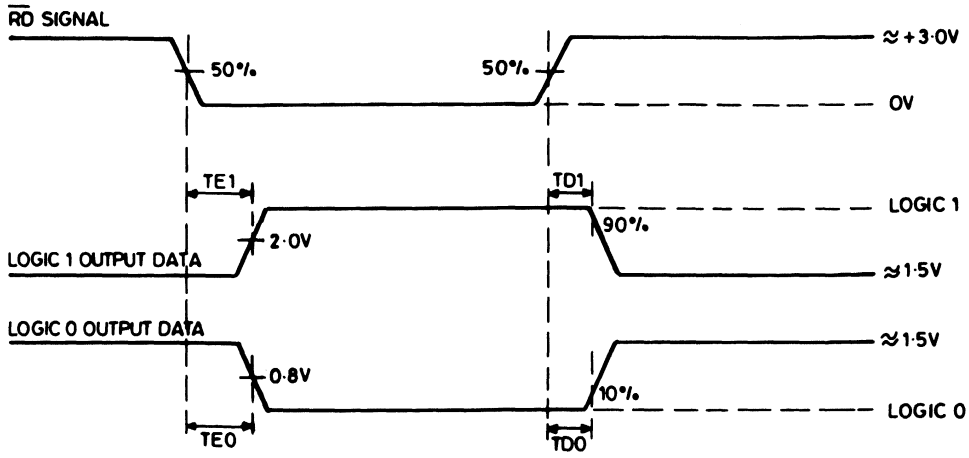


Fig. 8 Data outputs



TE = RD ENABLE DELAY TIME (CL = 50pF)
TD = RD DISABLE DELAY TIME (CL = 10pF)

Fig. 9a Output enable/disable delays

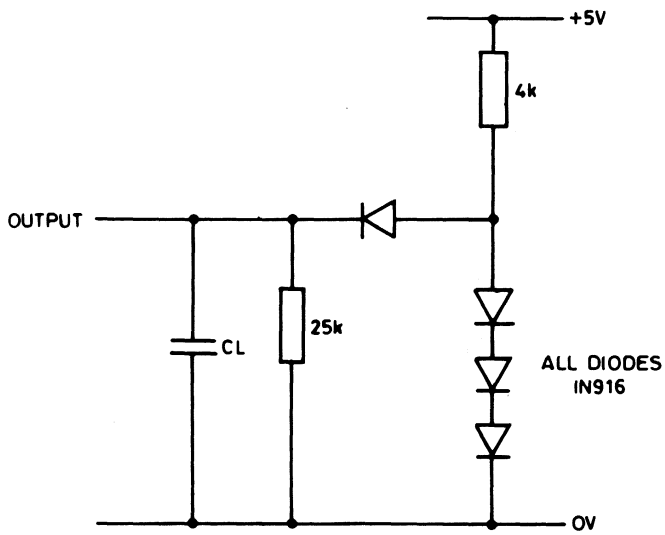


Fig. 9b Output load circuit

CLOCK INPUT

The ZN437 clock input must be driven externally with TTL/CMOS compatible signals. The device will accept microprocessor clocks up to 4MHz, here the clock pre-divider will need setting to ÷8.

ANALOGUE CIRCUITS

Reference

The ZN437 requires an external reference in the range +1.5 to +3.0V which is connected between $V_{REF\ IN}$ (pin 10) and analogue GND (pin 11). The slope resistance of such a reference source should be less than 2.5Ω or 2.5Ω/n where n is the number of converters supplied.

Suggested reference sources are the REF25Z for commercial applications and the ZNREF025A1 for military temperature range operation.

Ratiometric operation

If the output from a transducer varies with its supply then an external reference for the ZN437 should be derived from the same supply. The external reference can vary from +1.5 to +3.0V. The ZN437 will operate if $V_{REF\ IN}$ is less than +1.5V but reduced overdrive to the comparator will increase its delay and so the conversion time will need to be increased.

D-A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 10. Each element is connected to either 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (1mV).

A binary weighted voltage is produced at the output of the R-2R ladder:

$$\text{D-A output} = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input to the D-A from the successive approximation register.

V_{OS} is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. This offset will normally be removed by the setting up procedure and since the offset temperature coefficient is low (7ppm/°C) the effect on accuracy will be negligible.

The D-A output range can be considered to be 0 to V_{REFIN} − 1LSB through an output resistance R(2K7).

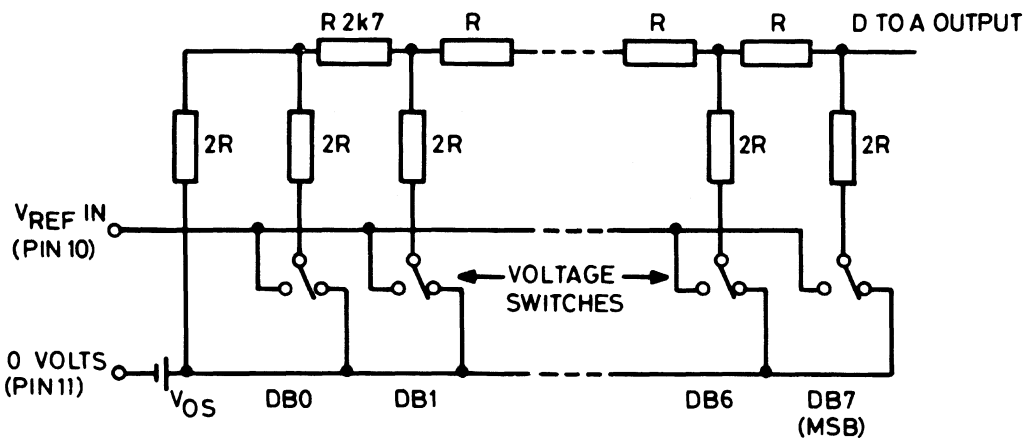


Fig. 10 R-2R Ladder Network

MULTIPLEXED INPUTS AND COMPARATOR

The ZN437 contains eight analogue inputs which are fed into a multiplexer. The required channel is then selected and fed into the comparator. The multiplexer is digitally controlled by the information contained in the 'Control Word' (bits DB0 – DB4). This allows the multiplexer to behave in any one of the four system operating modes as previously described.

The ZN437 contains a fast comparator. The equivalent input circuit for one channel is shown in Fig. 11. A negative supply voltage is required to supply the tail current of the input stages which is a nominal 1.1mA with $V_{EE} = -5V$ and $R_{EXT} = 1.8K\Omega$.

A list of suitable resistors for different supply voltages is given in the adjacent table.

V_{EE} (volts)	R_{EXT} (KΩ)
-3	–
-5	1.8
-10	6.2
-12	7.5
-15	11
-20	15
-25	20
-30	24

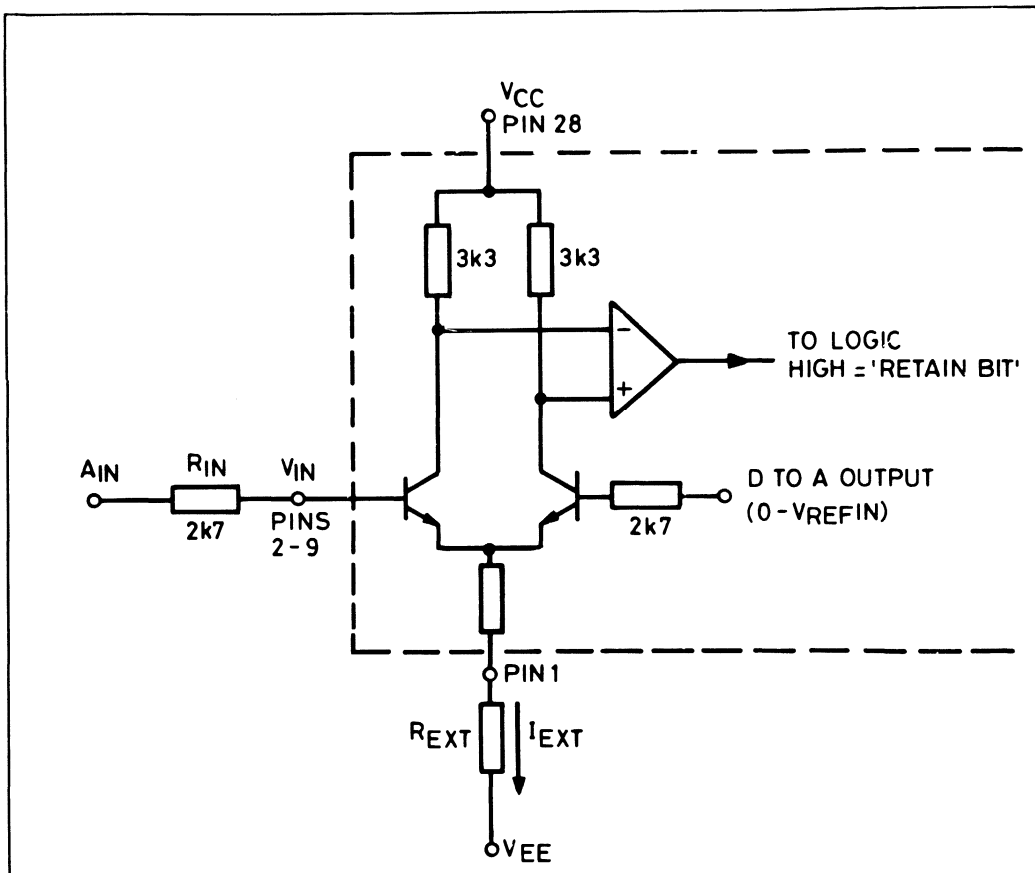


Fig. 11 Analogue input equivalent circuit for a channel

ANALOGUE INPUT RANGES

The basic connection of the ZN437, shown in Fig. 12, has an analogue input range 0 to V_{REF} which, in some applications, may be made available from previous signal conditioning/ scaling circuits. Input voltage ranges greater than this are accommodated by providing an attenuator on the comparator input, whilst for smaller input ranges the signal must be amplified to a suitable level.

Bipolar input ranges are accommodated by off-setting the analogue input ranges so that the input stage always sees a positive input voltage.

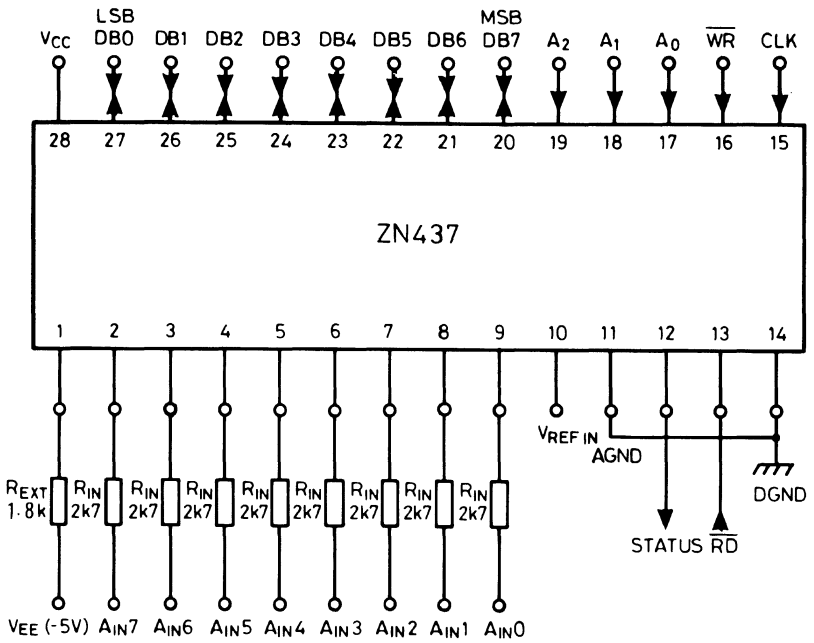


Fig. 12 External components for basic operation

UNIPOLAR OPERATION

The general connection for unipolar operation is shown in Fig. 13.

The values of R_1 and R_2 are chosen so that $V_{IN} = V_{REF\ IN}$ when the Analogue Input (A_{IN}) is at full-scale.

The resulting full-scale range is given by: $A_{IN}FS = \left(1 + \frac{R_1}{R_2}\right)$, $V_{REF\ IN} = G.V_{REF\ IN}$.

To match the ladder resistance $R_1//R_2$ (R_{IN}) = 2.7KΩ.

The required nominal values of R_1 and R_2 are given by $R_1 = 2.7GK\Omega$, $R_2 = \frac{2.7G}{G-1}\ K\Omega$

Using these relationships a table of nominal values of R_1 and R_2 can be constructed for $V_{REF\ IN} = 2.5V$.

Input range	G	R_1	R_2
+5V	2	5.4KΩ	5.4KΩ
+10V	4	10.8KΩ	3.6KΩ

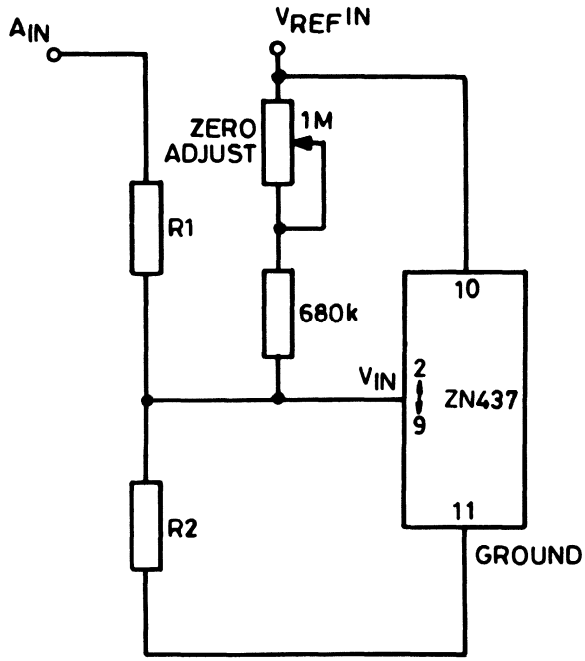


Fig. 13 General unipolar input connections

GAIN ADJUSTMENT

Due to tolerances in R_1 and R_2, tolerances in V_{REF} and the gain (full-scale) error of the DAC, some adjustment should be incorporated into R_1 to calibrate the full-scale of the converter. When used with 2% resistors a preset capable of adjusting R_1 by at least $\pm 5\%$ of its nominal value is suggested.

ZERO ADJUSTMENT

Zero adjustment needs providing to set the zero transition to the value of +0.5LSB. This is achieved by applying an adjustable positive offset to the comparator input via P2 and R_3.

Practical circuits values for +5V and +10V input ranges are given in Fig. 14 which incorporates both zero and gain adjustments.

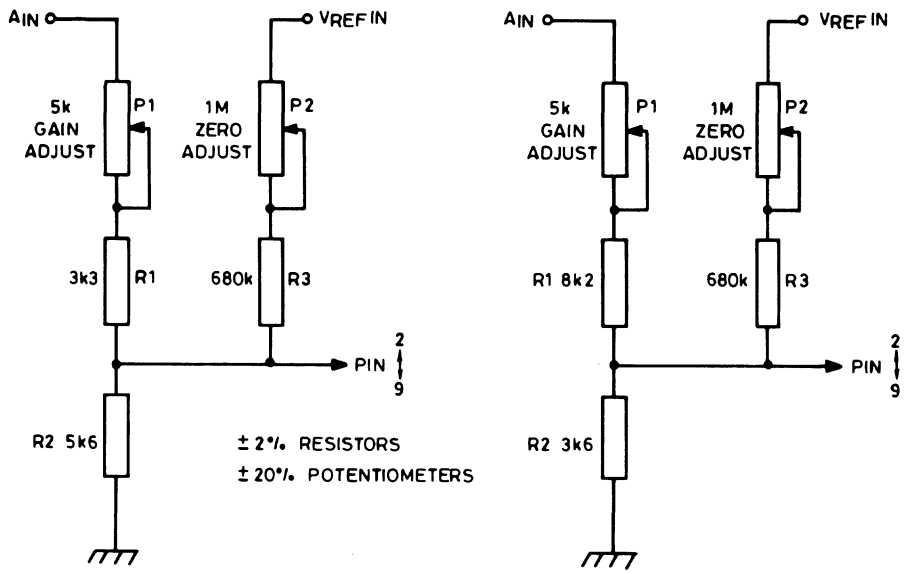


Fig. 14 Unipolar operation component values

UNIPOLAR ADJUSTMENT PROCEDURE

(i) Select the required channel for continuous conversion as described earlier and monitor the digital outputs ($\overline{RD}$ will need to be pulsed appropriately with the address inputs selecting the correct channel).

OFFSET SETTING

(ii) Apply 0.5LSB to A_{IN} and adjust zero until DB0 (LSB) just flickers between 0 and 1 with all other bits at 0.

i.e. transition 00000000 to 00000001.

GAIN SETTING

(iii) Apply full-scale minus 1.5LSB to A_{IN} and adjust gain until DB0 (LSB) just flickers between 0 and 1 with all other bits at 1.

i.e. transition 11111111 to 11111110.

UNIPOLAR SETTING-UP POINTS

Input range, +FS	0.5LSB	FS - 1.5LSB
+5V	9.8mV	4.9707V
+10V	19.5mV	9.9414V

$$1LSB = \frac{FS}{256}$$

UNIPOLAR LOGIC CODING

Analogue input (A_{IN}) (Nominal code centre value)	Output code (Binary)
FS - 1LSB	11111111
FS - 2LSB	11111110
0.75FS	11000000
0.5FS + 1LSB	10000001
0.5FS	10000000
0.5FS - 1LSB	01111111
0.25FS	01000000
1LSB	00000001
0	00000000

BIPOLAR OPERATION

For bipolar operation the input to the ZN437 is offset by half full-scale by connecting a resistor R_3 between $V_{REF\ IN}$ and V_{IN} (Fig. 15).

When $A_{IN} = -FS$, V_{IN} needs to be equal to zero.

When $A_{IN} = +FS$, V_{IN} needs to be equal to $V_{REF\ IN}$.

If the full-scale range is $\pm G$. $V_{REF\ IN}$ then $R_1 = (G - 1)$. R_2 and $R_1 = G$. R_3 fulfil the required conditions.

To match the ladder resistance, $R_1//R_2//R_3$ $(= R_{IN}) = 2.7K\Omega$.

Thus the nominal values of R_1, R_2, R_3 are given by $R_1 = 5.4G K\Omega$, $R_2 = 5.4G/(G - 1)K\Omega$, $R_3 = 5.4K\Omega$.

A bipolar range of $\pm V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $V_{REF\ IN}$) results if $R_1 = R_3 = 5.4K\Omega$ and $R_2 = \infty$.

Assuming $V_{REF\ IN} = 2.5V$, the nominal values of resistors for $\pm 5V$ and $\pm 10V$ input ranges are given in the following table.

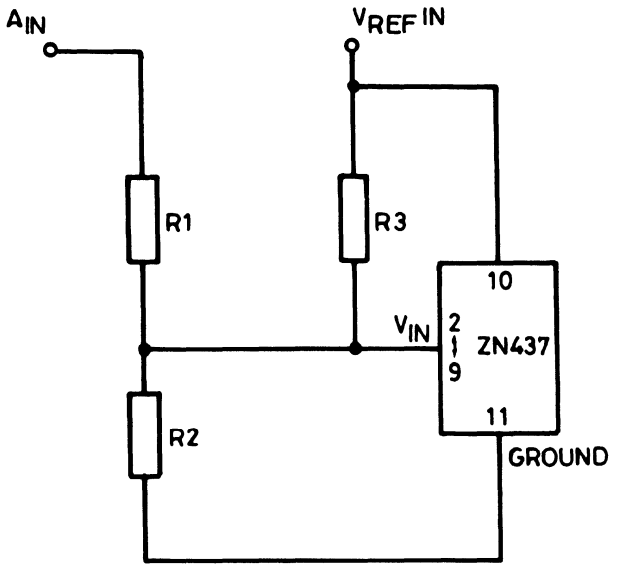


Fig. 15 Basic bipolar input connection

Input range	G	R_1	R_2	R_3
±5V	2	10.8KΩ	10.8KΩ	5.4KΩ
±10V	4	21.6KΩ	7.2KΩ	5.4KΩ

Minus full-scale (offset) is set by adjusting R_1 about its nominal value relative to R_3. Plus full-scale (gain) is set by adjusting R_2 relative to R_1. Practical circuit realisations are given in Fig. 16.

Note that R_3 will sink additional current from the reference to that required by V_{REFIN} and this should be taken into consideration when selecting the reference components.

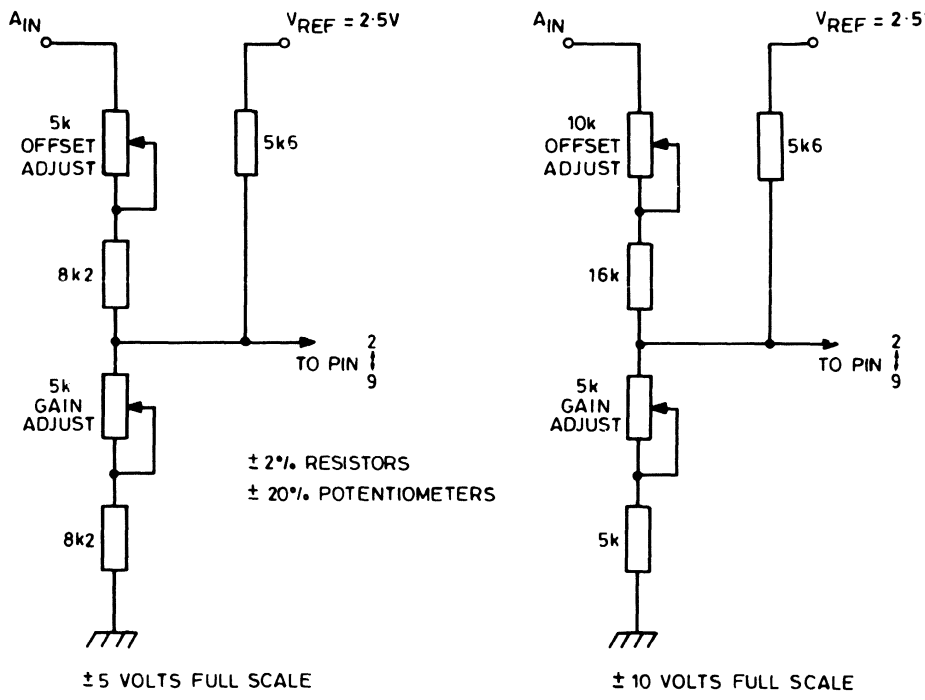


Fig. 16 Bipolar operation - component values

BIPOLAR ADJUSTMENT PROCEDURE

(i) Select the required channel for continuous conversion as described earlier and monitor the digital outputs ($\overline{RD}$ will need to be pulsed appropriately with the address inputs selecting the correct channel).

OFFSET SETTING

(ii) Apply −(FS - 0.5LSB) to A_{IN} and adjust offset until the DB0 (LSB) output just flickers between 0 and 1 with all other bits at 0.

i.e. transition 00000000 to 00000001.

GAIN SETTING

(iii) Apply +(FS - 1.5LSB) to A_{IN} and adjust gain until DB0 (LSB) just flickers between 0 and 1 with all other bits at 1.

i.e. transition 11111111 to 11111110.

BIPOLAR SETTING-UP POINTS

Input range, ±FS	−(FS −0.5LSB)	+(FS −1.5LSB)
±5V	−4.9805V	+4.9414V
±10V	−9.9609V	+9.8828V

$$1LSB = \frac{2FS}{256}$$

BIPOLAR LOGIC CODING

Analogue input (A_{IN}) (Nominal code centre value)	Digital output code MSB LSB
+(FS - 1LSB)	11111111
+(FS - 2LSB)	11111110
+0.5FS	11000000
+1LSB	10000001
0	10000000
−1LSB	01111111
−0.5FS	01000000
−(FS - 1LSB)	00000001
−FS	00000000

MICROPROCESSOR INTERFACING TO THE 8086

The typical circuitry required to interface the ZN437 to the 8086 microprocessor is shown in Fig. 17. The ZN437 has been located within the IO memory map using standard address decoding techniques. The decoded address is used to gate either the microprocessor $\overline{RD}$ or $\overline{WR}$ through to the ZN437 depending on which cycle is being executed.

The clock is derived from the PCLK output of the 8284 clock generator which is half the frequency of the microprocessor clock. The A-D converter of the ZN437 can run at a maximum clock frequency of 500KHz. The clock pre-divider bits in the control register should therefore be set to ÷8. This will give a converter clock frequency of 312KHz for the 5MHz 8086 and 500KHz for the 8MHz 8086-2. For the 10MHz 8086-1 the PCLK output of the 8284 clock generator should be further divided by 2 using a flip flop divider. This ensures that the converter clock rate is not exceeded and corresponds to a converter clock frequency of 312KHz.

The ZN437 is an 8-bit device and is shown connected to the lower 8 bits (AD0-AD7) of the 16-bit bus. Each ZN437 RAM location must therefore be located on an even address boundary. This is because the 8086 reads data from bits AD8-AD15 when reading from odd addresses. Similarly to write a Control Word to the ZN437 an IO write is performed to an even address in the 16 byte block enabled by the address decoding logic. Writing to any of the 8 even addresses will result in the word being written to the control register. This is because the state of the ZN437 address inputs is irrelevant during a ZN437 write cycle.

As an example assume the address decoding gives an active low output for an IO address of 100X hex, (where 'X' is any hex number). The addresses of the ZN437 RAM locations are shown below.

Therefore reading from IO address 1004 reads the converted data from analogue input 2.

It should be noted that as the ZN437 is an 8-bit device it is not necessary to decode the AD0 and BHE signals of the 8086.

HIGH SPEED INTERFACING

The high speed 8086-2 and 8086-1 have minimum access times of 130 and 125ns respectively. To interface these microprocessors to the ZN437 the wait state should be inserted in the ZN437 read cycle. This is shown by the dotted box in the circuit diagram of Fig. 17.

IO address	ZN437 RAM address	Corresponding input channel
1000	0	A_{IN} 0
1002	1	A_{IN} 1
1004	2	A_{IN} 2
1006	3	A_{IN} 3
1008	4	A_{IN} 4
100A	5	A_{IN} 5
100C	6	A_{IN} 6
100E	7	A_{IN} 7

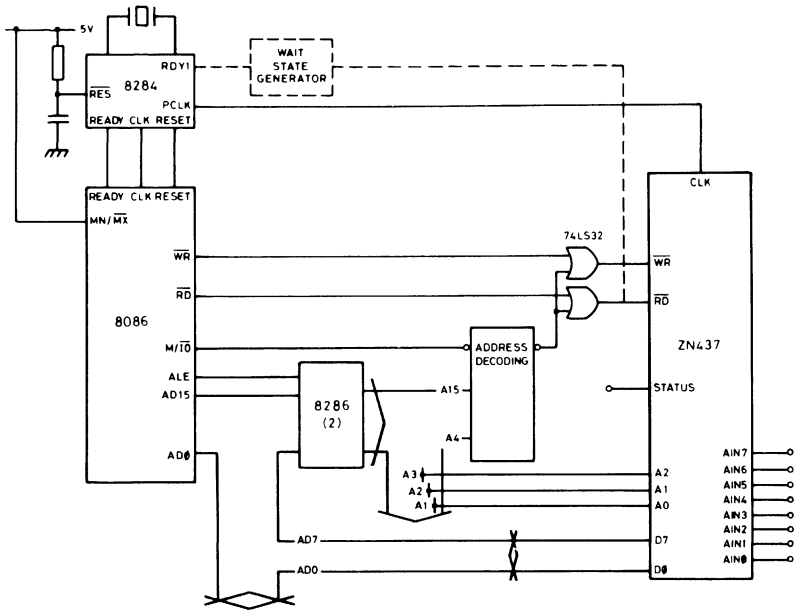


Fig. 17 ZN437 - 8086 interface

8088 INTERFACING

Fig. 18 shows the typical circuitry required to interface the ZN437 to the 8088. As can be seen from the diagram the circuitry is very similar to that required for the 8086. The main difference is the addressing of the ZN437 RAM. As the data bus is now only 8-bits wide every microprocessor read whether from odd or even addresses reads data from AD0-AD7. Therefore each ZN437 RAM location no longer has to lie on an even address boundary and so they can now occupy consecutive addresses.

To illustrate this consider the example used with the 8086. Here the address decoding gives an active low output pulse for an IO address of 100X hex, (where 'X' is any hex number). However in this case as AD3 is also decoded we will assume it has to be low. The addresses of the ZN437 RAM locations are shown below.

IO address	ZN437 RAM address	Corresponding input channel
1000	0	A_{IN} 0
1001	1	A_{IN} 1
1002	2	A_{IN} 2
1003	3	A_{IN} 3
1004	4	A_{IN} 4
1005	5	A_{IN} 5
1006	6	A_{IN} 6
1007	7	A_{IN} 7

As with the 8086 when using the higher speed version, the 8MHz 8088-2, the wait state should be inserted into the ZN437 read cycle.

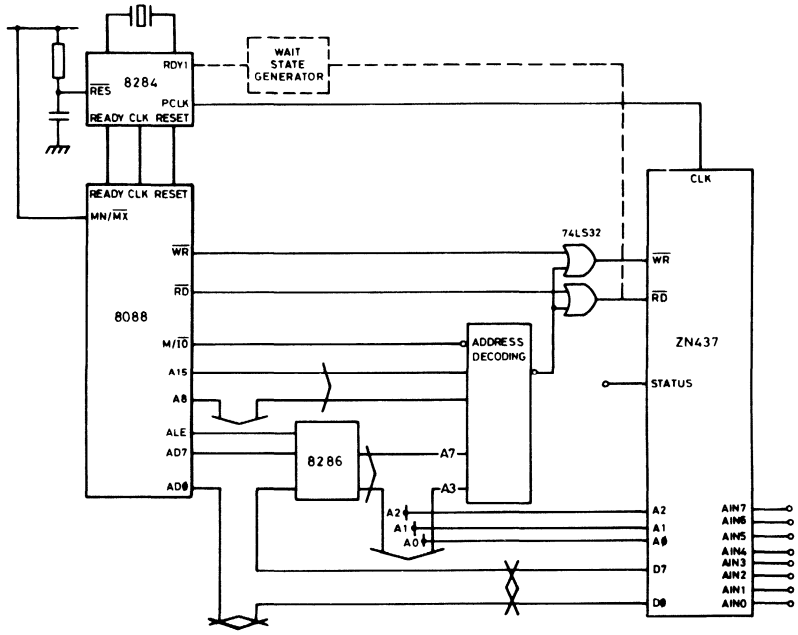


Fig. 18

INTERFACING TO THE Z80 MICROPROCESSOR

The ZN437 can easily be interfaced to the Z80, Z80A or Z80B microprocessors, as shown in Fig. 19.

The data lines from the microprocessor are connected directly to DB0-DB7 on the ZN437 for bi-directional data transfer. Some of the lower 8 address lines are decoded along with the I/O RQ line to gate through the RD and WR signals to the ZN437 as required. The decoded WR signal is used by the ZN437 to latch in the Control Word. The decoded RD signal is used to enable data onto the data bus from the location in the 8×8 bit RAM selected by the ZN437 address inputs A_0, A_1 and A_2.

The microprocessor clock can be connected directly to the ZN437 clock input when using the Z80 or Z80A. The Z80B will require an external $\div 2$ circuit. The ZN437 clock input is then divided down, as governed by the Control Word and should be set to give an internal clock of 500KHz or less.

The STATUS output goes low when a conversion is complete. This can be used to generate an interrupt or to set a flag for polling.

Alternatively STATUS can be left open circuit and a software delay used to ensure the conversion is complete.

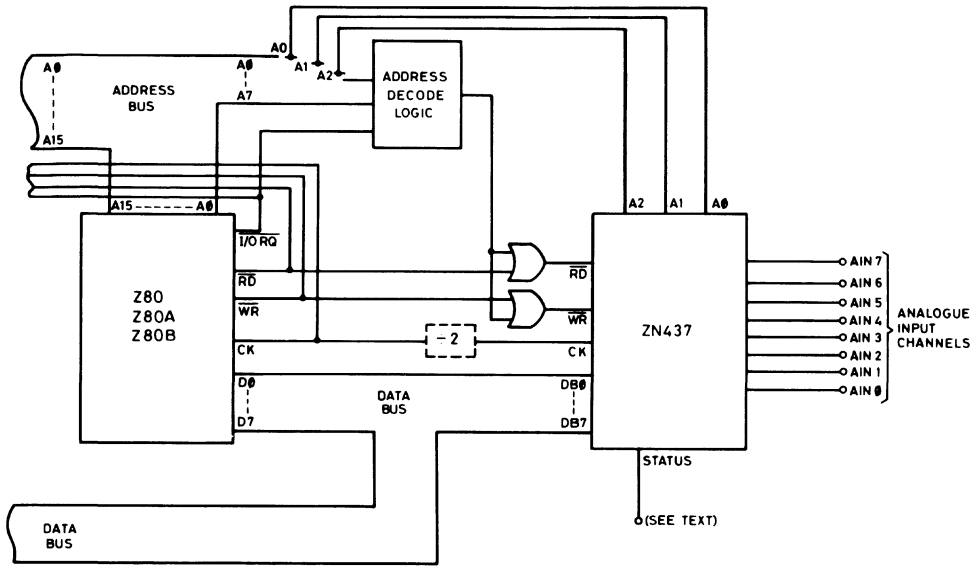


Fig. 19 Interfacing the ZN437 to the Z80 (schematic)

PLESSEY
Semiconductors

ZN438E/J

8-BIT MICROPROCESSOR COMPATIBLE D-A CONVERTER

The ZN438 is a monolithic 8-bit D-A converter with input latches to facilitate updating from a data bus and a buffer amplifier to give a low analogue output impedance. The latch is transparent when $\overline{\text{ENABLE}}$ is low and the data is held when $\overline{\text{ENABLE}}$ is taken high.

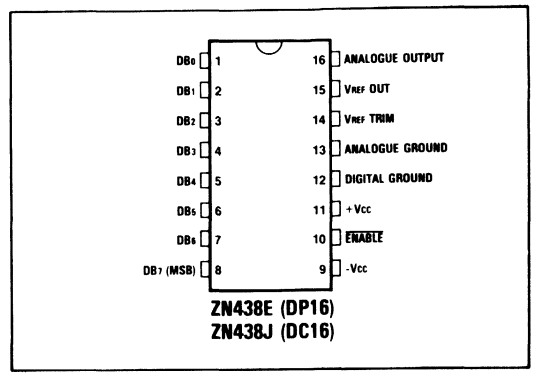
The ZN438 also contains a trimmable 2.5V reference which is internally connected to the R-2R ladder switches and to V_{REF} OUT.

FEATURES

- On-Chip High Speed Output Buffer Amplifier
- 1.25 microseconds Settling Time to ±0.5 LSB
- Trimmable Bandgap Reference
- Microprocessor, TTL and 5V CMOS Compatible
- Guaranteed Monotonicity over the Full Operating Temperature Range
- Commercial and Military Temperature Ranges

ORDERING INFORMATION

Device type	Operating temperature	Package
ZN438E	0°C to +70°C	DP16
ZN438J	-55°C to +125°C	DC16



Pin connections (top view)

ABSOLUTE MAXIMUM RATINGS

Supply voltage +Vcc	+7V
Supply voltage -Vcc	-9V
Logic input voltage	+Vcc
Operating temperature range	0°C to +70°C (ZN438E)
	-55°C to +125°C (ZN438J)
Storage temperature range	-55°C to +125°C
Analogue ground to digital ground	±200mV

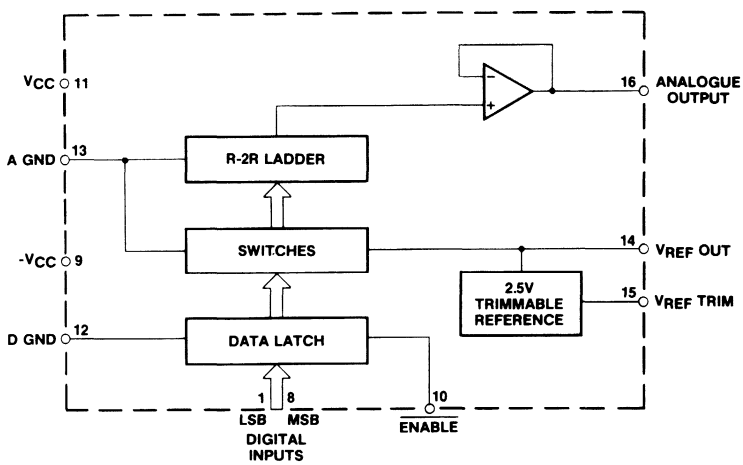


Fig.1 System diagram

ELECTRICAL CHARACTERISTICS (at $+V_{CC} = 5V$, $-V_{CC} = -5V$, $T_{amb} = 25°C$ with internal reference unless otherwise stated).

Parameter	$T_{amb} = +25°C$			Over specified temp. range		Units	Conditions
	Min.	Typ.	Max.	Min.	Max.		
D-A converter							
Resolution	8	–	–	8	–	Bits	
Accuracy	8	–	–	8	–	Bits	
Linearity error	–	–	±0.5	–	±0.5	LSB	
Differential linearity error	–	±0.5	–	–	±1	LSB	
Linearity error T.C.	–	±3	–	–	–	ppm/°C	
Differential linearity error T.C.	–	±6	–	–	–	ppm/°C	
Offset error	–	2	8	–	10	mV	
Offset error T.C.	–	±8	–	–	–	μV/°C	
Gain error	–	–	±0.5	–	–	LSB	With V_{REF} = 2.50V See note 1
Gain T.C.	–	60	–	–	150	ppm/°C	
Analogue output voltage	0	–	+2.7	0	+2.7	V	Note 2
Current	−3	–	+4	−3	+4	mA	$V_{out} = 0$ to V_{ref}
Analogue output impedance	–	6	10	–	–	Ω	
Settling time to 0.5LSB							$V_{REF} = 2.50V$ $C_{LOAD} = 470pF$ $R_L = 690Ω$
	–	1.25	–	–	–	μs	1LSB major transition
	–	2	–	–	–	μs	All bits ON to all bits OFF
	–	2	–	–	–	μs	All bits OFF to all bits ON

NOTE 1

For operation below −50°C the full-scale temperature coefficient may become significantly worse if V_{CC} is allowed to fall below 5V.

Note 2

In some cases the reference may be trimmed to give A_{out} greater than 2.7V. However, this should be avoided because the A_{out} may not be 8 bit accurate at voltages above this.

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	$T_{amb} = +25°C$			Over specified temp. range		Units	Conditions
	Min.	Typ.	Max.	Min.	Max.		
Internal voltage reference							
Output voltage	2.450	2.500	2.550	–	–	V	$R_L = 1.5K\Omega$ $C_L = 100nF$
Maximum trim range	–	±5	–	–	–	% of V_{ref}	$R_{TRIM} = 10K\Omega$
Output voltage T.C.	–	30	100	–	–	ppm/°C	
Reference current	1	–	5	1	5	mA	
Slope resistance	–	0.75	2	–	–	Ω	
Digital inputs							
High level input voltage	2	–	–	–	–	V	
Low level input voltage	–	–	0.8	–	–	V	
High level input current	–	–	60	–	–	μA	$V_{in} = 5.5V$ $V_{CC} = Max.$
High level input current	–	–	20	–	–	μA	$V_{in} = 2.4V$ $V_{CC} = Max.$
Low level input current	–	–	−5μA	–	–	μA	$V_{in} = 0.4V$ $V_{CC} = Max.$
Input clamp diode voltage	–	−1.5	–	–	–	V	$I_{in} = -8mA$
Enable pulse width t_W	100	–	–	–	–	ns	Refer to Fig. 7
Data set up time t_{DS}	150	–	–	–	–	ns	
Data hold time t_{DH}	10	–	–	–	–	ns	
Power supplies							
Supply voltage ($+V_{CC}$)	4.5	5	5.5	4.5	5.5	V	
Supply voltage ($-V_{CC}$)	−4.5	−5	−5.5	−4.5	−5.5	V	
Supply current ($+I_{CC}$)	–	35	–	–	–	mA	
Supply current ($-I_{CC}$)	–	12	–	–	–	mA	
Power consumption	–	235	–	–	–	mW	

D-A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 2. Each 2R element is connected to 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (< 1mV). A binary weighted voltage is produced at the output of the R-2R ladder.

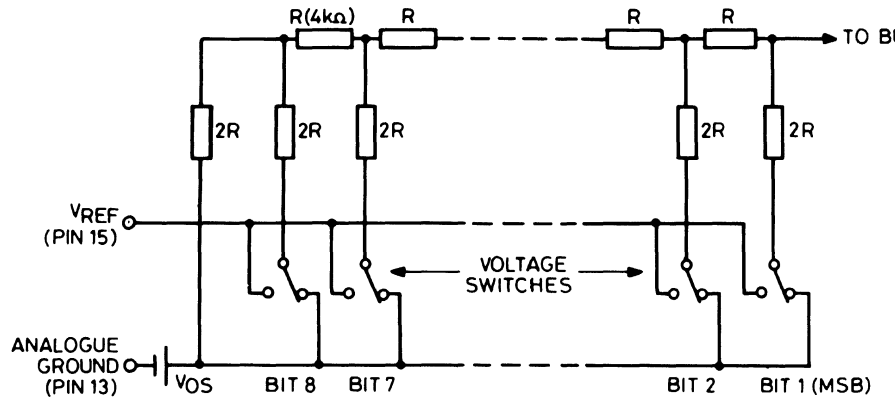


Fig. 2 The R-2R ladder network

$$\text{D-A output} = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input to the D-A from the data latch.

V_{OS} is a small offset voltage produced by the D-A switch currents flowing through the package lead resistance. The value of V_{OS} is typically 1mV. This offset will normally be removed by the setting up procedure.

REFERENCE

The internal reference is an active bandgap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig. 3). A resistor (R_{REF}) should be connected between $+V_{CC}$ (pin 11) and pin 15. The recommended value of 1K5 will supply a nominal reference current of (5-2.5)/1500 = 1.7mA. A stabilising/decoupling capacitor $C_{REF} = 0.1\mu F$ is required between pins 15 and 13.

The reference voltage can be trimmed by ± 5% with a 10K potentiometer (as shown in Fig. 4).

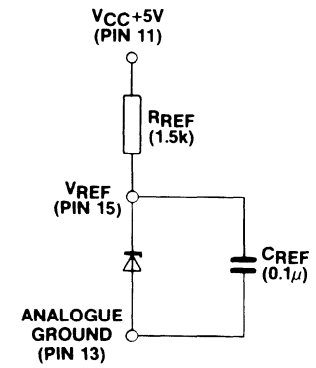


Fig. 3 Internal voltage reference

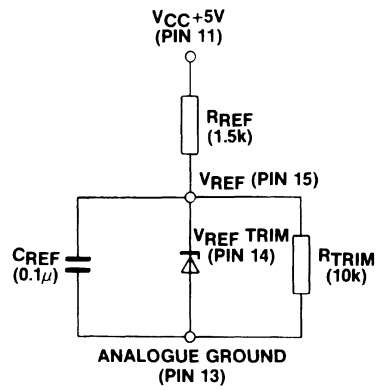


Fig. 4 Trimming circuit for the voltage reference

OPERATIONAL AMPLIFIER SECTION

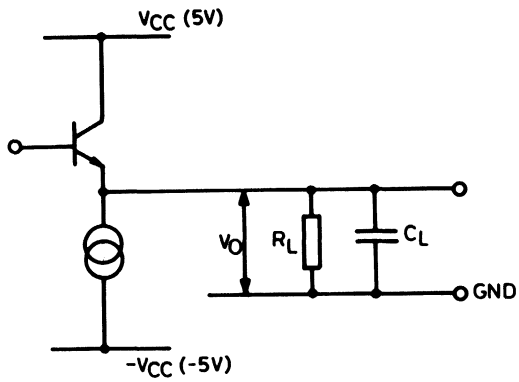


Fig. 5 Output stage

The D-A converter output is buffered by a unity gain, non-inverting amplifier with negligible offset error. Typically this buffer amplifier will develop 2.50V across an external load, and can drive capacitive loads of up to 470pF without a degredation of speed. The amplifier output can source 4mA and sink 3mA. The output stage of this amplifier consists of a bipolar transistor from the V_{CC} line and a current load to $-V_{CC}$ (the negative supply for the output amplifier). This output stage is shown in Fig. 5.

The power supply voltages can be increased, resulting in an improved performance in some parameters e.g. switching speed.

LOGIC

Input coding is binary for unipolar operation and offset binary for bipolar operation. When the enable input is low the data inputs drive the D-A directly. When enable goes high the input data word is held in the data latch.

The equivalent circuit for the data and clock inputs is shown in Fig. 6.

The ZN438 is provided with seperate analogue and digital ground connections. The circuit will operate correctly with as much as ±200mV between the two grounds.

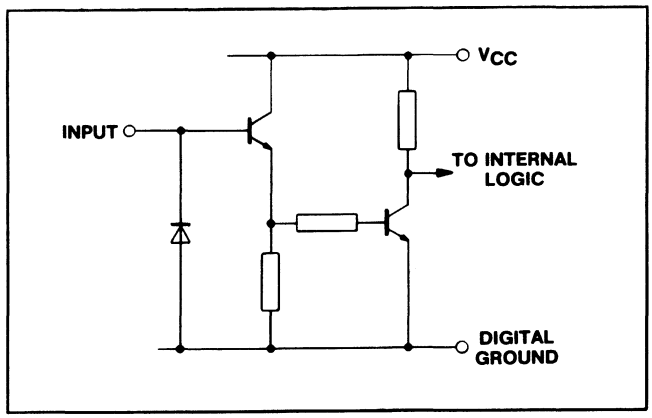


Fig. 6 Equivalent circuit of all inputs

TIMING AND CONTROL

The ZN438 has input data latches to simplify connection to a microprocessor data bus. The enable control line is used to control the condition of the latches. If enable is low the latches become transparent and the D-A converter responds to the digital inputs. If enable is taken high then the latches retain the data which was present on the digital inputs just prior to enable assuming a high state. While enable is high the analogue output remains at the value corresponding to the data held in the latches.

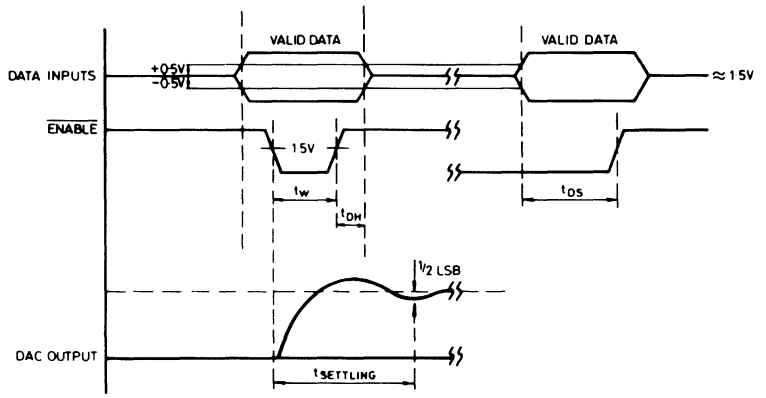
The function table is given in table 1 below.

Input data	$\overline{\text{Enable}}$	Latch output	Latch condition
0	0	0	Transparent
1	0	1	Transparent
0	⌐	0	Latching
1	⌐	1	Latching
X	1	Previous data	Latched

X = Don't care

⌐ = Low to high level transition

Table 1 ZN438 control logic function table



t_W = Enable pulse width
t_{DH} = Data hold time
t_{DS} = Data set-up time
$T_{SETTLING}$ = DAC output settling time to ±0.5LSB

Fig. 7 Timing diagram

GROUNDING

AC or transient voltages between analogue ground (pin 13) and digital ground (pin 12) can cause noise at the analogue output (pin 16). Digital systems are a source of noise which can be removed by connecting AGND and DGND together at the ZN438 or as close as possible to it. It is important that the voltage difference between AGND and DGND should not exceed 200mV.

(1) UNIPOLAR OPERATION

The nominal output range of the ZN438 is 0V to (V_{REF} – 1LSB) where V_{REF} is typically 2.50V. A circuit diagram showing the minimum external components required to give this output range is shown in Fig. 8. The reference trim input is used to provide the necessary gain adjustment by allowing variations of the internal reference voltage by ±5%.

For unipolar output ranges greater than 2.50V an external amplifier is required. A general schematic diagram is shown in Fig. 9.

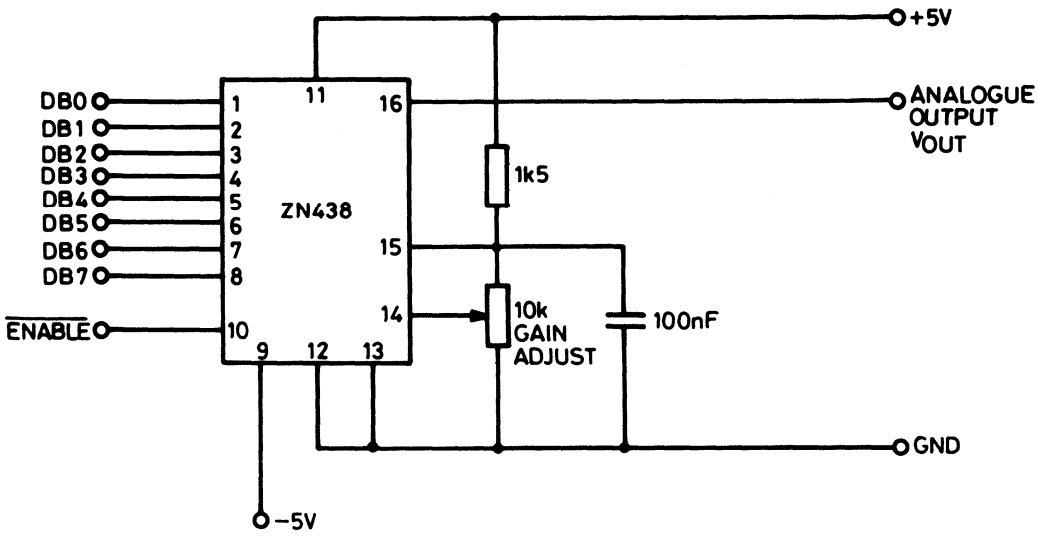


Fig. 8 Basic unipolar circuit diagram

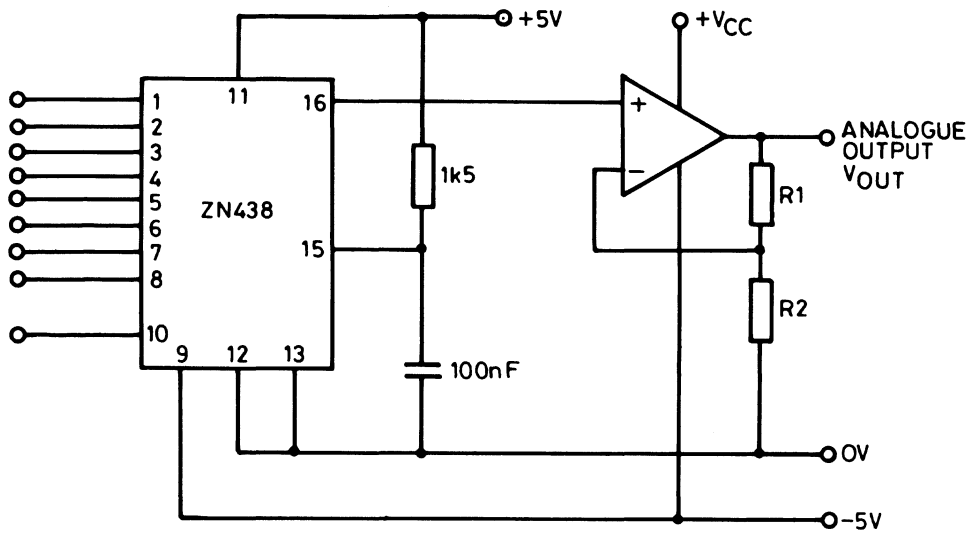


Fig. 9 Extended unipolar schematic diagram

The full-scale range of Fig. 9 is given by the equation:

$$V_{OUT\ FS} = \left(1 + \frac{R_1}{R_2}\right)(V_{REF} - 1LSB)$$
$$= G.(V_{REF} - 1LSB)$$

The circuit diagrams of Fig. 10 give typical component values for full-scale outputs of +5 and +10V. Zero offset adjustment is provided by use of the op-amp offset null capability. Gain adjustment is made by varying the value of R1.

The LF351 is a low cost JFET operational amplifier pin compatible with the industry standard 741. It features a high slew rate of 13 V/μs which gives a typical settling time for all bits on to all bits off (or vice versa) of 2μs for a 10V full-scale output. If a fast settling time is not required a 741 could be used as a direct replacement for the LF351. This would result in a typical settling time of 20μs for the conditions quoted above.

It can be seen from the gain equation that it is the relative and not the absolute value of the feedback resistors that is important. The values given here have been chosen to give minimum ringing on the output of the LF351 op-amp. As with all fast slew rate op-amps this can be a problem due to the minimal internal compensation used to achieve the fast slew rate. With lower slew rate amplifiers this will not be as much of a problem and hence the value of the feedback components could be increased if desired.

It should be noted that the V_{REF} trim potentiometer is no longer required as the gain adjustment is now provided by varying the op-amp feedback resistor R1.

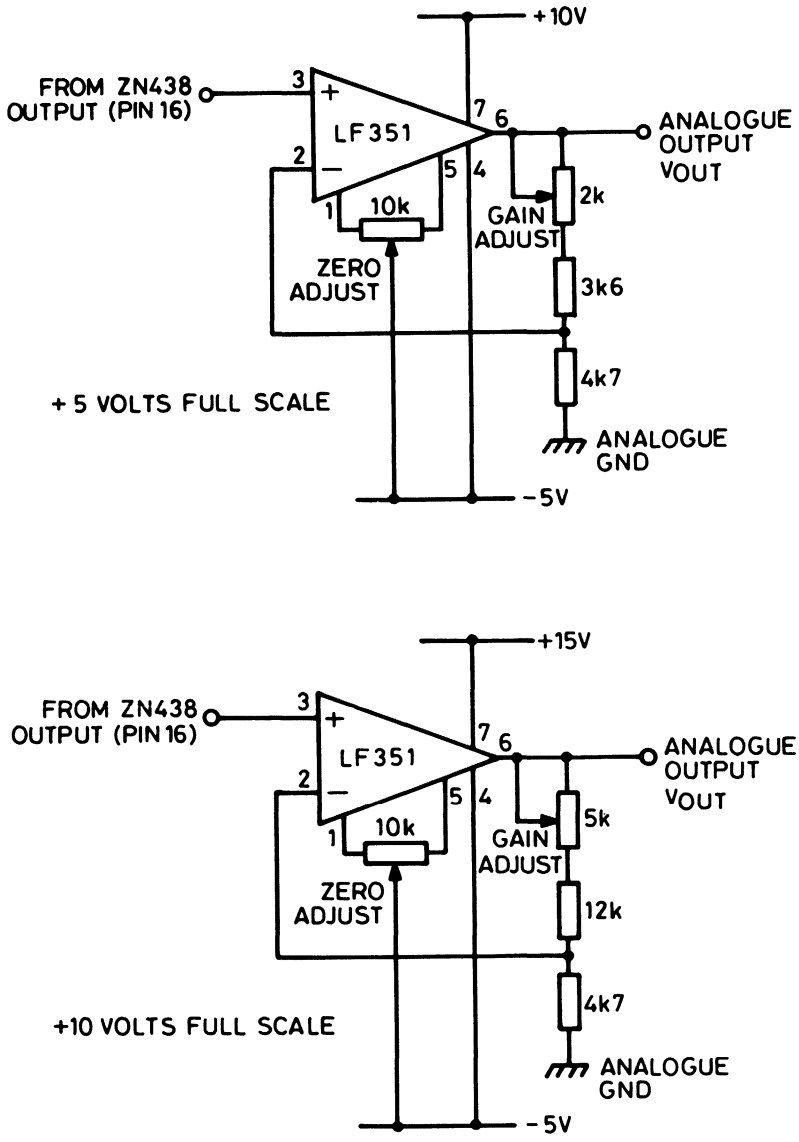


Fig. 10 Extended unipolar component values

Unipolar adjustment procedure

(i) Set all bits to OFF (low) with $\overline{\text{enable}}$ low and adjust zero until $V_{OUT} = 0.0000V$. (Not applicable to Fig. 8 as no offset adjustment is available)

(ii) Set all bits ON (high) and adjust gain until $V_{OUT} = FS - 1LSB$.

Unipolar setting up points

Output range, +FS	LSB	FS - 1LSB
+2.50V	9.8mV	2.4902V
+5V	19.5mV	4.9805V
+10V	39.1mV	9.9609V

$$1LSB = \frac{FS}{256}$$

Unipolar logic coding

Input code (Binary)	Analogue output (Nominal value)
11111111	FS - 1LSB
11111110	FS - 2LSB
11000000	0.75FS
10000001	0.5FS + 1LSB
10000000	0.5FS
01111111	0.5FS - 1LSB
01000000	0.25FS
00000001	1LSB
00000000	0

(2) BIPOLAR OPERATION

For bipolar operation the output from the ZN438 is offset by half full-scale by connecting a resistor between $V_{REF\ OUT}$ and the inverting input of the external amplifier. A general schematic diagram is shown in Fig. 11.

When the digital input to the ZN438 is zero its analogue output will be zero resulting in an output of −full-scale from the external amplifier. An input of all ones will give a ZN438 output of $+(V_{REF} - 1LSB)$ and a resulting amplifier output of +(full-scale − 1LSB).

Practical circuit diagrams are given in Fig. 12 with typical component values for full-scale ranges of ±5 and ±10V. Note, the V_{REF} dropper resistor has been reduced from 1K5 to 1K1 to supply the amplifier feedback resistor current. Minus full-scale (offset) is set by adjusting R1 about its nominal value relative to R3. Plus full-scale (gain) is set by adjusting R2 relative to R1.

A bipolar output range of $\pm V_{REF}$ (which corresponds to the basic unipolar range 0 to V_{REF}) is obtained if $R_1 = R_3 = 3K9$ and $R_2 = \infty$.

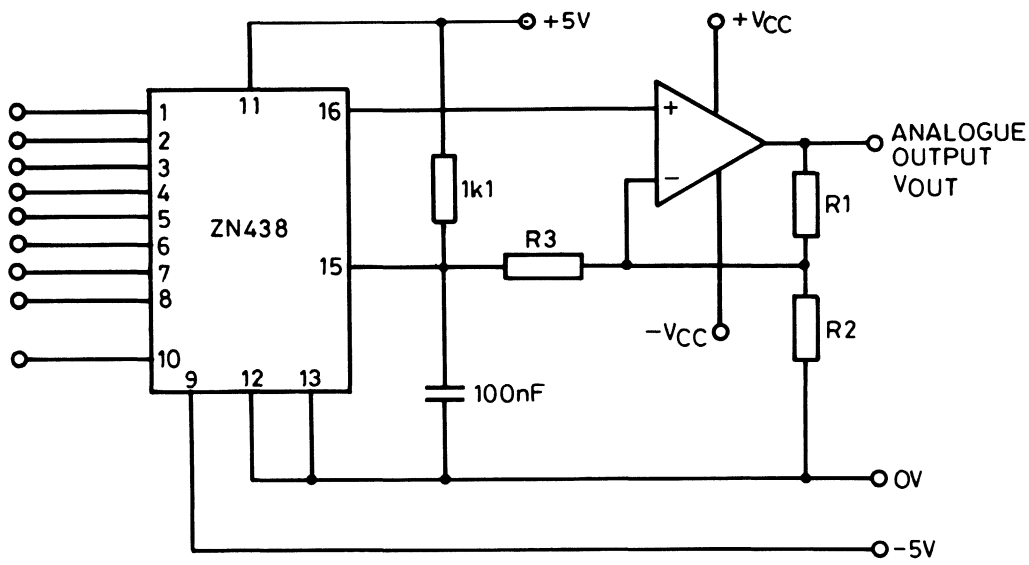


Fig. 11 Bipolar schematic diagram

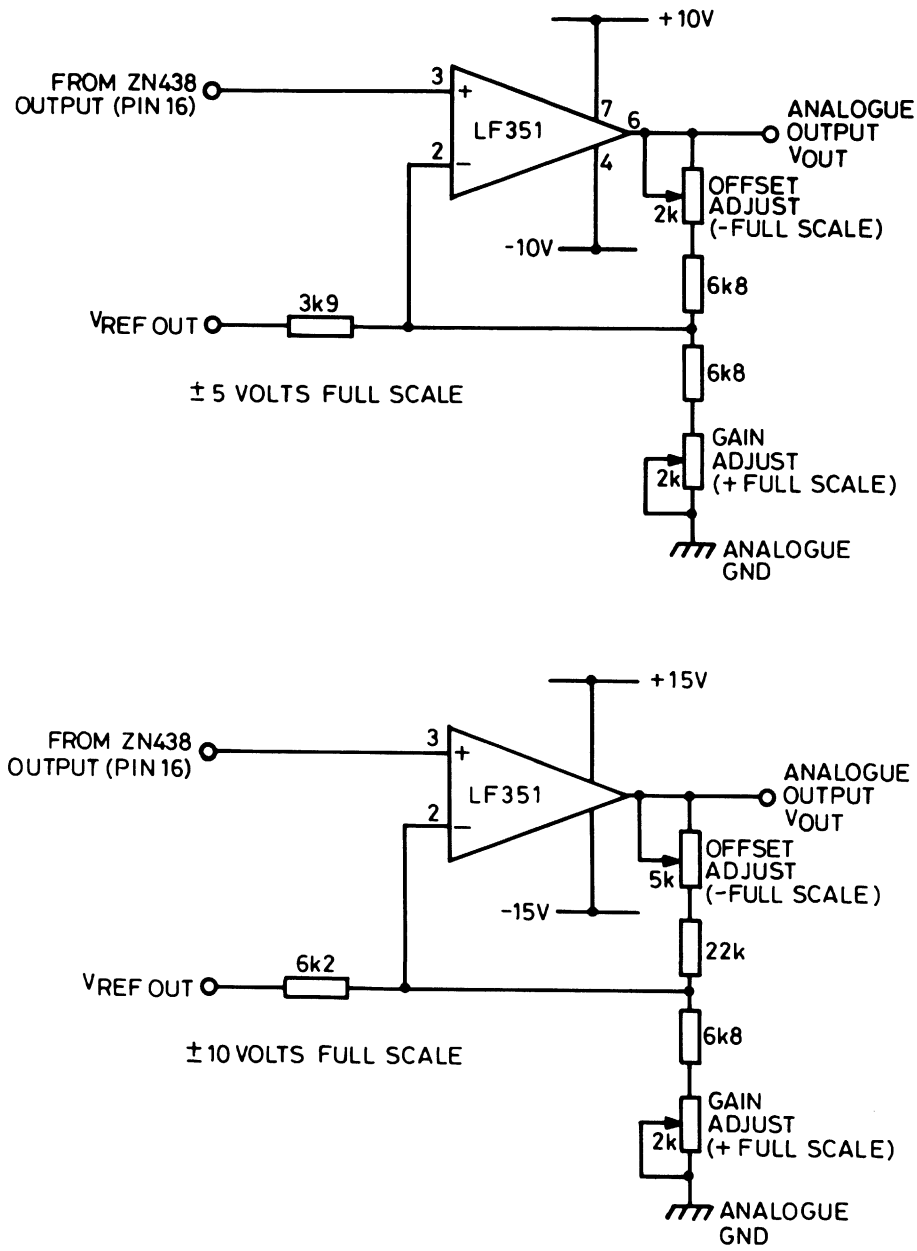


Fig. 12 Bipolar component values

Bipolar adjustment procedure

(i) Set all bits to OFF (low) with $\overline{\text{enable}}$ low and adjust offset until the amplifier output reads – full-scale.

(ii) Set all bits ON (high) and adjust gain until the amplifier output reads + (full-scale – 1LSB).

Bipolar setting up points

Output range, ±FS	LSB	–FS	+FS - 1LSB
±2.50V	19.5mV	–2.5000V	+2.4805V
±5V	39.1mV	–5.0000V	+4.9609V
±10V	78.1mV	–10.0000V	+9.9219V

$$1LSB = \frac{2FS}{256}$$

Bipolar logic coding

Input code (Offset binary)	Analogue output (Nominal value)
11111111	+(FS - 1LSB)
11111110	+(FS - 2LSB)
11000000	+0.5FS
10000001	+1LSB
10000000	0
01111111	–1LSB
01000000	–0.5FS
00000001	–(FS - 1LSB)
00000000	–FS

ZN439

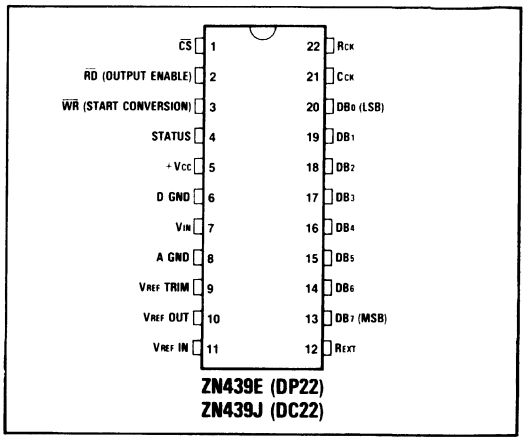
8-BIT MICROPROCESSOR COMPATIBLE A-D CONVERTER

The ZN439 is an 8-bit successive approximation A-D converter, designed to be easily interfaced to microprocessors. All active circuitry is contained on-chip including clock generator trimmable 2.5V bandgap reference, control logic and double buffered latches with three-state outputs.

These features give extra flexibility in use, with just three inputs to control all ADC operations and double buffered output latches which will allow data to be read at any time irrespective of the status of the converter.

FEATURES

- Choice of Linearity: ¼ LSB - ZN439-9, ½ LSB - ZN439-8, 1 LSB - ZN439-7
- 5 microseconds Conversion Time
- Microprocessor, TTL and CMOS Compatible
- On-Chip Clock
- Trimmable Bandgap Reference
- Versatile Microprocessor Interfacing with Double Buffered Output Latch
- Equally Suitable for Stand-Alone Applications
- ROM Type Operation
- Commercial or Military Temperature Ranges



Pin connections - top view

ORDERING INFORMATION

Device type	Linearity error (LSB)	Operating temperature	Package
ZN439E-9	¼	0°C to +70°C	DP22
ZN439J-9	¼	-55°C to +125°C	DC22
ZN439E-8	½	0°C to +70°C	DP22
ZN439J-8	½	-55°C to +125°C	DC22
ZN439E-7	1	0°C to +70°C	DP22
ZN439J-7	1	-55°C to +125°C	DC22

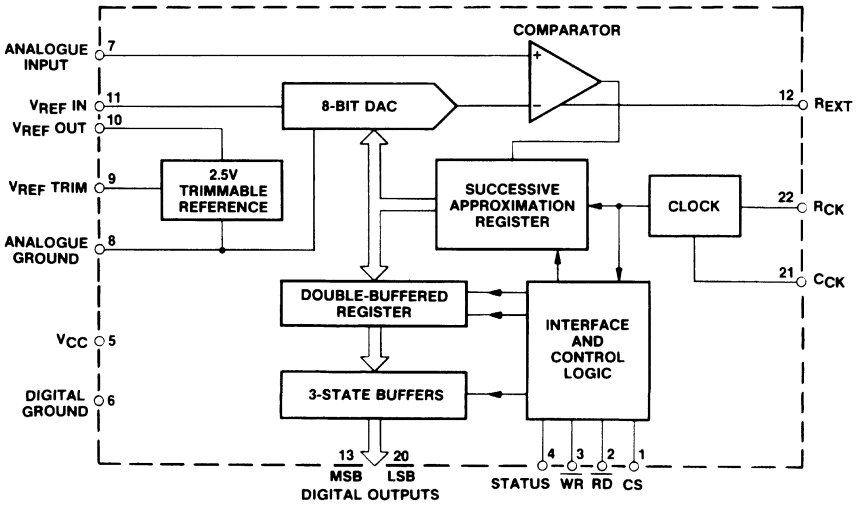


Fig.1 System diagram

ELECTRICAL CHARACTERISTICS (at $V_{CC} = 5V$, $T_{amb} = 25°C$ and $f_{CLK} = 1.6MHz$ unless otherwise specified).

Parameter	$T_{amb} = +25°C$			Over specified Temp. range		Units	Conditions
	Min.	Typ.	Max.	Min.	Max.		
ZN439-9							
Linearity error	–	–	±0.25	–	±0.25	LSB	
Differential linearity error	–	–	±0.5	–	±0.5	LSB	
ZN439-8							
Linearity error	–	–	±0.5	–	±0.5	LSB	
Differential linearity error	–	–	±0.75	–	±0.75	LSB	
ZN439-7							
Linearity error	–	–	±1	–	±1	LSB	
Differential linearity error	–	–	±1	–	±1	LSB	
ALL TYPES							
Zero transition	–	7	–	–	–	mV	ZN439E
(00000000→00000001)	–	7	–	–	–	mV	ZN439J
Full-scale transition	–	2.550	–	–	–	V	ZN439E
(11111110→11111111)	–	2.550	–	–	–	V	ZN439J
Linearity temperature coefficient		±3 typ.				ppm/°C	Ext. Ref.
Differential linearity temperature coefficient		±6 typ.				ppm/°C	
Gain temperature coefficient		±10 typ.				ppm/°C	
Offset temperature coefficient		±7 typ.				ppm/°C	
Resolution	8	–	–	–	–	Bits	
Conversion time	5	–	–	–	–	μs	
Supply rejection	–	0.2	–	–	–	%/V	
Supply voltage	4.5	5.0	5.5	4.5	5.5	V	
Supply current	–	30	45	–	–	mA	Outputs in high impedance state
Power consumption	–	150	225	–	–	mW	
Reference input range	1.5	–	3.0	–	–	V	
Ladder output impedance	–	2.7	–	–	–	kΩ	
COMPARATOR							
Input current	–	1.0	–	–	–	μA	$V_{in} = +3V$, $R_{ext} = 82K$
Input resistance	–	100	–	–	–	kΩ	
Tail current	25	–	150	25	150	μA	$R_{ext} = 82K$, $V- = -5V$
Negative supply	−3	−5	−30	−3	−30	V	
Input voltage	−0.5	–	+3.5	−0.5	+3.5	V	

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	$T_{amb} = +25°C$			Over specified Temp. range		Units	Conditions
	Min.	Typ.	Max.	Min.	Max.		
INTERNAL VOLTAGE REFERENCE							
Output voltage	–	2.588	–	–	–	V	PIN 9 NC $R_{REF} = 1.6K$ $C_{REF} = 0.47\mu F$
Output voltage tolerance	–	–	±3	–	–	%	
Slope impedance	–	0.75	–	–	–	Ω	
Reference current	0.25	–	5.2	0.25	5.2	mA	
Trim range	±5	–	–	±5	–	%	$R_{TRIM} = 10K$
Output voltage temperature coefficient	–	70	–	–	–	ppm/°C	At 5mA operating current (worst case) 25ppm at 2.0mA
CLOCK							
Maximum on-chip clock frequency	–	1.6	–	–	–	MHz	$R_{ck} = 1.5K\Omega$ $C_{ck} = 100pF$ (See Fig. 13)
Clock frequency tempco	–	−0.1	–	–	–	%/°C	
Clock capacitor	100	–	–	–	–	pF	
Clock resistor	1.0	–	-	–	–	kΩ	
Maximum external clock frequency	2	–	–	2	–	MHz	
Clock pulse width	250	–	–	–	–	ns	
High level I/P voltage V_{IH}	3.5	–	–	3.5	–	V	
Low level I/P voltage V_{IL}	–	–	0.8	–	0.8	V	
High level I/P current I_{IH}	–	1	–	–	–	μA	$V_{CC} = 5.5V$ $V_{IN} = 4V$
Low level I/P current I_{IL}	–	10	–	–	–	nA	$V_{CC} = 5.5V$ $V_{IN} = 0.8V$
Supply rejection	–	3.5	–	–	–	%/V	Int. clock Freq.
LOGIC $\overline{WR}$ + $\overline{CS}$ INPUTS							
High level I/P voltage V_{IH}	2	–	–	2	–	V	
Low level I/P voltage V_{IL}	–	–	0.8	–	0.8	V	
High level I/P current I_{IH}	–	40	–	–	–	μA	$V_{CC} = +5.5V$ $V_{IN} = +5.5V$
High level I/P current I_{IH}	–	20	–	–	–	μA	$V_{CC} = +5.5V$ $V_{IN} = +2.4V$
Low level I/P current I_{IL}	–	−50	–	–	–	μA	$V_{CC} = +5.5V$ $V_{IN} = +0.4V$
LOGIC $\overline{RD}$ INPUT							
High level I/P voltage V_{IH}	2	–	–	2	–	V	
Low level I/P voltage V_{IL}	–	–	0.8	–	0.8	V	
High level I/P current I_{IH}	–	220	–	–	–	μA	$V_{CC} = +5.5V$ $V_{IN} = +5.5V$

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	$T_{amb} = +25°C$			Over specified Temp. range		Units	Conditions
	Min.	Typ.	Max.	Min.	Max.		
High level I/P current I_{IH}	–	120	–	–	–	μA	$V_{CC} = +5.5V$ $V_{IN} = +2.4V$
Low level I/P current I_{IL}	–	−370	–	–	–	μA	$V_{CC} = +5.5V$ $V_{IN} = +0.4V$
DATA AND STATUS OUTPUTS							
High level output voltage V_{OH}	2.4	–	–	2.4	–	V	$I_{OH\ MAX}$
Low level output voltage V_{OL}	–	–	0.4	–	0.4	V	$I_{OL\ MAX}$
High level output current I_{OH}	–	–	−800	–	–	μA	
Low level output current I_{OL}	–	–	2	–	–	mA	
Three-state disable output	–	–	2.0	–	–	μA	$V_{OUT} = 0.4V$
leakage current (Data output only)	–	–	2.0	–	–	μA	$V_{OUT} = 2.4V$
Enable/disable							
Delay times T_{E1}	90	120	160	–	–	ns	
T_{E0}	60	100	120	–	–	ns	
T_{D1}	80	120	160	–	–	ns	
T_{D0}	60	80	110	–	–	ns	
Write pulse width	150	–	–	–	–	ns	
WR input to status O/P high	–	280	350	–	–	ns	
Read pulse width	160	–	–	–	–	ns	
Read input high to status output high	–	240	400	–	–	ns	

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	+7V
Maximum voltage, logice and V_{REF} inputs, A_{IN}	V_{CC}, −0.5V
Operating temperature range	0°C to +70°C (ZN439E) −55°C to +125°C (ZN439J)
Storage temperature range	−55°C to +125°C

GENERAL CIRCUIT OPERATION

The ZN439 utilises the successive approximation technique to produce an 8-bit parallel digital output. Upon receipt of a negative going pulse on the $\overline{WR}$ input the status output goes high, and the DAC input is set to the MSB. The resulting analogue output is compared with the unknown analogue input signal by means of the comparator. If the analogue input is larger, the MSB is left in circuit and if not the MSB is removed. On the second clock pulse this sequence is repeated for the next most significant bit and so on until all the 8 bits have been compared. On the 8th negative clock edge status goes low indicating that the conversion is complete.

The double-buffered register means the outputs can be enabled at any time, irrespective of the conversion status, and valid data will always be presented to the data bus. **Therefore the $\overline{RD}$ signal can be completely asynchronous with respect to the status.** Data can be read by taking $\overline{RD}$ low, thus enabling the three-state outputs. $\overline{RD}$ cannot be tied low as this will prevent the converter from updating it's outputs at the end of a conversion.

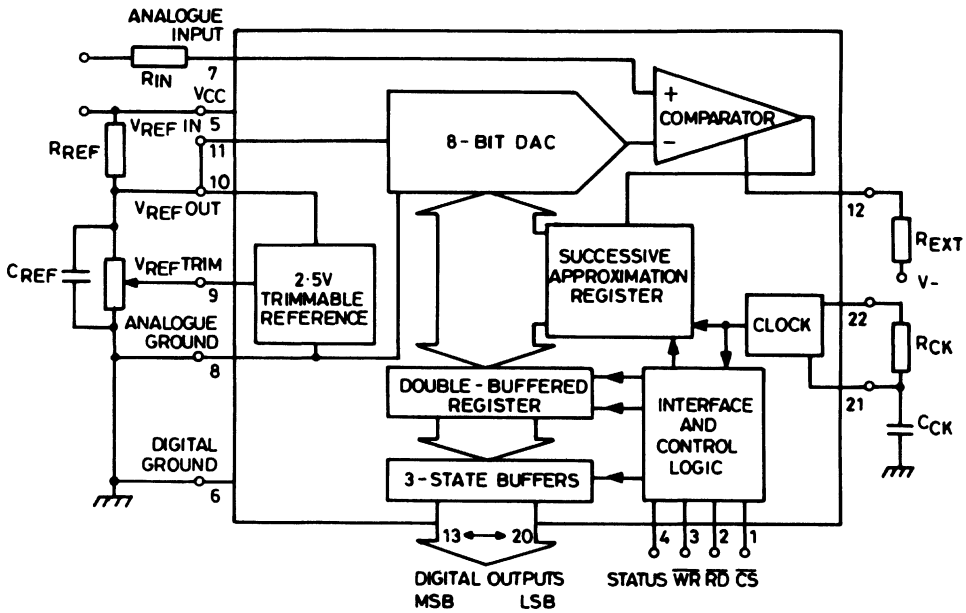


Fig. 2 Typical external components

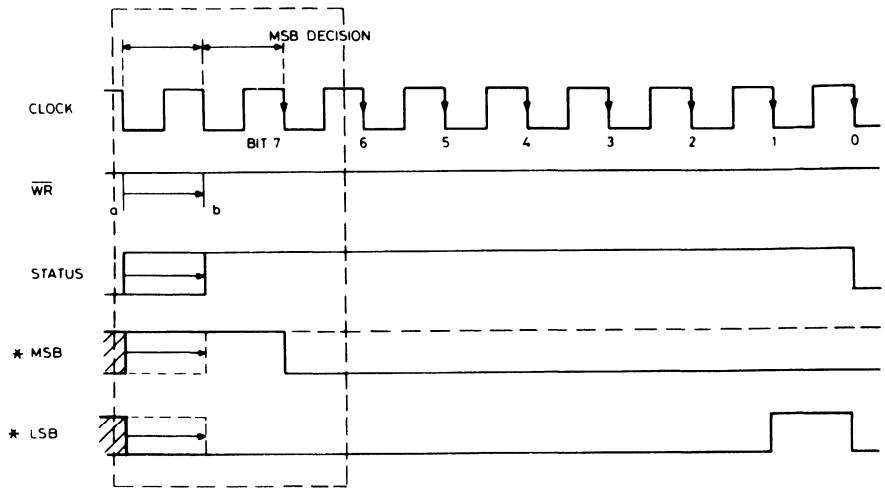
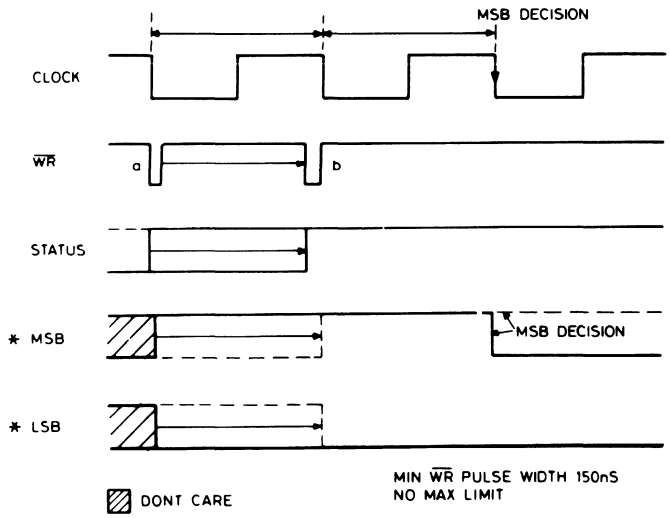


Fig. 3a



*Note: These signals are the internal MSB and LSB of the successive approximation register.

Fig. 3b (expanded inset)

Fig. 3 Timing diagram

CONVERSION TIMING

The ZN439 will accept a low going convert ($\overline{WR}$) pulse, which can be completely asynchronous with respect to the clock, and will produce valid data between 8 and up to 9 clock pulses later depending on the relative timing of the clock and convert signals. Timing diagrams for a conversion are shown in Fig. 3.

The ZN439 is first selected by taking $\overline{CS}$ (chip select) low. The converter is cleared by a low going convert ($\overline{WR}$) pulse, which sets the most significant bit and the status while resetting all other bits. Holding the $\overline{WR}$ input low will not inhibit the operation of the device.

The convert ($\overline{WR}$) pulse can be as short as 150ns; however the MSB must be allowed to settle for at least 625ns before the MSB decision is made. To ensure that this criterion is met even with short write pulses the converter waits for a falling clock edge before commencing with the conversion. This ensures that the MSB is allowed to settle for at least a full clock period or 625ns at maximum clock frequency. If the $\overline{WR}$ input is pulsed low at any time the conversion will restart. The input signals can be locked out during a conversion by removing the $\overline{CS}$ signal. This will isolate the converter from the external signals around it.

The status output goes low at the end of a conversion indicating that new data is now available. Internal logic monitors the $\overline{WR}$ input and if at the end of a conversion the $\overline{WR}$ input is high the clock signal will be locked out of the converter leaving it set up (i.e. the code 10000000 will appear on the input to the DAC) and waiting for its next convert ($\overline{WR}$) pulse. If the $\overline{WR}$ input is low the clock signal will not be inhibited allowing the converter to procede with another conversion. The double buffering on the three-state data outputs gives extra flexibility allowing the $\overline{RD}$ input to operate completely asynchronously with respect to the status and always produce valid data. Note that the $\overline{RD}$ input cannot be tied low as this will prevent the converter from updating at the end of a conversion.

CONTINUOUS CONVERSION

The ZN439 can be made to cycle by simply tying the $\overline{CS}$ and $\overline{WR}$ inputs low. It should be noted that after power up, valid data will only be available after the internal reference has stabilised. This time will depend upon the values of the reference decoupling capacitor and load resistor, but will be approximately 2mS for a 1K6 resistor and a 0.47μF capacitor.

A timing diagram for the continuous conversion mode is shown in Fig. 5 (overleaf).

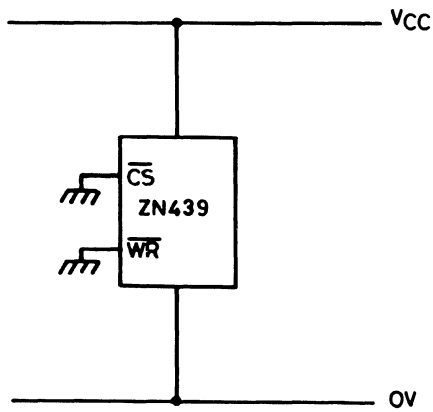


Fig. 4 Circuit for continuous conversion

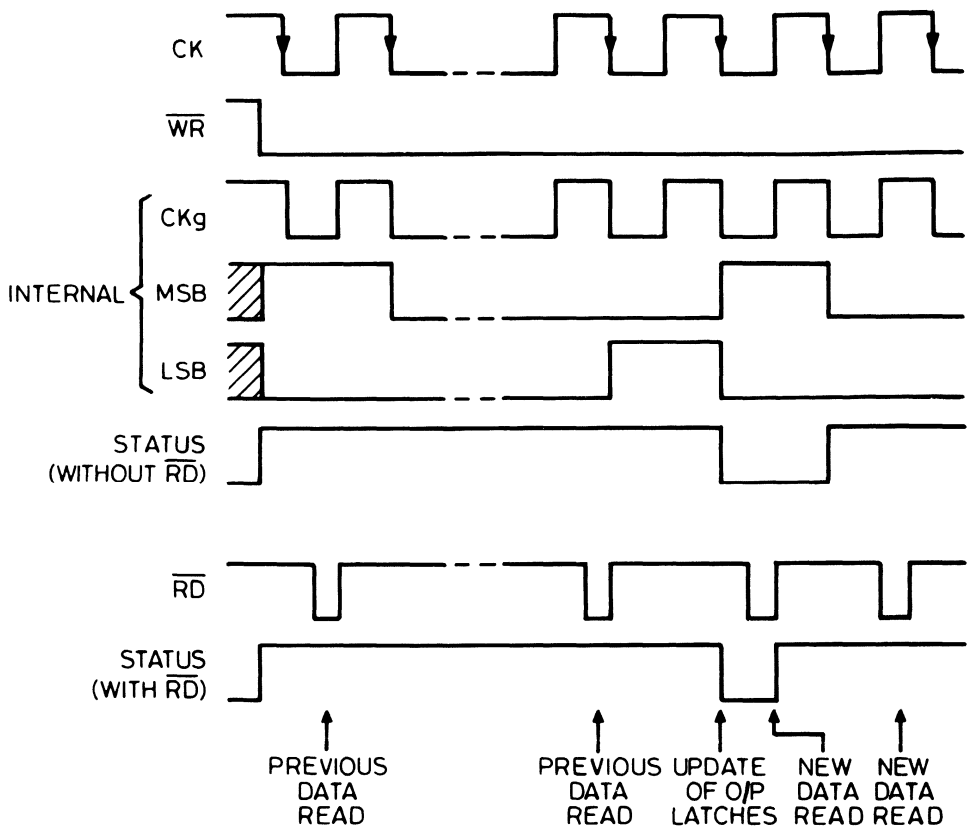


Fig. 5 Timing for continuous conversion

INTERRUPT DRIVEN

The ZN439 can also be used in an interrupt driven mode by using the status output. A WR pulse initiates a conversion sending the status high. The high to low transition of the STATUS output, indicating the end of a conversion, can be used as an interrupt signal by the microprocessor i.e. informing the microprocessor that a conversion has been completed. On receiving the interrupt the microprocessor sends out an RD pulse to take in the new data. On the rising edge of the RD pulse data is latched into the microprocessor and internal control logic forces the status output high hence removing the interrupt signal.

A timing diagram for the interrupt driven mode is shown in Fig. 6.

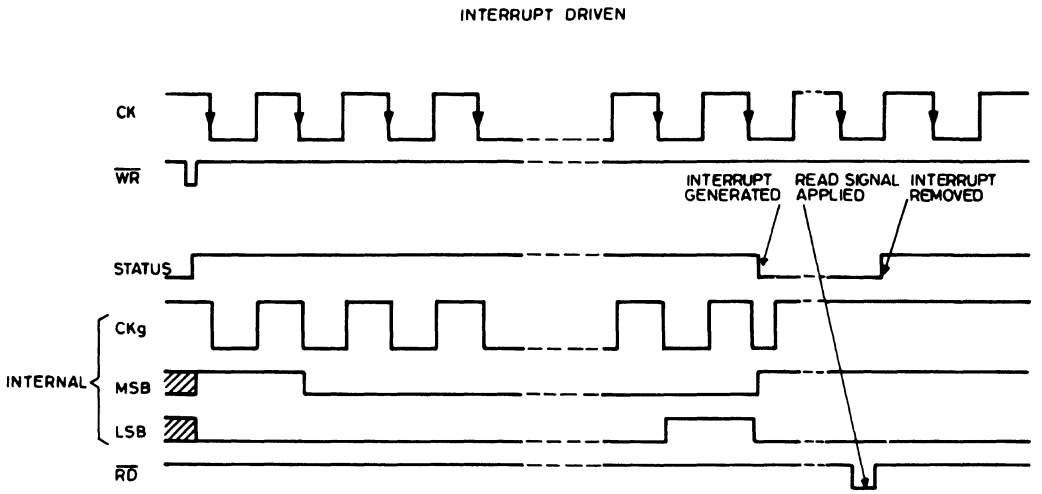


Fig. 6 Timing for interrupt driven mode

'STAND ALONE' OPERATION

The ZN439 is equally suitable for stand alone applications containing an on-chip clock and a 2.5V trimmable bandgap reference.

A typical circuit for unipolar operation is shown in Fig. 7a.

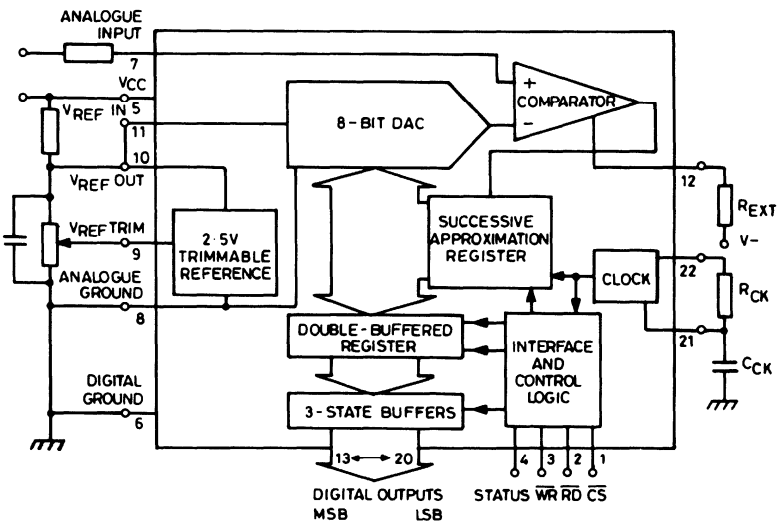


Fig. 7a Unipolar operation

By tying the $\overline{WR}$ and $\overline{CS}$ inputs low the device can be made to cycle. Also if the status output is connected via an inverter to the $\overline{RD}$ input the device can be updated at the end of each conversion and the output buffers enabled without the need for extra external control signals.

A timing diagram for stand alone operation is shown in Fig. 8.

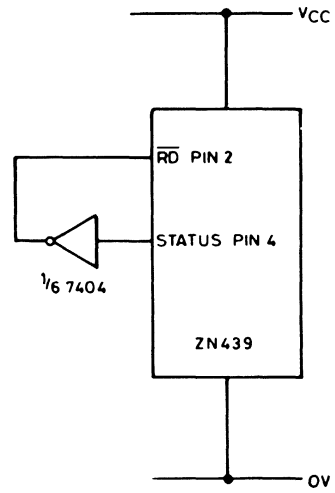
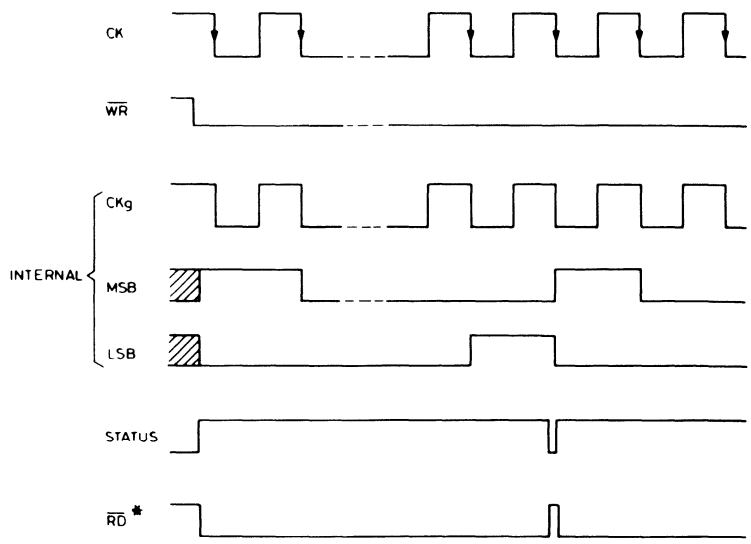


Fig. 7b Circuit for updating 'stand alone' converter



*Data valid while read is low subject to three-state delays

Fig. 8 Timing for 'stand alone' operation

DATA OUTPUTS

The data outputs are provided with three-state buffers to allow connection to a common data bus. An equivalent circuit is shown in Fig. 9. Whilst the $\overline{RD}$ input is high both output transistors are off and the device presents only a high impedance load to the bus. When $\overline{RD}$ is low the data outputs will assume the logic states present on the outputs of the double buffered register.

A test circuit and timing diagram for the output enable/disable delays are given in Fig. 10 (overleaf).

The status output utilises the same active pull-up as the data outputs for CMOS/TTL compatibility.

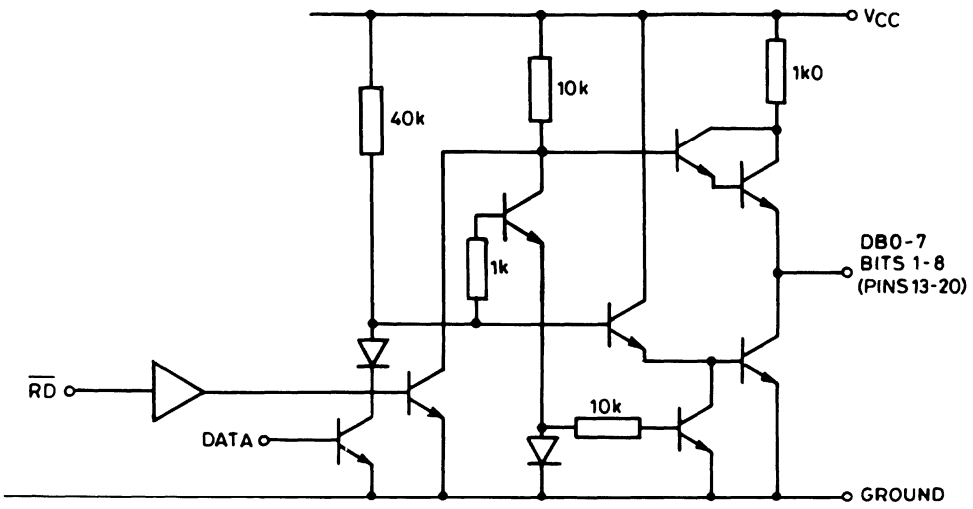
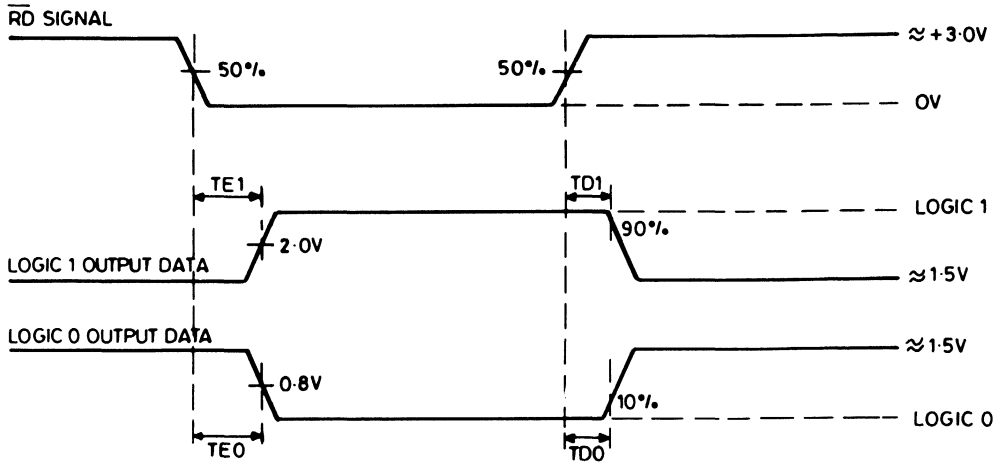


Fig. 9 Data outputs



TE = RD ENABLE DELAY TIME
TD = RD DISABLE DELAY TIME

Fig. 10a Output enable/disable delays

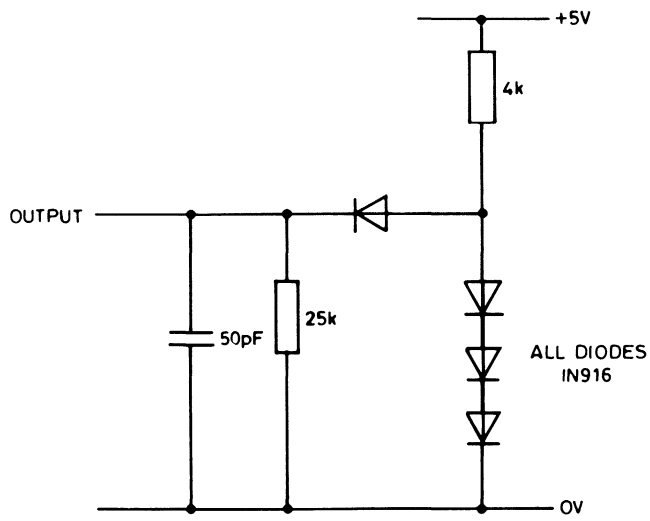


Fig. 10b Output load circuit

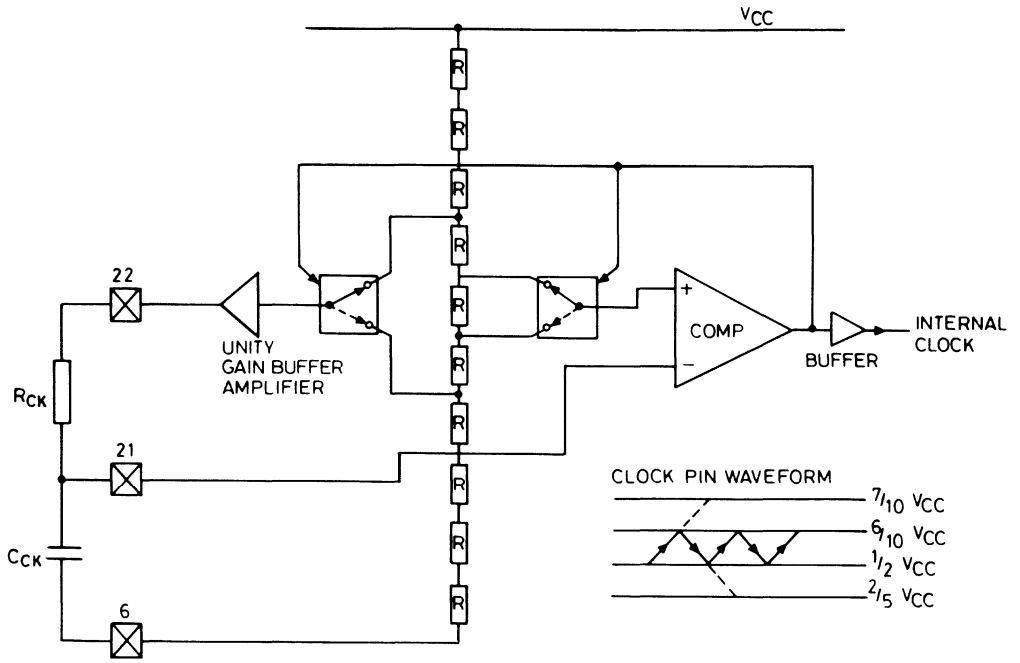


Fig. 11 Clock oscillator circuit

ON-CHIP CLOCK

The ZN439 on-chip clock oscillator operates with only two external components; a resistor connected between pin 21 and pin 22 and a capacitor between pin 21 and pin 6. The clock oscillator circuit and the external component connections are shown in Fig. 11.

The oscillator frequency may be varied with the aid of a potentiometer or variable capacitor as shown in Fig. 12a and Fig. 12b. Alternatively it is possible to overdrive the oscillator input with an external clock signal from a TTL or CMOS gate as shown in Fig. 12c.

A graph of oscillator frequency against capacitor and resistor values is given in Fig. 13.

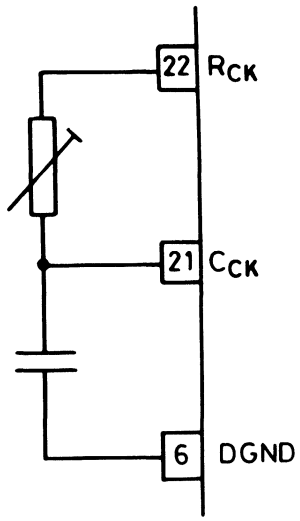


Fig. 12a Fixed capacitor
+ fixed/variable resistor

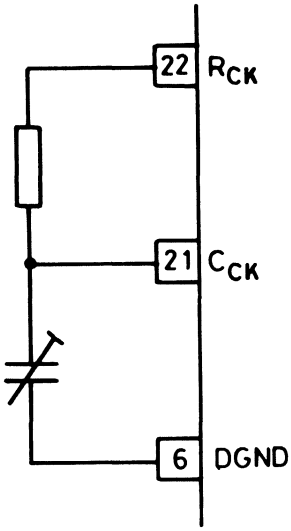


Fig. 12b Fixed resistor
+ fixed/variable capacitor

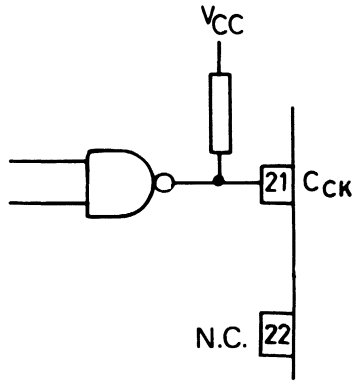


Fig. 12c External TTL or CMOS drive

Fig. 12 Clock circuit external components

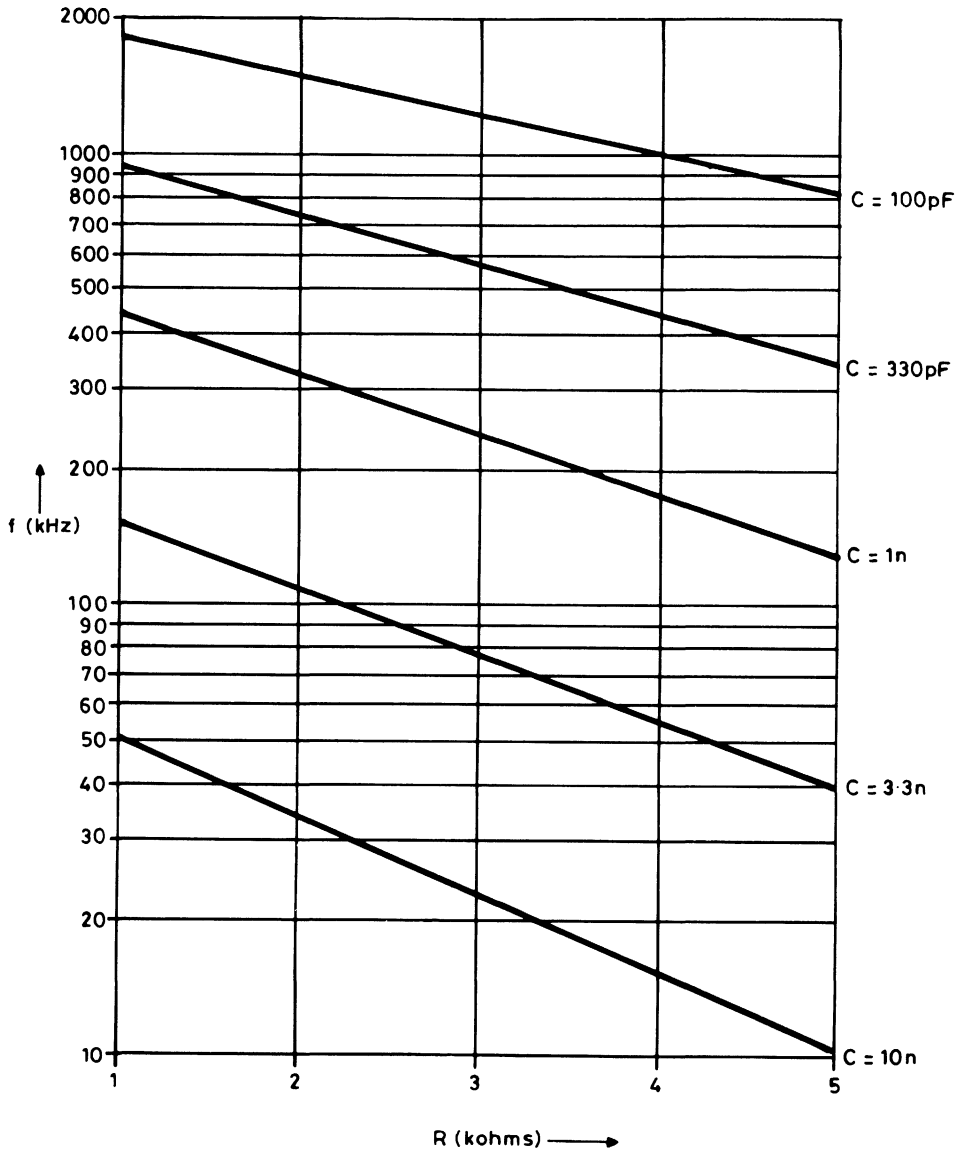


Fig. 13 Typical clock frequency v R. and C. values

ANALOGUE CIRCUITS

REFERENCE

(a) Internal reference

The internal reference is an active bandgap circuit which is equivalent to a 2.5 Zener diode with a very low slope impedance (Fig. 14). A resistor (R_{REF}) should be connected between V_{CC} and $V_{REF\ OUT}$, and a decoupling capacitor, C_{REF} (0.47μF), is required between $V_{REF\ OUT}$ and AGND. For internal reference operation $V_{REF\ OUT}$ is connected to $V_{REF\ IN}$.

A suitable current to drive one ZN439 is nominally 1.5mA and will be supplied by an R_{REF} of 1K6 [(5 – 2.56)/1K6 = 1.5mA].

If the reference is required to drive more than one ZN439 then the reference current can be increased e.g. an $R_{REF} = 470\Omega$ will supply a nominal reference current of (5 – 2.56)/0.47 = 5.2mA and this may be used to drive up to four ZN439's from just one internal reference. This useful feature saves power and gives excellent gain tracking between the converters.

Alternatively with $R_{REF} = 680\Omega$, the internal reference can be used as the reference voltage for other external circuits and can source or sink up to 1.5mA.

(b) External reference

If required an external reference in the range +1.5 to +3.0V may be connected to $V_{REF\ IN}$. The slope resistance of such a reference source should be less than $\frac{2.5\Omega}{n}$, where n is the number of converters supplied.

RATIOMETRIC OPERATION

If the output from a transducer varies with its supply then an external reference for the ZN439 should be derived from the same supply. The external reference can vary from +1.5 to +3.0V. The ZN439 will operate if $V_{REF\ IN}$ is less than +1.5V but reduced overdrive to the comparator will increase its delay and so the conversion time will need to be increased.

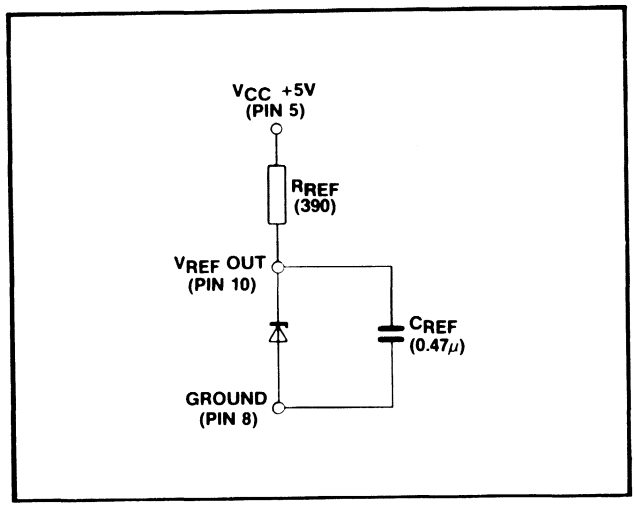


Fig. 14 Internal voltage reference

COMPARATOR

The ZN439 contains a fast comparator, the equivalent input circuit of which is shown in Fig. 15. A negative supply voltage is required to supply the tail current of the comparator. However as this is only 25 to 150μA and need not be well stablised it can be supplied by a simple diode pump circuit driven from the R_{CK} pin (pin 22).

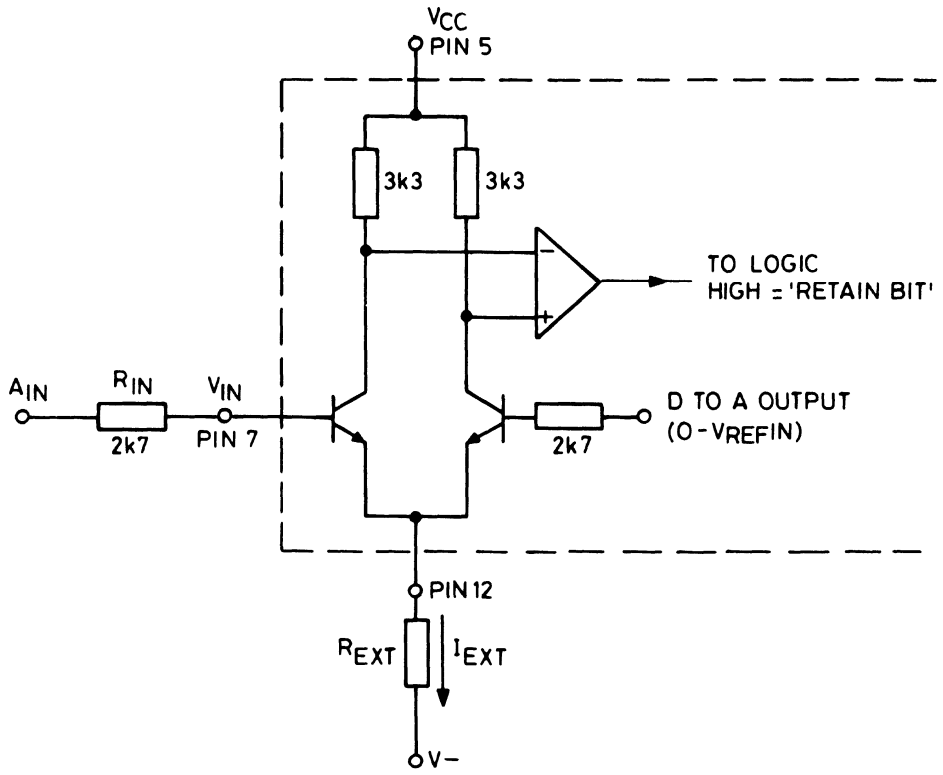


Fig. 15 Comparator equivalent circuit

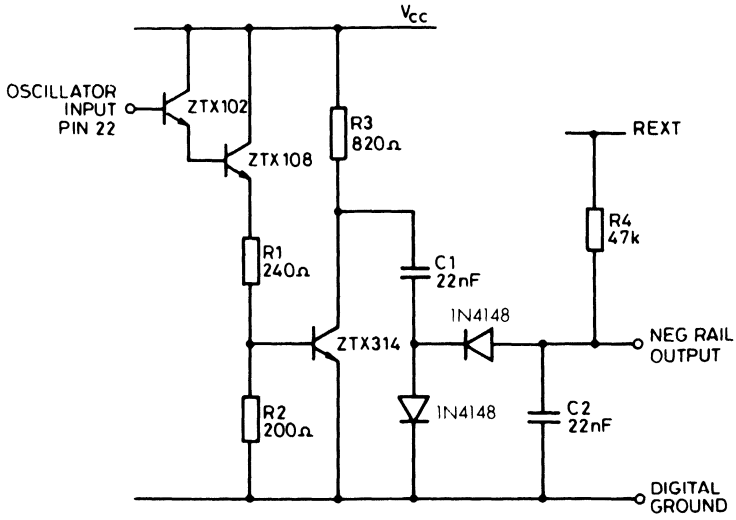


Fig. 16 Diode pump circuit

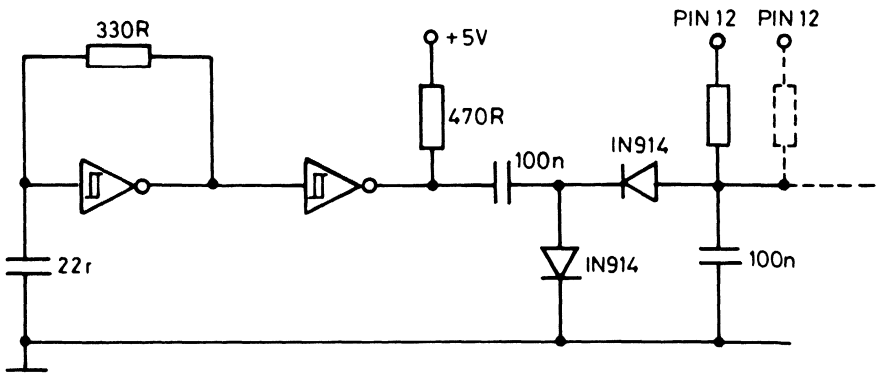


Fig. 17 Diode pump circuit to supply comparator tail current for up to five ZN439's

A suitable circuit is shown in Fig. 16. This circuit can be used in any converter operation mode. The diode pump circuit shown in Fig. 16 is driven by the on-chip clock (pin 22) and applies a voltage of about −3V to R4, thus providing the tail current for the comparator.

Where several ZN439's are used in a system the self-oscillating diode pump circuit of Fig. 17 is recommended. Alternatively, if a negative supply is available in the system then this may be utilised. A list of suitable resistors for different supply voltages is given in Table 1.

Table 1

V_- (volts)	R_{EXT} (kΩ)
3	47
5	82
10	150
12	180
15	220
20	330
25	390
30	470

D-A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 18. Each element is connected to either 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (1mV).

A binary weighted voltage is produced at the output of the R-2R ladder:

$$\text{D-A output} = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input to the D-A from the successive approximation register.

V_{OS} is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. This offset will normally by removed by the setting up procedure and since the offset temperature coefficient is low (7ppm/°C) the effect on accuracy will be negligible.

The D-A output range can be considered to be $0 - V_{REF\ IN}$ through an output resistance R(2k7).

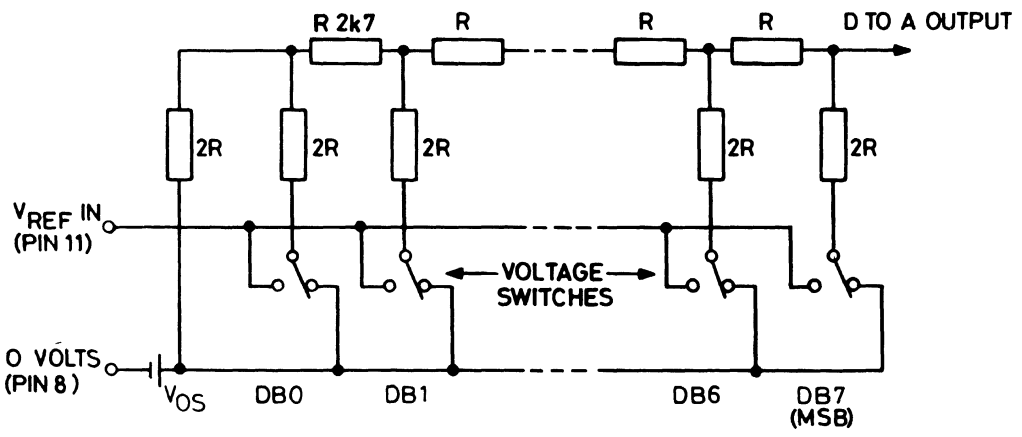


Fig. 18 R-2R ladder network

ANALOGUE INPUT RANGES

The basic connection of the ZN439 shown in Fig. 19 has an analogue input range 0 to $V_{REF\,IN}$ which, in some applications, may be made available from previous signal conditioning/ scaling circuits. Input voltage ranges greater than this are accommodated by providing an attenuator on the comparator input, whilst for smaller input ranges the signal must be amplified to a suitable level.

Bipolar input ranges are accommodated by off-setting the analogue input ranges so that the comparator always sees a positive input voltage.

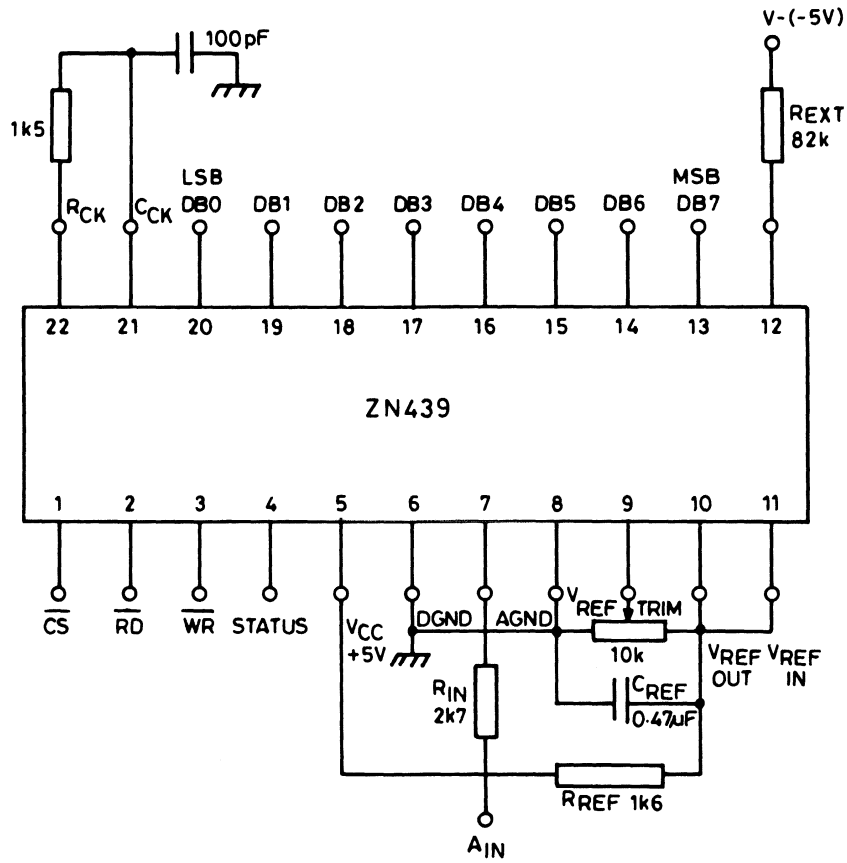


Fig. 19 External components for basic operation

UNIPOLAR OPERATION

The general connection for unipolar operation is shown in Fig. 20.

The values of R_1 and R_2 are chosen so that $V_{IN} = V_{REF\ IN}$ when the analogue input (A_{IN}) is at full-scale.

The resulting full-scale range is given by: $A_{IN}FS = \left|1 + \frac{R_1}{R_2}\right|$, $V_{REF\ IN} = G.V_{REF\ IN}$.

To match the ladder resistance R_1/R_2 (R_{IN}) = 2.7k.

The required nominal values of R_1 and R_2 are given by $R_1 = 2.7Gk$, $R_2 = \frac{2.7G}{G-1}$ k

Using these relationships a table of nominal values of R_1 and R_2 can be constructed for $V_{REF\ IN} = 2.5V$.

Input range	G	R_1	R_2
+5V	2	5.4k	5.4k
+10V	4	10.8k	3.6k

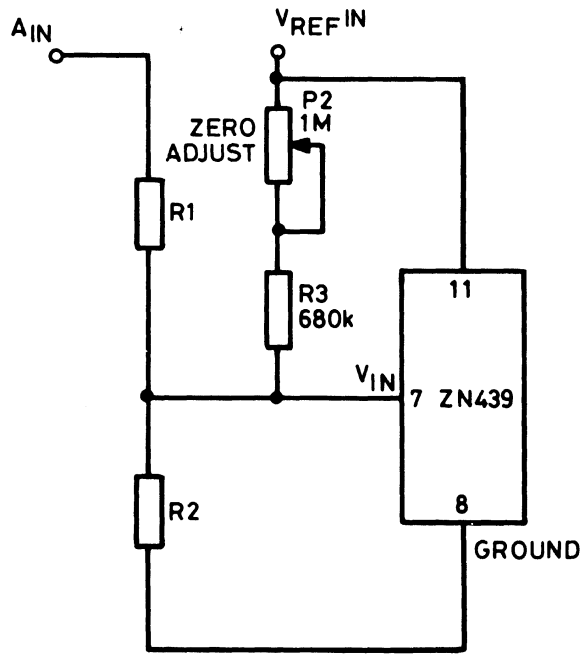


Fig. 20 General unipolar input connections

GAIN ADJUSTMENT

Due to tolerances in R_1 and R_2, tolerances in V_{REF} and the gain (full-scale) error of the DAC, some adjustment should be incorporated into R_1 to calibrate the full-scale of the converter. When used with the internal reference and 2% resistors a preset capable of adjusting R_1 by at least $\pm 5\%$ of its nominal value is suggested.

ZERO ADJUSTMENT

Zero adjustment must be provided to set the zero transition to the value of $+\frac{1}{2}$LSB. This is achieved by applying an adjustable positive offset to tie the comparator input via P2 and R_3. The values shown are suitable for all input ranges greater than $1\frac{1}{2}$ times $V_{REF\ IN}$.

Practical circuits values for +5 and +10V input ranges are given in Fig. 21 which incorporates both zero and gain adjustments.

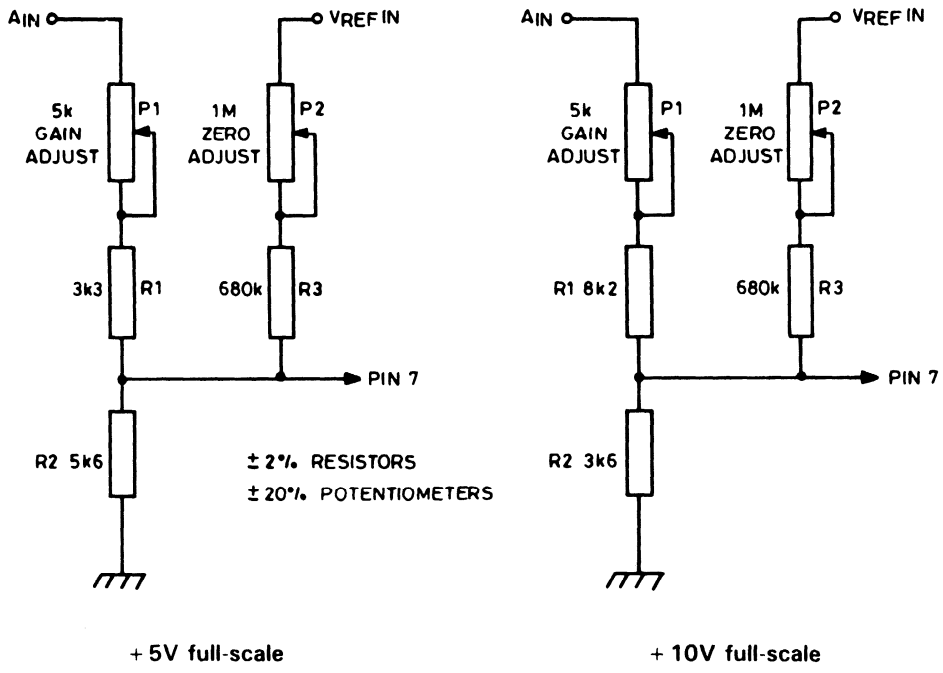


Fig. 21 Unipolar operation component values

UNIPOLAR ADJUSTMENT PROCEDURE

(i) Apply continuous $\overline{WR}$ pulses at intervals long enough to allow a complete conversion or hold $\overline{WR}$ low and monitor the digital outputs.

OFFSET SETTING

(ii) Apply ½LSB to A_{IN} and adjust zero until DB0 (LSB) just flickers between 0 and 1 with all other bits at 0.

i.e. for transition 00000000 to 00000001.

GAIN SETTING

(iii) Apply full-scale minus 1.½LSB to A_{IN} and adjust gain until DB0 (LSB) just flickers between 0 and 1 with all other bits at 1.

i.e. for transition 11111111 to 11111110.

UNIPOLAR SETTING-UP POINTS

Input range, +FS	½LSB	FS - 1½LSB
+5V	9.8mV	4.9707V
+10V	19.5mV	9.9414V

$$1LSB = \frac{FS}{256}$$

UNIPOLAR LOGIC CODING

Analogue input (A_{IN}) (Nominal code centre value)	Output code (Binary)
FS - 1LSB	11111111
FS - 2LSB	11111110
¾FS	11000000
½ FS + 1LSB	10000001
½FS	10000000
½FS - 1LSB	01111111
¼FS	01000000
1LSB	00000001
0	00000000

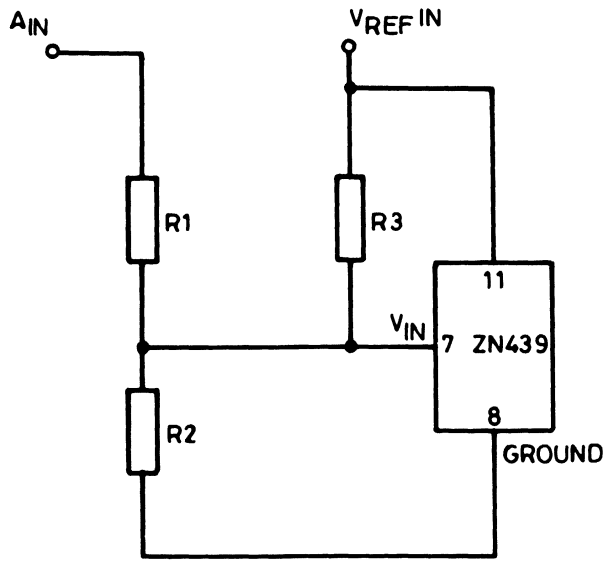


Fig. 22 Basic bipolar input connection

BIPOLAR OPERATION

For bipolar operation the input to the ZN439 is offset by half full-scale by connecting a resistor R_3 between $V_{REF\ IN}$ and V_{IN} (Fig. 22).

When $A_{IN} = -FS$, V_{IN} needs to be equal to zero.

When $A_{IN} = +FS$, V_{IN} needs to be equal to $V_{REF\ IN}$.

If the full-scale range is $\pm G.\ V_{REF\ IN}$ then $R_1 = (G - 1).\ R_2$ and $R_1 = G.\ R_3$ fulfil the required conditions.

To match the ladder resistance, $R_1/R_2/R_3$ $(= R_{IN}) = 2.7k$.

Thus the nominal values of R_1, R_2, R_3 are given by $R_1 = 5.4Gk$, $R_2 = 5.4G/(G - 1)k$, $R_3 = 5.4k$.

A bipolar range of $\pm V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $V_{REF\ IN}$) results if $R_1 = R_3 = 5.4k$ and $R_2 = \infty$.

Assuming the $V_{REF\ IN} = 2.5V$ the nominal values of resistors for ± 5 and $\pm 10V$ input ranges are given in the following table.

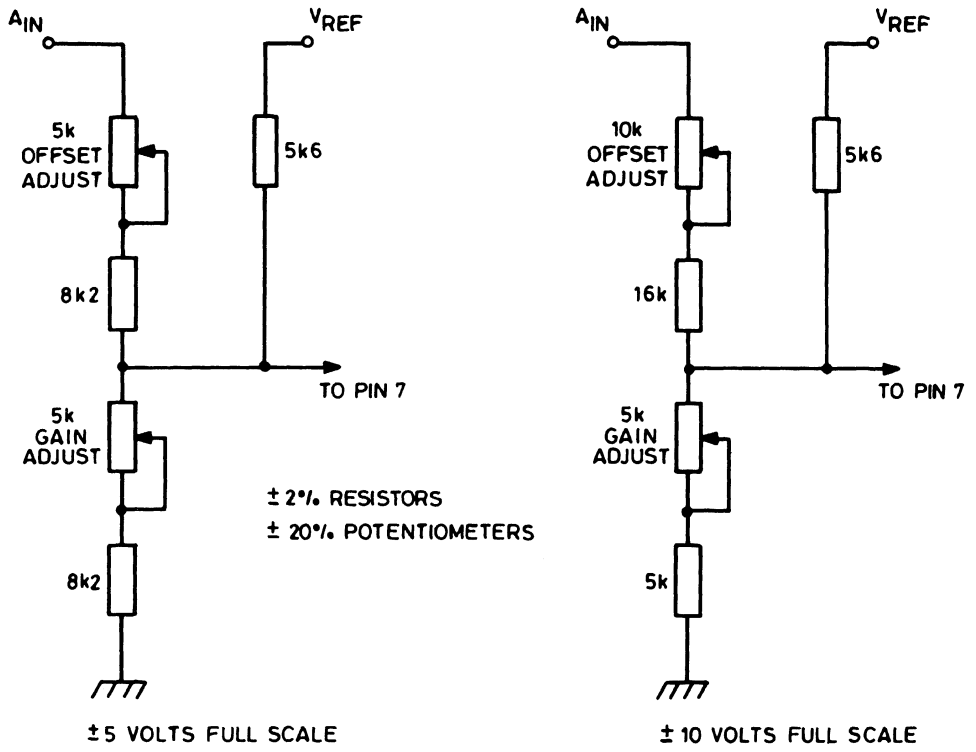


Fig. 23 Bipolar operation - component values

Input range	G	R_1	R_2	R_3
±5V	2	10.8k	10.8k	5.4k
±10V	4	21.6k	7.2k	5.4k

Minus full-scale (offset) is set by adjusting R_1 about its nominal value relative to R_3. Plus full-scale (gain) is set by adjusting R_2 relative to R_1. Practical circuit realisations are given in Fig. 23.

BIPOLAR ADJUSTMENT PROCEDURE

(i) Apply continuous $\overline{WR}$ pulses at intervals long enough to allow a complete conversion or hold $\overline{WR}$ low and monitor the digital outputs.

OFFSET SETTING

(ii) Apply $-(FS - \frac{1}{2}LSB)$ to A_{IN} and adjust offset until the DB0 (LSB) output just flickers between 0 and 1 with all other bits at 0.

i.e. for transition 00000000 to 00000001.

GAIN SETTING

(iii) Apply $+(FS - 1\frac{1}{2}LSB)$ to A_{IN} and adjust gain until DB0 (LSB) just flickers between 0 and 1 with all other bits at 1.

i.e. for transition 11111111 to 11111110.

BIPOLAR SETTING-UP POINTS

Input range, $\pm FS$	$-(FS - \frac{1}{2}LSB)$	$+(FS - 1\frac{1}{2}LSB)$
$\pm 5V$	−4.9805V	+4.9414V
$\pm 10V$	−9.9609V	+9.8828V

$$1LSB = \frac{2FS}{256}$$

BIPOLAR LOGIC CODING

Analogue input (A_{IN}) (Nominal code centre value)	Digital output code MSB LSB
+(FS - 1LSB)	11111111
+(FS - 2LSB)	11111110
$+\frac{1}{2}FS$	11000000
+1LSB	10000001
0	10000000
−1LSB	01111111
$-\frac{1}{2}FS$	01000000
−(FS - 1LSB)	00000001
−FS	00000000

PLESSEY
Semiconductors

ZN447/ZN448/ZN449

8-BIT MICROPROCESSOR COMPATIBLE A-D CONVERTERS

The ZN447, ZN448 and ZN449 are 8-bit, successive approximation A-D converters designed for easy interfacing to microprocessors. All active circuitry is contained on-chip including a clock generator and stable 2.5V bandgap reference.

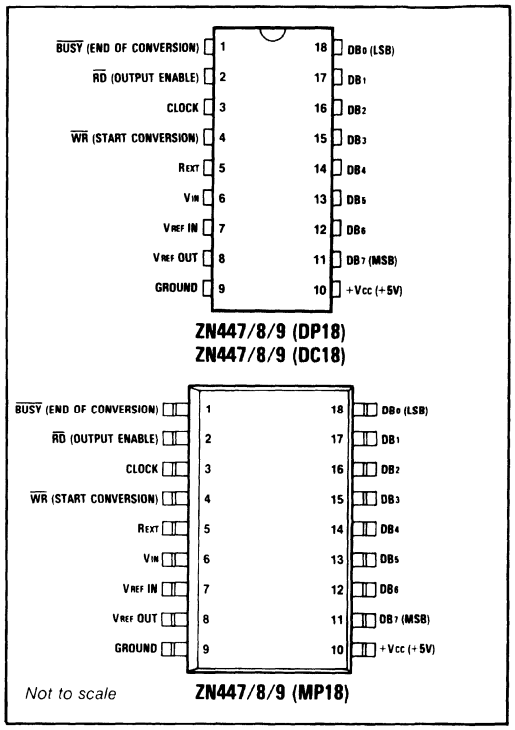
Only a reference resistor and capacitor, clock resistor and capacitor and input resistors are required for operation with either unipolar or bipolar input voltage.

FEATURES

- Easy Interfacing to Microprocessor, or operates as a 'Stand-Alone' Converter
- Fast: 9 microseconds Conversion time Guaranteed
- Choice of Linearity: 0.3 LSB — ZN447, 0.5 LSB — ZN448, 1 LSB — ZN449
- On-Chip Clock
- Choice of On-Chip or External Reference Voltage
- Unipolar or Bipolar Input Ranges
- Commercial or Military Temperature Ranges

ORDERING INFORMATION

Device type	Linearity error (LSB)	Operating temperature	Package
ZN447D	0.3	0°C to + +70°C	MP18
ZN447E	0.3	0°C to + +70°C	DP18
ZN447J	0.3	-55°C to +125°C	DC18
ZN448D	0.5	0°C to + +70°C	MP18
ZN448E	0.5	0°C to + +70°C	DP18
ZN448J	0.5	-55°C to +125°C	DC18
ZN449D	1.0	0°C to + +70°C	MP18
ZN449E	1.0	0°C to + +70°C	DP18
ZN449J	1.0	-55°C to +125°C	DC18



Pin connections - top view

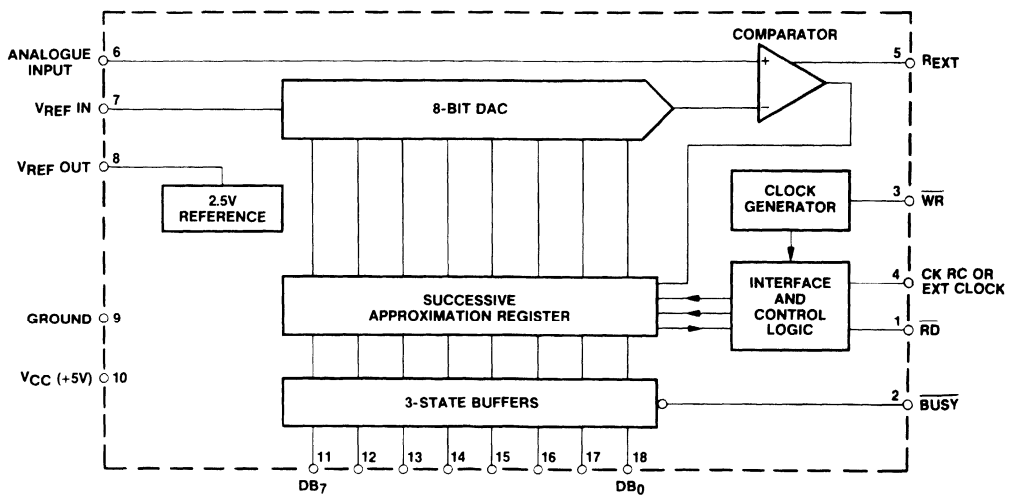


Fig.1 System diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC} +	+7V
Max. voltage, logic and V_{REF} inputs	$+V_{CC}$
Operating temperature range	0°C to +70°C (MP and DP packages) -55°C to +125°C (DC package)
Storage temperature range	-55°C to +125°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5V, T_{amb} = 25°C, f_{CLK} = 900kHz, unless otherwise specified).

Parameter	Min.	Typ.	Max.	Units	Conditions
ZN447					
Linearity error	–	–	±0.3	LSB	
Differential linearity error	–	–	±0.5	LSB	
Zero transition (00000000→00000001)	10.5	12	13.5	mV	MP package
	13.5	15	16.5	mV	DP package
	15	16.5	18	mV	DC package
Full-scale transition (11111110→11111111)	2.548	2.550	2.552	V	V_{REF} = 2.560V
ZN448					
Linearity error	–	–	±0.5	LSB	
Differential linearity error	–	–	±0.75	LSB	
Zero transition (00000000→00000001)	9	12	15	mV	MP package
	12	15	18	mV	DP package
	13	16.5	20	mV	DC package
Full-scale transition (11111110→11111111)	2.545	2.550	2.555	V	V_{REF} = 2.560V
ZN449					
Linearity error	–	–	±1	LSB	
Differential linearity error	–	–	±1	LSB	
Zero transition (00000000→00000001)	7	12	17	mV	MP package
	10	15	20	mV	DP package
	11.5	16.5	21.5	mV	DC package
Full-scale transition (00000000→11111111)	2.542	2.550	2.558	V	V_{REF} = 2.560V
All types					
Resolution	8	–	–	bits	
Linearity temperature coefficient	–	±3	–	ppm/°C	
Differential linearity temperature coefficient	–	±6	–	ppm/°C	
Full-scale temperature coefficient	–	±2.5	–	ppm/°C	
Zero temperature coefficient	–	±8	–	μV/°C	
Reference input range	1	–	3	V	
Supply voltage	4.5	5	5.5	V	
Supply current	–	25	40	mA	
Power consumption	–	125	200	mW	

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	Min.	Typ.	Max.	Units	Conditions
Comparator					
Input current	–	1	–	μA	$V_{IN} = +3V$, $R_{EXT} = 82k\Omega$
Input resistance	–	100	–	kΩ	
Tail current	25	65	150	μA	$V- = -5V$
Negative supply	−3	−5	−30	V	
Input voltage	−0.5	–	+3.5	V	
On-chip reference					
Output voltage ZN447	2.520	2.550	2.580		$R_{REF} = 390\Omega$
ZN448	2.520	2.550	2.580	V	
ZN449	2.500	2.550	2.600		$C_{REF} = 4\mu7$
Slope resistance	–	0.5	2	Ω	
V_{REF} temperature coefficient	–	50	–	ppm/°C	
Reference current	4	–	15	mA	
Clock					
On-chip clock frequency	–	–	1	MHz	
Clock frequency temperature coefficient	–	+0.5	–	%/°C	
Clock resistor	–	–	2	kΩ	
Maximum external clock frequency	0.9	–	1	MHz	
Clock pulse width	500	–	–	ns	
High level input voltage V_{IH}	4	–	–	V	
Low level input voltage V_{IL}	–	–	0.8	V	
High level input current I_{IH}	–	–	800	μA	$V_{IN} = +4V$, $V_{CC} = MAX$
Low level input current I_{IL}	–	–	−500	μA	$V_{IN} = +0.8V$, $V_{CC} = MAX$
Logic (over operating temperature range)					
Convert input					
High level input voltage V_{IH}	2	–	–	V	
Low level input voltage V_{IL}	–	–	0.8	V	
High level input current I_{IH}	–	300	–	μA	$V_{IN} = +2.4V$, $V_{CC} = MAX$
Low level input current I_{IL}	–	±10	–	μA	$V_{IN} = +0.4V$, $V_{CC} = MAX$
$\overline{RD}$ input					
High level input voltage V_{IH}	2	–	–	V	
Low level input voltage V_{IL}	–	–	0.8	V	
High level input current I_{IH}	–	+150	–	μA	$V_{IN} = +2.4V$, $V_{CC} = MAX$
Low level input current I_{IL}	–	−300	–	μA	$V_{IN} = +0.4V$, $V_{CC} = MAX$

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	Min.	Typ.	Max.	Units	Conditions
High level output voltage V_{OH}	2.4	–	–	V	I_{OH} = MAX, V_{CC} = MIN
Low level output voltage V_{OL}	–	–	0.4	V	I_{OL} = MAX, V_{CC} = MIN
High level output current I_{OH}	–	–	– 100	μA	
Low level output current I_{OL}	–	–	1.6	mA	
Three-state disable output leakage	–	–	2	μA	V_{OUT} = + 2V
Input clamp diode voltage	–	–	– 1.5	V	
$\overline{RD}$ input to data output	–	180	250	ns	
Enable/disable delay times T_{E1}	180	210	260	ns	
T_{E0}	60	80	100	ns	
T_{D1}	80	110	140	ns	
T_{D0}	60	80	100	ns	
Convert pulse width $t_{\overline{WR}}$	200	–	–	ns	
$\overline{WR}$ input to $\overline{BUSY}$ output	–	–	250	ns	

GENERAL CIRCUIT OPERATION

The ZN447 utilises the successive approximation technique. Upon receipt of a negative-going pulse at the $\overline{WR}$ input the $\overline{BUSY}$ output goes low, the MSB is set to 1 and all other bits are set to 0, which produces an output voltage of $V_{REF/2}$ from the DAC. This is compared to the input voltage V_{IN}; a decision is made on the next negative clock edge to reset the MSB to 0 if $\frac{V_{REF}}{2} > V_{IN}$ or leave it set to 1 if $\frac{V_{REF}}{2} < V_{IN}$. Bit 2 is set to 1 on the same clock edge, producing an output from the DAC of $\frac{V_{REF}}{4}$ or $\frac{V_{REF}}{2} + \frac{V_{REF}}{4}$ depending on the state of the MSB. This voltage is compared to V_{IN} and on the next clock edge a decision is made regarding bit 2, whilst bit 3 is set to 1. This procedure is repeated for all eight bits. On the eighth negative clock edge $\overline{BUSY}$ goes high indicating that the conversion is complete.

During a conversion the $\overline{RD}$ input will normally be held high to keep the three-state buffers in their high impedance state. Data can be read out by taking $\overline{RD}$ low, thus enabling the three-state outputs. Readout is non-destructive.

CONVERSION TIMING

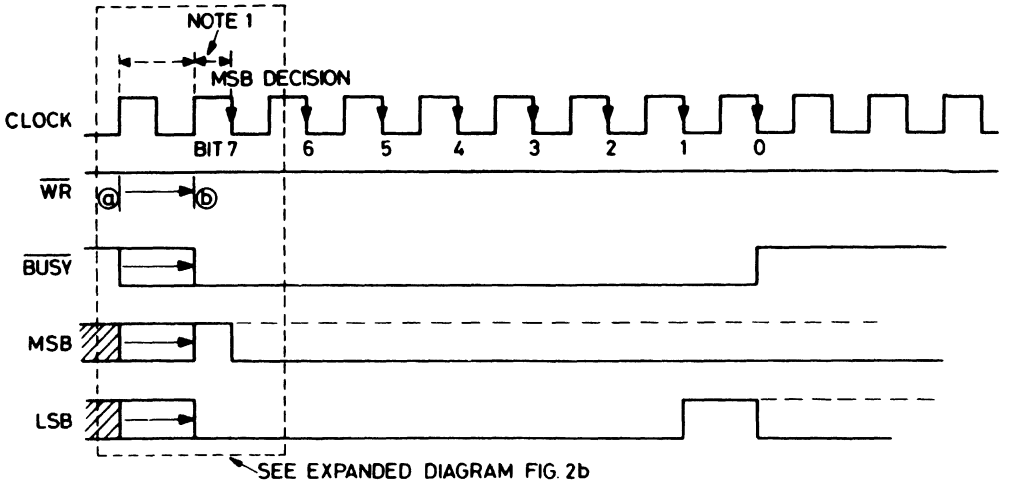
The ZN447 will accept a low-going CONVERT pulse, which can be completely asynchronous with respect to the clock, and will produce valid data between 7.5 and 8.5 clock pulses later depending on the relative timing of the clock and CONVERT signals. Timing diagrams for a conversion are shown in Fig. 2.

The converter is cleared by a low-going CONVERT pulse, which sets the most significant bit and resets all the other bits and the $\overline{BUSY}$ flag. Whilst the CONVERT input is low the MSB output of the DAC is continuously compared with the analogue input, but otherwise the converter is inhibited.

After the CONVERT input goes high again the MSB decision is made and the successive approximation routine runs to completion.

The CONVERT pulse can be as short as 200ns; however the MSB must be allowed to settle for at least 550ns before the MSB decision is made. To ensure that this criterion is met even with short CONVERT pulses the converter waits, after the CONVERT input goes high, for a rising clock edge followed by a falling clock edge, the MSB decision being taken on the falling clock edge. This ensures that the MSB is allowed to settle for at least half a clock period, or 550ns at maximum clock frequency. The CONVERT input is not locked out during a conversion and if it is pulsed low at any time the converter will restart.

The $\overline{BUSY}$ output goes high simultaneously with the LSB decision, at the end of a conversion indicating data valid. Note that if the three-state data outputs are enabled during a conversion the valid data will be available at the outputs after the rising edge of the $\overline{BUSY}$ signal. If, however, the outputs are not enabled until after $\overline{BUSY}$ goes high then the data will be subject to the propagation delay of the three-state buffers. (See under DATA OUTPUTS).



NOTE 1. GUARANTEED PERIOD OF 0.5 CLOCK CYCLE MIN. 1.5 CLOCK CYCLES MAX. ALLOWS MSB TO SETTLE BEFORE MSB DECISION

Fig. 2a

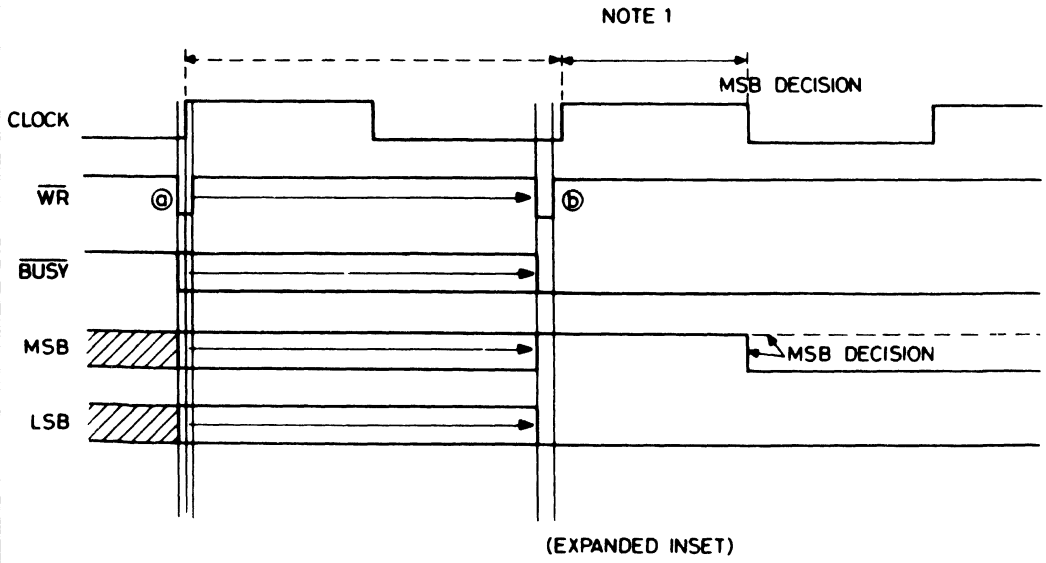


Fig. 2b

Fig. 2 ZN447 timing diagram

CONTINUOUS CONVERSION

If a free-running conversion is required then the converter can be made to cycle by inverting the BUSY output and feeding it to the CONVERT input. To ensure that the converter starts reliably after power up an initial start pulse is required. This can be ensured by using a NOR gate instead of an inverter and feeding it with a positive going pulse which can be derived from a simple RC network that gives a single pulse when power is applied, as shown in Fig. 3a.

The ADC will complete a conversion on every eighth clock pulse, with the $\overline{BUSY}$ output going high for a period determined by the propagation delay of the NOR gate, during which time the data can be stored in a latch. The time available for storing data can be increased by inserting delays into the inverter path.

A timing diagram for the continuous conversion mode is shown in Fig. 3b.

As the $\overline{BUSY}$ output uses a passive pull-up the rise time of this output depends on the RC time constant of the pull-up resistor and load capacitance. In the continuous conversion mode the use of a 4k7 external pull-up resistor is recommended to reduce the risetime and ensure that a logic 1 level is reached.

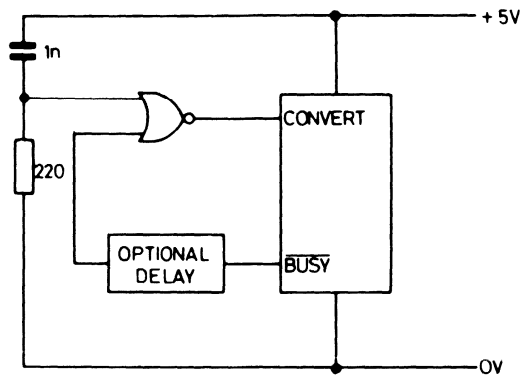


Fig. 3a Circuit for continuous conversion

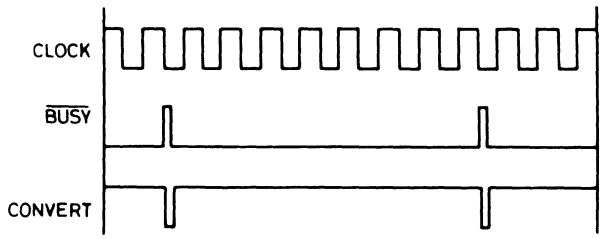


Fig. 3b Timing for continuous conversion

DATA OUTPUTS

The data outputs are provided with three-state buffers to allow connection to a common data bus. An equivalent circuit is shown in Fig. 4. Whilst the $\overline{RD}$ input is high both output transistors are turned off and the ZN447 presents only a high impedance load to the bus.

When $\overline{RD}$ is low the data outputs will assume the logic states present at the outputs of the successive register.

A test circuit and timing diagram for the output enable/disable delays are given in Fig. 5.

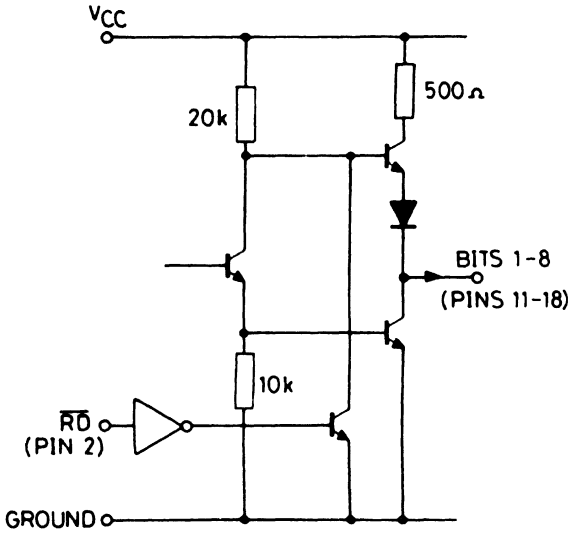


Fig. 4 Data output

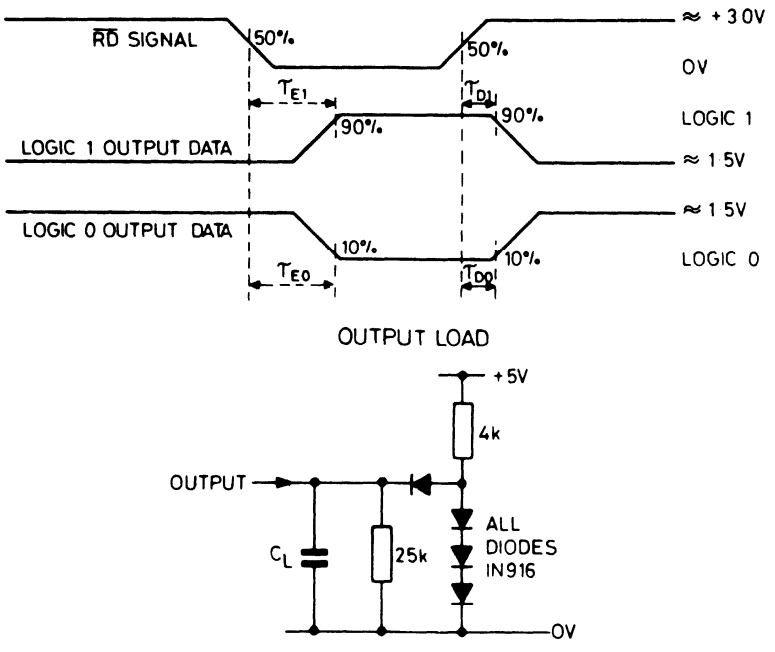


Fig. 5 Output enable/disable delays

$\overline{\text{BUSY}}$ OUTPUT

The $\overline{\text{BUSY}}$ output, shown in Fig. 6, utilises a passive pull-up for CMOS/TTL compatibility. This also allows up to four $\overline{\text{BUSY}}$ outputs to be wire-ANDed together to form a common interrupt line.

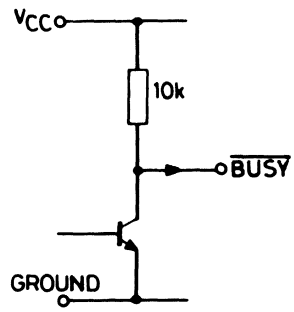


Fig. 6 $\overline{\text{BUSY}}$ output

ON-CHIP CLOCK

The on-chip clock operates with only a single external capacitor connected between pin 3 and ground as shown in Fig. 7a. A graph of typical oscillator frequency versus capacitance is given in Fig. 8. The oscillator frequency may be trimmed by means of an external resistor in series with the capacitor, as shown in Fig. 7b. For optimum accuracy and stability of the oscillator frequency without trimming the use of a crystal or ceramic resonator is recommended, as shown in Fig. 7c. The final option is to overdrive the oscillator input with an external clock signal from a TTL or CMOS gate, as shown in Fig. 7d.

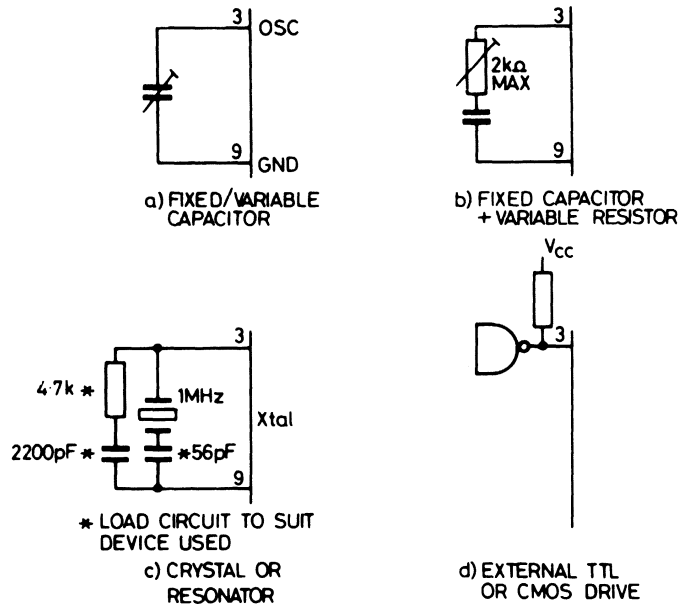


Fig. 7 Clock circuit external components

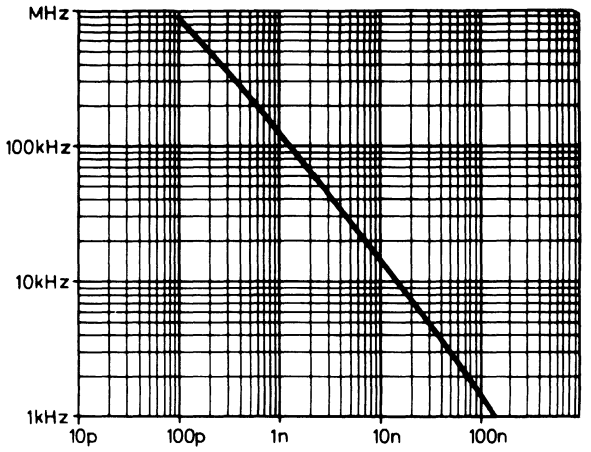


Fig. 8 Typical clock frequency v C_{CK} ($R_{CK} = 0$)

ANALOGUE CIRCUITS

D-A converter

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 9. Each element is connected to either 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (1mV).

A binary weighted voltage is produced at the output of the R-2R ladder.

D to A output $= \frac{n}{256} (V_{REF\ IN} - V_{OS}) + V_{OS}$

where n is the digital input to the D-A from the successive approximation register.

V_{OS} is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. This offset will normally be removed by the setting up procedure and since the offset temperature coefficient is low ($8\mu V/°C$) the effect on accuracy will be negligible.

The D-A output range can be considered to be $0 - V_{REF\ IN}$ through an output resistance R (4k).

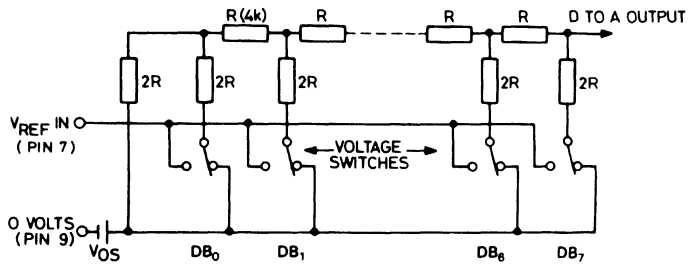


Fig. 9 R-2R ladder network

REFERENCE

(a) Internal reference

The internal reference is an active bandgap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig. 10). A resistor (R_{REF}) should be connected between pins 8 and 10.

The recommended value of 390Ω will supply a nominal reference current of (5 – 2.5) /0.39 = 6.4mA. A stabilising/decoupling capacitor, C_{REF} (4μ7), is required between pins 8 and 9. For internal reference operation $V_{REF\ OUT}$ (pin 8) is connected to $V_{REF\ IN}$ (pin 7).

Up to five ZN447's may be driven from one internal reference, there being no need to reduce R_{REF}. This useful feature saves power and gives excellent gain tracking between the converters.

Alternatively the internal reference can be used as the reference voltage for other external circuits and can source or sink up to 3mA.

(b) External reference

If required an external reference voltage in the range +1.5 to +3V may be connected to $V_{REF\ IN}$. The slope resistance of such a reference source should be less than $\frac{2.5\Omega}{n}$, where n is the number of converters supplied.

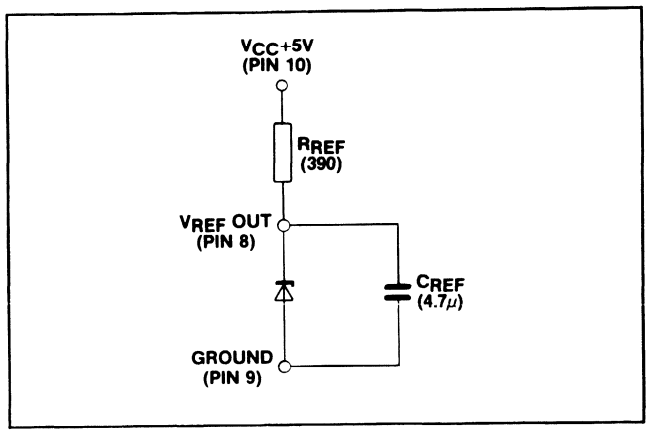


Fig. 10 Internal voltage reference

RATIOMETRIC OPERATION

If the output from a transducer varies with its supply then an external reference for the ZN447 should be derived from the same supply. The external reference can vary from +1.5 to +3V. The ZN447 will operate if $V_{REF\ IN}$ is less than +1.5V but reduced overdrive to the comparator will increase its delay and so the conversion time will need to be increased.

COMPARATOR

The ZN447 contains a fast comparator, the equivalent input circuit of which is shown in Fig. 11. A negative supply voltage is required to supply the tail current of the comparator. However as this is only 25 to 150μA and need not be well stabilised it can be supplied by a simple diode pump circuit driven from the $\overline{BUSY}$ output.

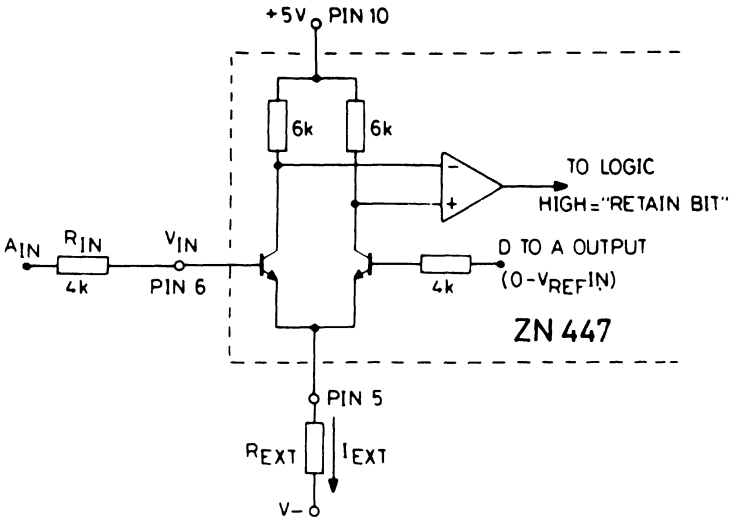


Fig. 11 Comparator equivalent circuit

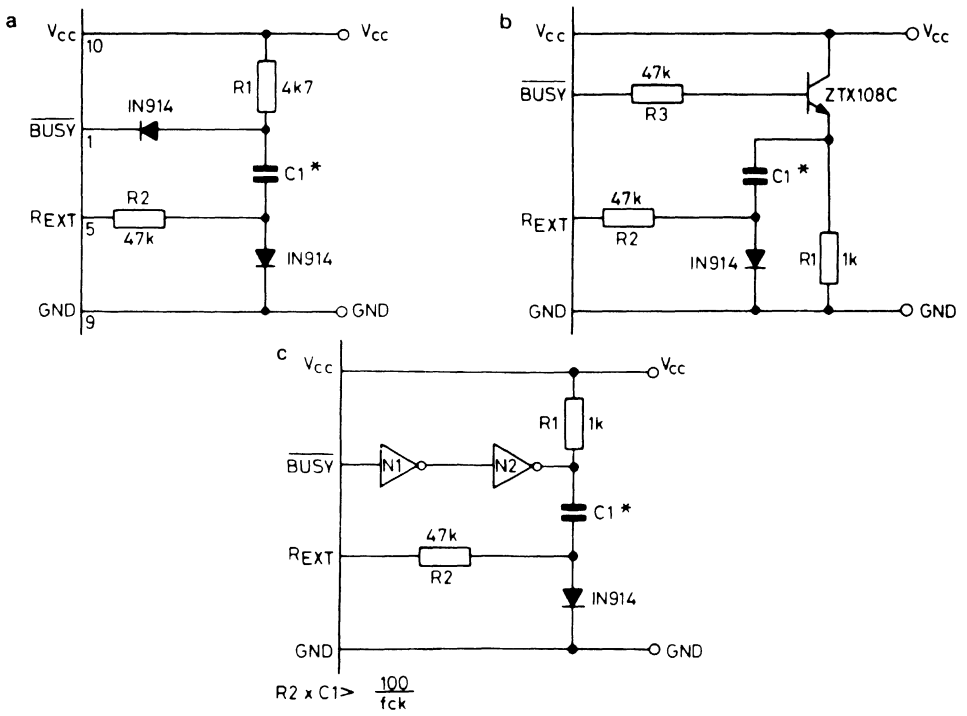


Fig. 12 Diode pump circuits to supply comparator tail current

Several suitable circuits are shown in Fig. 12. The principle of operation is the same in each case. Whilst the $\overline{BUSY}$ output is high, capacitor C1 is charged to about 4-4.5V. During a conversion the $\overline{BUSY}$ output goes low and the upper end of C1 is thus also pulled low. The lower end of C1 therefore applies about −4V to R2, thus providing the tail current for the comparator. The time constant R2. C1 is chosen according to the clock frequency so that droop of the capacitor voltage is not significant during a conversion.

The constraint on using this type of circuit is that C1 must be recharged whilst the $\overline{BUSY}$ output is high. If the $\overline{BUSY}$ output is high for greater than one converter clock period then the circuit of Fig. 12a will suffice. If this is not the case, for example, in the continuous conversion mode, then the circuits of Figs. 12b and 12c are recommended, since these can pump more current into the capacitor.

Where several ZN447's are used in a system the self-oscillating diode pump circuit of Fig. 13 is recommended. Alternatively, if a negative supply is available in the system then this may be utilised. A list of suitable resistor values for different supply voltages is given in table 1.

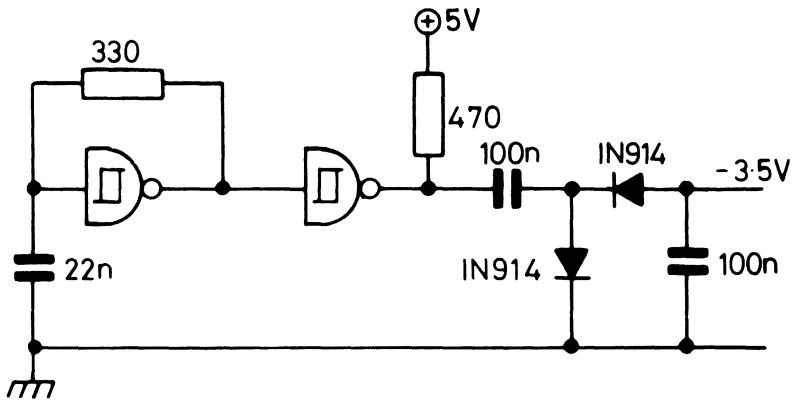


Fig. 13 Diode pump circuit to supply comparator tail current for up to five ZN447's

Table 1

V− (volts)	R_{EXT} (kΩ)
3	47
5	82
10	150
12	180
15	220
20	330
25	390
30	470

ANALOGUE INPUT RANGES

The basic connection of the ZN447 shown in Fig. 14 has an analogue input range 0 to $V_{REF\,IN}$ which, in some applications, may be made available from previous signal conditioning/ scaling circuits. Input voltage ranges greater than this are accommodated by providing an attenuator on the comparator input, whilst for smaller input ranges the signal must be amplified to a suitable level.

Bipolar input ranges are accommodated by off-setting the analogue input range so that the comparator always sees a positive input voltage.

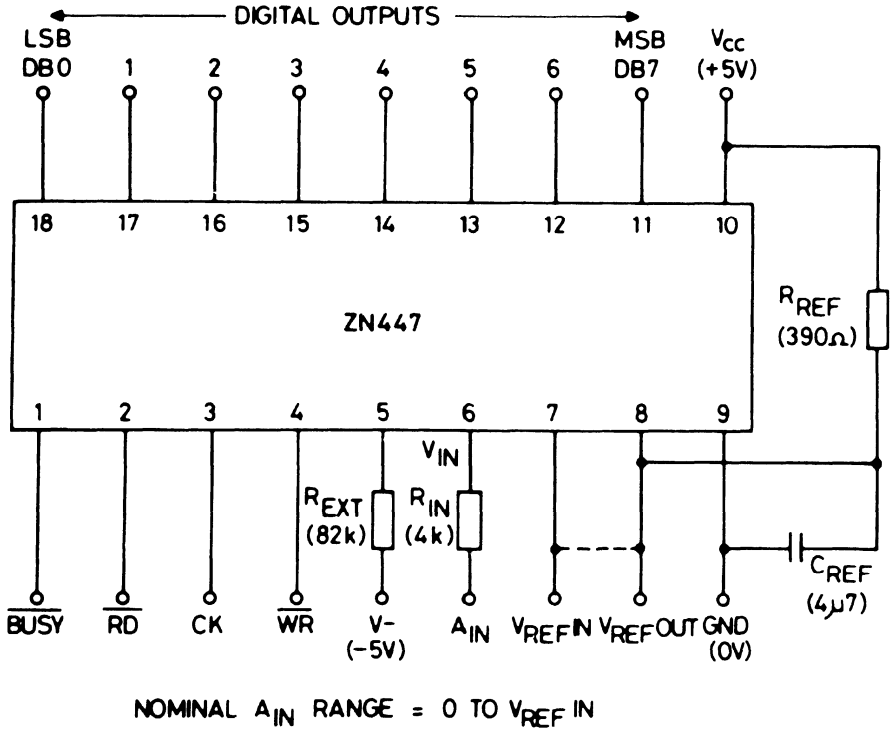


Fig. 14 External components for basic operation

UNIPOLAR OPERATION

The general connection for unipolar operation is shown in Fig. 15.

The values of R_1 and R_2 are chosen so that $V_{IN} = V_{REF\ IN}$ when the Analogue Input (A_{IN}) is at full-scale.

The resulting full-scale range is given by

$A_{IN}\ FS = (1 + \frac{R1}{R2})$, $V_{REF\ IN} = G.V_{REF\ IN}$.

To match the ladder resistance R1/R2 (R_{IN}) = 4k.

The required nominal values of R_1 and R_2 are given by $R_1 = 4G$ k, $R_2 = \frac{4G}{G-1}$ k

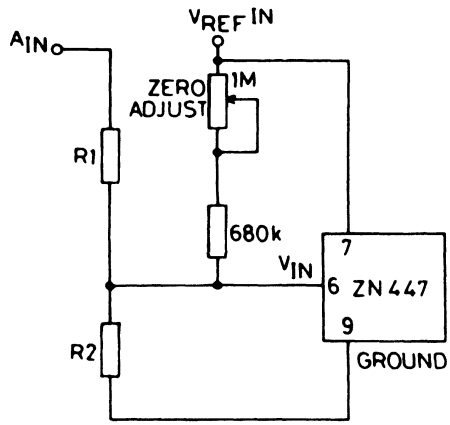


Fig. 15 General unipolar input connections

Using these relationships a table of nominal values of R_1 and R_2 can be constructed for $V_{REF\ IN} = 2.5V$.

Input range	G	R_1	R_2
+5V	2	8k	8k
+10V	4	16k	5.33k

Gain adjustment

Due to tolerances in R_1 and R_2, tolerances in V_{REF} and the gain (full-scale) error of the DAC, some adjustment should be incorporated into R_1 to calibrate the full-scale of the converter. When used with the internal reference and 2% resistors a preset capable of adjusting R_1 by at least ±5% of its nominal value is suggested.

Zero adjustment

Due to offsets in the DAC and comparator the zero (0 to 1) code transition would occur with typically 15mV applied to the comparator input, which corresponds to 1.5LSB with a 2.56V reference.

Zero adjustment must therefore be provided to set the zero transition to its correct value of +0.5LSB or 5mV with a 2.56V reference. This is achieved by applying an adjustable positive offset to the comparator input via P2 and R3. The values shown are suitable for all input ranges greater than 1.5 times $V_{REF\ IN}$.

Practical circuit values for +5 and +10V input ranges are given in Fig. 16, which incorporates both zero and gain adjustments.

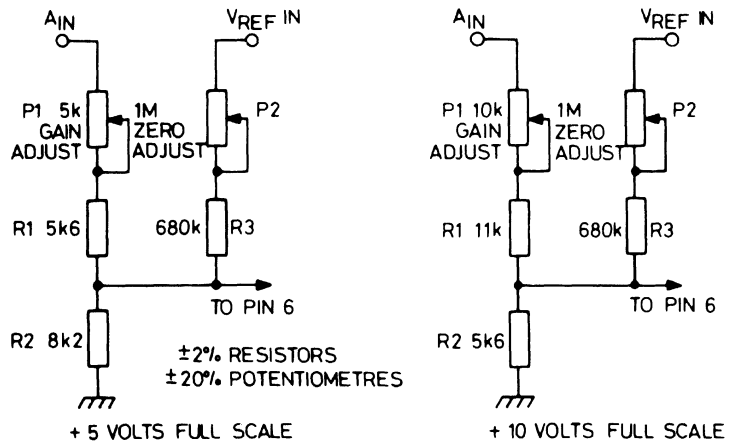


Fig. 16 Unipolar component values

Unipolar adjustment procedure

(i) Apply continuous convert pulses at intervals long enough to allow complete conversion and monitor the digital outputs.

(ii) Apply full-scale minus 1.5LSB to A_{IN} and adjust gain until bit 8 (LSB) output just flickers between 0 and 1 with all other bits at 1.

(iii) Apply 0.5LSB to A_{IN} and adjust zero until bit 8 just flickers between 0 and 1 with all other bits at 0.

Unipolar setting up points

Input range, +FS	0.5LSB	FS - 1.5LSB
+5V	9.8mV	4.9707V
+10V	19.5mV	9.9414V

$$1LSB = \frac{FS}{256}$$

Unipolar logic coding

Analogue input (A_{IN}) (Nominal code centre value)	Output code (Binary)
FS - 1LSB	11111111
FS - 2LSB	11111110
0.75FS	11000000
0.5FS + 1LSB	10000001
0.5FS	10000000
0.5FS - 1LSB	01111111
0.25FS	01000000
1LSB	00000001
0	00000000

BIPOLAR OPERATION

For bipolar operation the input to the ZN447 is offset by half full-scale by connecting a resistor R_3 between $V_{REF\ IN}$ and V_{IN} (Fig. 17).

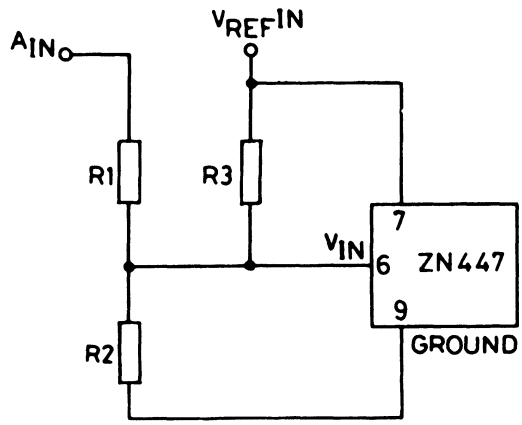


Fig. 17 Basic bipolar input connection

When $A_{IN} = -FS$, V_{IN} needs to be equal to zero.

When $A_{IN} = +FS$, V_{IN} needs to be equal to $V_{REF\ IN}$.

If full-scale range is $\pm G$. $V_{REF\ IN}$ then $R_1 = (G - 1)$. R_2 and $R_1 = G$. R_3 fulfil the required conditions.

To match the ladder resistance, $R_1/R_2/R_3$ $(= R_{IN}) = 4k$.

Thus the nominal values of R_1, R_2, R_3 are given by $R_1 = 8$ Gk, $R_2 = 8G/(G - 1)k$, $R_3 = 8k$.

A bipolar range of $\pm V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $+V_{REF\ IN}$) results if $R_1 = R_3 = 8k$ and $R_2 = \infty$.

Assuming that $V_{REF\ IN} = 2.5V$ the nominal values of resistors for ± 5 and $\pm 10V$ input ranges are given in the following table.

Input range	G	R_1	R_2	R_3
$\pm 5V$	2	16k	16k	8k
$\pm 10V$	4	32k	10.66k	8k

Minus full-scale (offset) is set by adjusting R_1 about its nominal value relative to R_3. Plus full-scale (gain) is set by adjusting R_2 relative to R_1.

Practical circuit realisations are given in Fig. 18.

Note that in the $\pm 5V$ case R_3 has been chosen as 7.5k (instead of 8.2k) to obtain a more symmetrical range of adjustment using standard potentiometers.

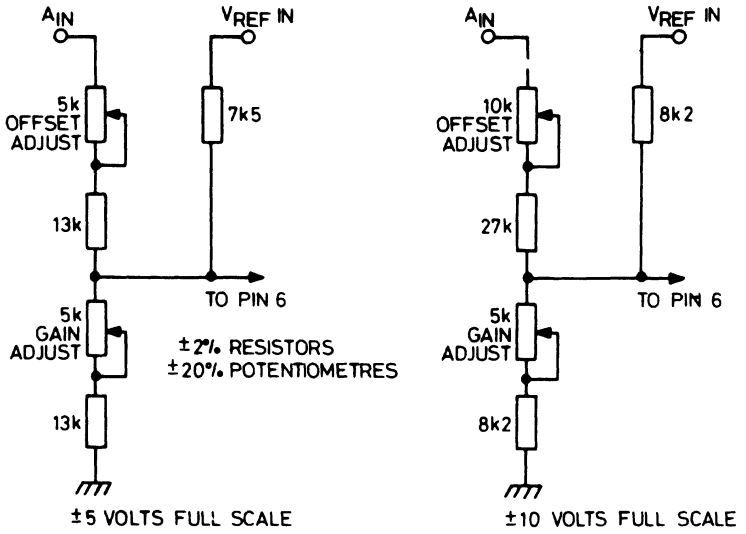


Fig. 18 Bipolar operation - component values

Bipolar adjustment prodedure

(i) Apply continuous SC pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

(ii) Apply −(FS - 0.5LSB) to A_{IN} and adjust offset until the bit 8 (LSB) output just flickers between 0 and 1 with all other bits at 0.

(iii) Apply +(FS - 1.5LSB) to A_{IN} and adjust gain until bit 8 just flickers between 0 and 1 with all other bits at 1.

(iv) Repeat step (ii).

Bipolar setting up points

Input range, ±FS	−(FS −0.5LSB)	+(FS −1.5LSB)
±5V	−4.9805V	+4.9414V
±10V	−9.9609V	+9.8828V

$$1LSB = \frac{2FS}{256}$$

Bipolar logic coding

Analogue input (A_{IN}) (Nominal code centre value)	Output code (Offset binary)
+(FS - 1LSB)	11111111
+(FS - 2LSB)	11111110
+0.5FS	11000000
+1LSB	10000001
0	10000000
−1LSB	01111111
−0.5FS	01000000
−(FS - 1LSB)	00000001
−FS	00000000

PLESSEY
Semiconductors

ZN450

SINGLE CHIP 3½ DIGIT DVM IC

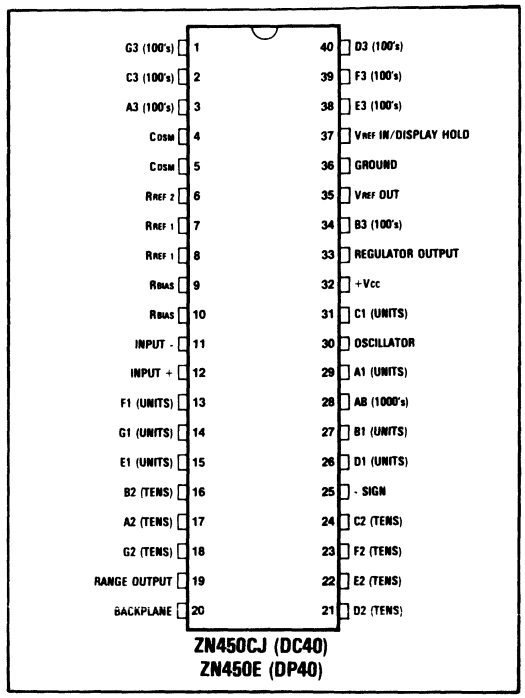
The ZN450 is a complete digital voltmeter fabricated on a monolithic chip and requires only ten external, passive components for operation. A novel charge-balancing conversion technique ensures good linearity. The auto-zero function is completely digital in operation, thus obviating the need for a capacitor to store the error voltage. This versatile IC can be used as the basis not only for digital voltmeters and multimeters but also for other instruments such as digital thermometers.

FEATURES

- 199.9mV Full-Scale Reading
- Digital Auto-Zero with Guaranteed Zero Reading for 0V Input
- True Polarity at Zero for Null Detection
- True Differential Inputs
- Direct Drive of Liquid Crystal Display
- On-Chip Clock and Precision Reference
- Underrange/Overrange Indication
- Low Power Consumption, less than 35mW
- Wide Supply Voltage Range, Single Supply Rail
- No External Active Circuits Required

ORDERING INFORMATION

Device type	Operating temperature	Package
ZN450E	0°C to +70°C	DP40
ZN450CJ	0°C to +70°C	DC40



Pin connections - top view

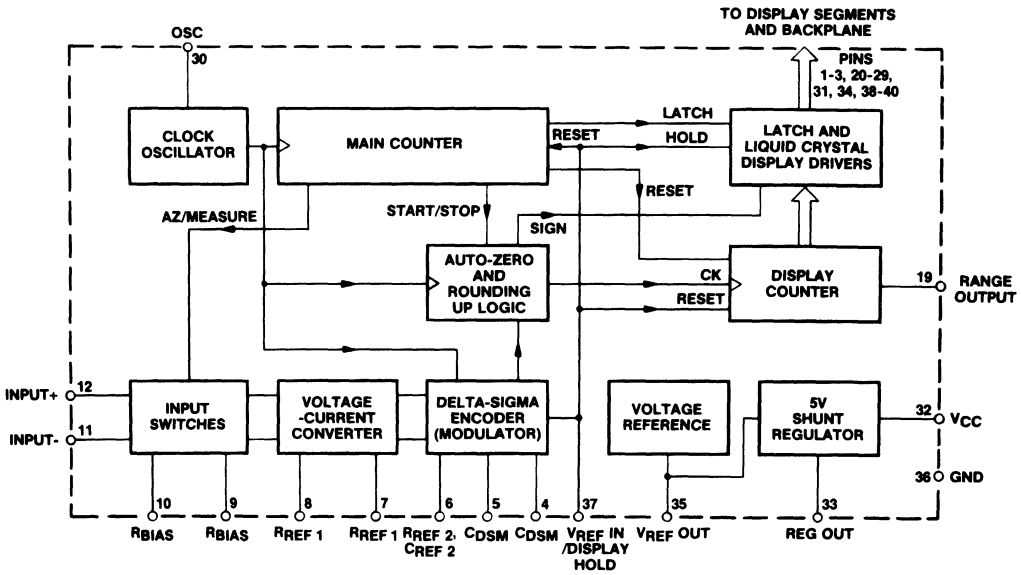


Fig.1 ZN450 System diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	-0.5 to +7.0V
Max. voltage, all other inputs	-0.5 to (V_{CC} +0.5)V
Operating temperature range	0°C to 70°C
Storage temperature range	-55°C to +125°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5V, T_{amb} = +25°C unless otherwise specified).

Parameter	Min.	Typ.	Max.	Unit	Conditions
Full-scale reading	-1999	-	+1999		
Zero reading	-000.0	±000.0	+000.0	digital reading	V_{IN} = 0, V_{FS} = 200mV
Rollover error	-2	0	+2	count	$-V_{IN} = +V_{IN} = \pm 200$mV conversion time ≥ 0.5 sec.
Linearity	-1	0	+1	count	V_{FS} = 200mV conversion time ≥ 0.5 sec.
Common mode range	1.8	-	3.8	V	
Common mode rejection	-	120	-	μV/V	
Supply rejection	-	100	-	μV/V	
Input offset current	-	0.1	1	nA	Input bias resistors matched to 0.1%
Input resistance	7	10	13	MΩ	With 10M input resistors
Zero temperature coefficient	-	-	1	μV/°C	
Full-scale temperature coefficient	Determined by tracking of external resistors				Ref. T.C. = 0ppm/°C
Oscillator frequency range	-	-	300	kHz	
Conversion time (48000 oscillator periods)	0.25	-	-	seconds	
Voltage reference					
Output voltage	1.26	1.3	1.35	V	
Temperature coefficient	-	50	80	ppm/°C	
Knee current	-	-	150	μA	
Maximum sink current	1	2	-	mA	
Supply voltage					
(a) Direct	4.5	5	5.5	V	
(b) Using on-chip shunt regulator	6.0	-	-	V	
(c) Using external NPN transistor	6.5	-	-	V	
(d) Using two transistor regulator	5.5	-	-	V	
Supply current	-	4	8	mA	
Shunt regulator					
Output voltage	4.5	5	5.5	V	
Sink current	-	-	15	mA	
Display outputs					
Peak voltage	-	$\pm V_{CC}$	-		
D.C. component	-	-	±25	mV	
Backplane frequency	-	$\frac{1}{2000}$	-	oscillator frequency	

GENERAL DESCRIPTION

The ZN450 utilises a charge-balancing conversion principle, which offers a number of advantages over the more common dual-slope integration method.

These include a fixed conversion time which is independent of the analogue input voltage, completely digital auto-zero and inherently bipolar operation. Linearity is also extremely good over the entire input voltage range, unlike some dual-slope designs where stray capacitance can cause problems around zero.

The conversion time of the ZN450 is divided into two periods, measure and auto-zero, unlike the dual-slope system which has three distinct phases, signal integrate, reference integrate and auto-zero.

The heart of the ZN450 is the delta-sigma encoder, a simplified circuit of which is shown in Fig. 2.

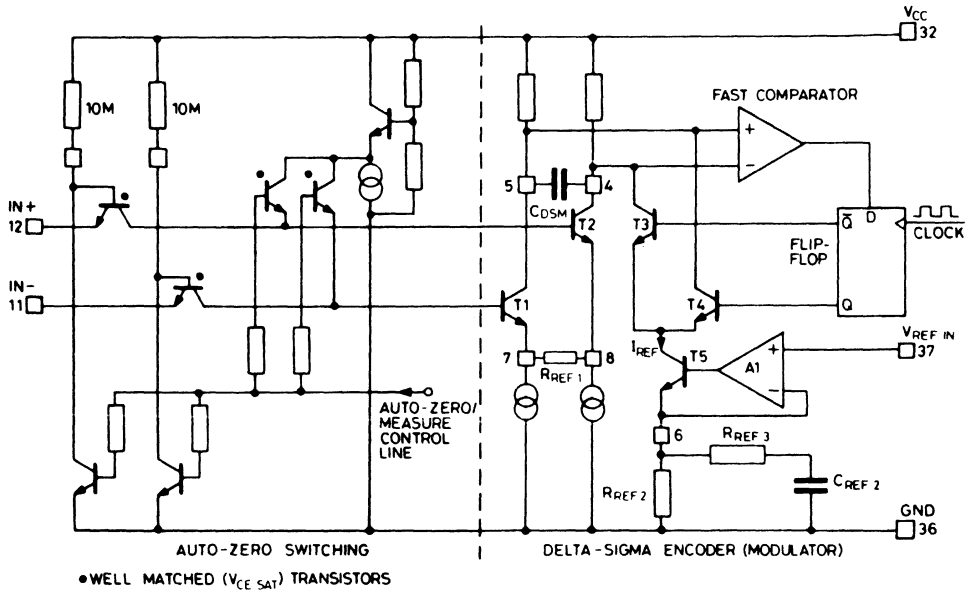


Fig. 2 Input switching and delta-sigma encoder

The delta-sigma encoder of the ZN450 consists of a voltage-current converter comprising T_1 and T_2, a reference generator A1/T5 and a feedback loop containing a fast comparator, D-type flip-flop and current switches T_3 and T_4.

These can switch a current $I_{REF} = \frac{V_{REF}}{R_{REF2}}$ into the collector circuit of either T_1 or T_2, depending on the state of the flip-flop.

The polarity of the voltage across capacitor C_{DSM} is monitored by the comparator, whose output is sampled on every clock pulse by the flip-flop. The outputs of the flip-flop switch I_{REF} into the collector circuit of either T_1 or T_2 so as to oppose the existing voltage on C_{DSM} i.e. to maintain the average charge acquired by C_{DSM} at zero, thus keeping the circuit in equilibrium.

Assuming perfect symmetry in the circuit, with zero volts applied between the bases of T_1 and T_2 their collector currents will be equal, and the only charge acquired by C_{DSM} will be that put on it by I_{REF}. The flip-flop will thus change state on every clock pulse so that C_{DSM} will alternately acquire charge quanta of $+I_{REF}T_C$ and $-I_{REF}T_C$ (where T_C is the clock period) and the nett charge acquired will be zero. The output of the flip-flop will thus be a square-wave with a 50% duty cycle.

During the measurement phase the voltage to be measured is applied between the bases of T_1 and T_2 and is converted into a current $I_{IN} = \frac{V_{IN}}{R_{REF1}}$ flowing in R_{REF1}. This produces a different current $2I_{IN}$ in the collector currents of T_1 and T_2, so that the charge acquired by C_{DSM} is no longer equal and opposite ($\pm I_{REF}$) but is now $(I_{REF} - 2I_{IN})\ T_C$ when T_4 is turned on and $(-I_{REF} - 2I_{IN})\ T_C$ when T_3 is turned on.

In order to maintain equilibrium the flip-flop will now no longer change state on every clock pulse but will remain in one state for a longer period than it remains in the opposite state.

i.e.

$$N_1 T_C(I_{REF} - 2I_{IN}) + (N - N_1)T_C(-I_{REF} - 2I_{IN}) = 0$$

where N_1 is the number of clock pulses for which the flip-flop output is a '1' and N is the total number of clock pulses over which the measurement is made and assuming N is so large that quantising error can be ignored.

$$\text{Thus } N_1(I_{REF} - 2I_{IN}) = (N - N_1)(I_{REF} + 2I_{IN})$$

At this point it is perhaps worth noting that the DSM saturates (0 or 100% duty cycle) when I_{IN} is plus or minus $\frac{I_{REF}}{2}$.

In order to provide an overload margin for series mode rejection the ZN450's DSM operates with a peak duty-cycle of nominally 10% for minus full-scale and 90% for plus full-scale ($I_{IN} = \pm \frac{2}{5} I_{REF}$) giving an overload margin of 25% of the full-scale input voltage.

Now

$$\frac{2N_1 - N}{N} = \frac{2I_{IN}}{I_{REF}} \text{ i.e. } N_1 - \frac{N}{2} = \frac{NI_{IN}}{I_{REF}} = \frac{NV_{IN}\,R_{REF2}}{R_{REF1}\,V_{REF}}$$

What this means is that an up counter preset to $-\frac{N}{2}$ and allowed to count N_1 will accumulate a number proportional to V_{IN}, assuming N, R_{REF1}, R_{REF2} and V_{REF} are fixed. By suitable choice of these parameters $N_1 - \frac{N}{2}$ can be made directly equal to V_{IN} in volts or millivolts. Furthermore, by making the preset number greater or less than $\frac{N}{2}$ in proportion to any zero error in the system it is possible to provide a digital auto-zero.

The ZN450 indicates positive overrange at a count of +2000 when the duty cycle is 90% and $I_{IN} = \frac{2}{5} I_{REF}$. The required value of N can thus be obtained by substituting the overrange reading of 2000 for $N_1 - \frac{N}{2}$ and the corresponding value of $\frac{2}{5}$, for $\frac{I_{IN}}{I_{REF}}$, $2000 = \frac{2N}{5}$, $N = 5000$.

In fact the display counter is preceded by a +4 stage which is part of the auto-zero logic so the actual measurement period must be 20,000 clock periods to give a maximum of 5000 pulses at the display counter.

The display counter of the ZN450 can count from −5000 to +5000. It is preset to nominally −2500 during the auto-zero phase by allowing it to count from −5000 to −2500, as explained below.

AUTO-ZERO

Due to offsets and component mismatching in the delta-sigma encoder the displayed count accumulated for zero input voltage will not be zero. In order to remove this error and give a true zero reading for 0V input the ZN450 incorporates an auto-zero facility. This is completely digital in operation and there is no need to store the error as an analogue voltage on a capacitor, as is the case with some dual slope-designs. Furthermore the conversion period of the ZN450 comprises two well-defined phases, measure and auto-zero, unlike dual-slope DVMs which have signal integrate, reference integrate and auto-zero phases.

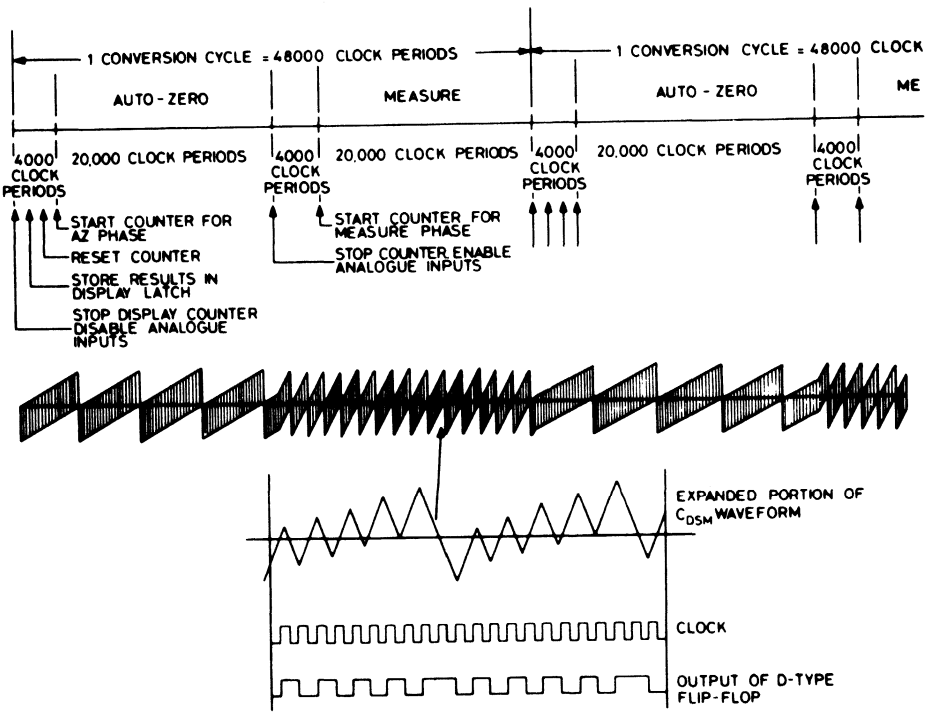


Fig. 3 Timing diagram of ZN450

A timing diagram of the ZN450 is shown in Fig. 3. Its duration is 48000 clock periods and its two principal components are the measurement phase and the auto-zero phase which each occupy 20,000 clock periods. Each phase is separated by a space of 4000 clock periods to allow the input switches to settle. This also illustrates another advantage of the charge balancing conversion technique. Since the delta sigma encoder can run continuously without saturating and its average duty-cycle is always a measure of the input voltage, it is possible to allow the input switches to settle in this way before starting a measurement by activating the system counters.

Contrast this with the dual-slope DVM where the integrator capacitor begins to accumulate charge immediately the input voltage is connected. The system counter must start at the precise instant that the input voltage is connected which means that the input switches must be fast and noise-free. Furthermore termination of the measurement is determined by the comparator accurately detecting a single zero-crossing, so noise in the comparator or from other sources can cause error. In the charge balancing DVM the comparator detects many zero crossings and noise tends to be integrated out.

Operation of the auto-zero system is best understood by considering what happens when an auto-zero phase is followed by a measurement with zero volts input. During the auto-zero phase the inputs of the DSM are disconnected from the analogue inputs and shorted to a point within common-mode range of the DVM. The counter is reset to -5000 and the system is allowed to run for 20,000 clock periods, but with the DSM output inverted. This means that the number of clock pulses counted will be, not N_1 but $(N-N_1)$. During the subsequent measurement with zero input voltage N_1 pulses will be counted, so that the total count will be N, i.e. 5000. The display counter will thus have counted from -5000 up to zero and zero will be displayed.

Due to quantising error inherent in any digital measurement it is possible that the result of the measurement with zero input could differ from the result of the auto-zero by 1 count, thus giving rise to a zero error of ± 1 digit. To avoid this problem the ZN450 incorporates two guard bits in the form of a + 4 stage and rounding up logic preceding the display counter. This means that although the display resolution is 1 part in ± 2000 the resolution of the measurement is four times better. Any zero error in the two (non-displayed) guard bits will not appear in the display and the logic also subdivides the zero state into + 0000 and − 0000 for true polarity indication.

As an additional benefit flicker in the last digit of the display is minimised.

INPUT RESISTANCE

The input resistance of the ZN450 is determined by the two 10M bias resistors, the value of R_{REF1}, and h_{fe} and r_e of T1 and T2.

An equivalent input circuit is shown in Fig. 4. The input resistance comprises h_{fe} ($R_{REF1} + 2_{re}$) in parallel with 20M due to the two 10M input resistors.

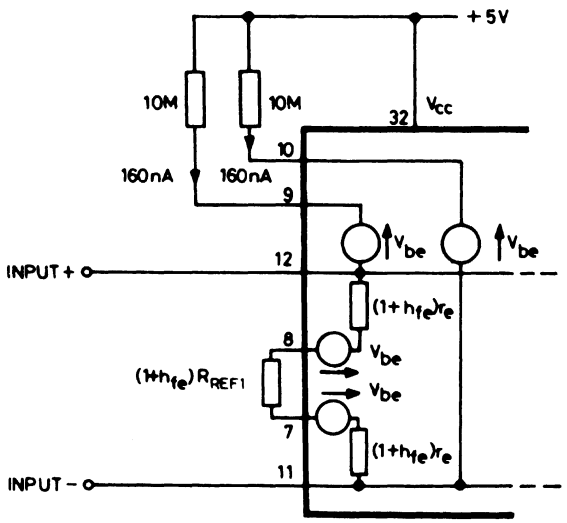


Fig. 4 Equivalent input circuit of the ZN450

The h_{fe} of T1 and T2 is typically about 100 and r_e is around 2.5k, therefore:

$$R_{IN} = \frac{100\ (R_{REF1} + 5k) \times 20M}{100\ (R_{REF1} + 5k) + 20M}$$

For 200mV full-scale, when $R_{REF1} = 200k$ the input resistance is around 10M.

REFERENCE LOOP AND SUPPLY REGULATOR

The reference current defining loop is shown in more detail in Fig. 5.

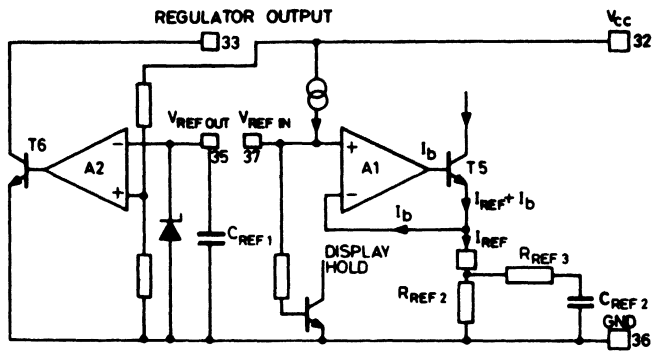


Fig. 5 Reference current loop and supply regulator

A reference input voltage applied to the non-inverting input of A1 causes the output of A1 to bias T5 such that the inverting input of A1 assumes the same potential and a current $\frac{V_{REF\,IN}}{R_{REF2}}$ flows in R_{REF2}. By making the input bias current of A1 the same as the base current of T5 this base current flows into the inverting input of A1 instead of through R_{REF2}. The reference current flowing in the collector of T5 is therefore almost identical to the current flowing in R_{REF2}. The reference loop is stabilised by C_{REF2} and R_{REF3}.

A highly stable on-chip bandgap reference of approximately 1.28V is provided and this may be used by linking $V_{REF\,OUT}$ to $V_{REF\,IN}$ when the reference will be biased on by the 150μA current source connected to the non-inverting input of A1. The on-chip reference is stabilised by C_{REF1}. The on-chip reference also provides the reference voltage for the on-chip supply regulator A2. This compares V_{REF} against $\frac{V_{CC}}{4}$ and controls V_{CC} with transistor T_6 such that the two are kept equal, i.e. $V_{CC}=5V$.

The supply regulator can be configured as a shunt or series regulator using only a few external components.

If $V_{REF\,OUT}$ is not connected to $V_{REF\,IN}$ but supply regulation is still required then the on-chip reference must be biased on by a 22k resistor to V_{CC}.

SETTING FULL-SCALE RANGE

The described equation previously arrived at for the charge-balancing converter was:

$$\frac{NV_{IN}\cdot R_{REF2}}{V_{REF}\cdot R_{REF1}} = N_1 - \frac{N}{2}$$

$$\text{i.e. displayed reading} = \frac{NV_{IN}\cdot R_{REF2}}{V_{REF}\cdot R_{REF1}}$$

and since $N=5000$

$$\text{Displayed reading} = 5{,}000\ \frac{V_{IN}\cdot R_{REF2}}{V_{REF}\cdot R_{REF1}}$$

or, substituting the maximum reading of ± 1999 and rearranging again:

$$V_{IN}(\text{full-scale}) = \frac{\pm 1999 V_{REF}\cdot R_{REF1}}{5000.R_{REF2}} \simeq \frac{\pm 0.4 V_{REF}\cdot R_{REF1}}{R_{REF2}}$$

These equations are in fact not exact since they do not take account of the reference amplifier

offset voltage, which is typically ±5mV. This offset means that I_{REF} is not precisely $\frac{V_{REF}}{R_{REF2}} \cdot r_e$ of T1 and T2 in the voltage current converter also appears with R_{REF2} (typically 5k). In practice this is not a problem since the tolerance of the on-chip reference means that a calibration adjustment must be provided anyway.

Using the on-chip reference voltage of 1.26 - 1.35 volts the recommended component values for a full-scale reading of 199.9mV would be $R_{REF1} = 200k$, $R_{REF2} = 500k$ (min.), 520k (max.). Allowing for the use of 2% tolerance components for R_{REF1} and R_{REF2} an adequate adjustment range for calibration purposes will be provided if R_{REF2} is made up of a 470k resistor in series with a 100k multiturn trimmer. Full-scale ranges less than 200mV can be accommodated by reducing the value of R_{REF1}, thus producing the same full-scale input current for a smaller input voltage. The limitations on the minimum value of R_{REF1} are caused by non-linearity in the voltage-current converter, offsets in the auto-zero switches, and the fact that r_e becomes a much larger proportion of R_{REF1}. These factors place a practical limit of about 20k on R_{REF1}.

Similarly full-scale ranges greater than ±200mV can be accommodated by the value of R_{REF1}. The maximum input voltage that can be applied is limited by the common-mode range of the differential inputs. Provided the common-mode range of either input terminal is not exceeded the maximum differential voltage that can be applied between the inputs is about ±2V.

The full-scale range can also be adjusted by varying R_{REF2} which determines the reference current, and indeed placing a preset in series with R_{REF2} is the recommended method of calibration. I_{REF} can also be varied by using an adjustable external reference voltage instead of the internal reference, which makes ratiometric operation possible.

The minimum value of I_{REF} is limited to about 3μA since above this value the voltage-current converter becomes non-linear. The maximum value of I_{REF} is not quite so well defined as it is determined by deterioration in the performance of current switches T3 and T4 at low collector currents. The minimum usable value of I_{REF} is typically 500nA. This means that the upper and lower limits are $\frac{V_{REF}}{500nA}$ and $\frac{V_{REF}}{3\mu A}$ respectively. The upper and lower limits on V_{REF} itself are determined by the common-mode range of the reference current amplifier A1 which is 1 to 1.5V. Ratiometric operation with a variable V_{REF} within these limits is possible provided that the upper or lower limit of I_{REF} is not exceeded.

SUPPLY VOLTAGE OPTIONS

The ZN450 is designed to be extremely flexible with regard to supply voltage and four power supply options are possible allowing operation over a wide range of supply voltages. These options are illustrated in Fig. 6.

The first option is to ignore the on-chip regulator and to connect an externally stabilised voltage of 4.5 to 5.5V direct to pin 32, for example a 5V logic supply.

For supply voltages greater than 6V the on-chip shunt regulator (pin 33) may be used by linking pins 32 and 33. When using the shunt regulator an external resistor must be placed in series with the supply to limit the regulator current as shown in Fig. 6b. The value of this resistor is given by:

$$R = \frac{V_{supply} - 5 \text{ volts}}{5} \left(k, \frac{V}{mA}\right)$$ which allows for the maximum 8mA current consumption of the I.C.

If the supply voltage is unstabilised then R should be calculated using the minimum supply voltage that will be encountered. The current drawn by this configuration increases with supply voltage as the shunt regulator sinks more current in order to maintain V_{CC} at 5V. The maximum allowable supply voltage is thus determined by the 15mA maximum rating of the shunt regulator, assuming very little current is drawn by the DVM circuitry, i.e.

$$V_{max} = 15(mA) \times R(k\Omega) + 5 \text{ volts}$$
$$= (3V_{min} - 10) \text{ volts}$$

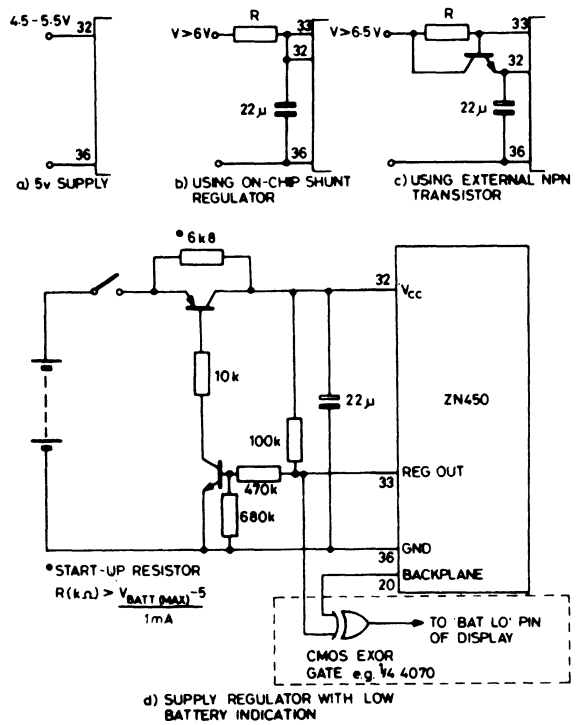


Fig. 6 Supply voltage options

Since the current drawn by the shunt regulator increases with supply voltage this configuration is not recommended for battery operation where long battery life is a prime criterion, as the current drawn from a new battery could be up to three times the maximum current consumption of the DVM.

For battery operation a series regulator circuit is recommended which can be constructed using one or two external transistors controlled by pin 33. The simplest series regulator, shown in Fig. 6c, uses a single NPN transistor and allows operation down to about 6.5V. Current consumption of this circuit is the normal current consumption of the DVM plus the base current of the transistor.

The base resistor must be chosen such that it can supply sufficient base drive when the supply voltage is a mimimum assuming

(a) Maximum DVM current of 8mA

(b) Maximum shunt regulator voltage of 5.5V

(c) Minimum gain of the transistor

$$\text{Now base current } I_b\ (\text{mA}) = \frac{V_{min} - V_{reg} - V_{beT1}}{R_b}$$

$$\text{required base current} = \frac{8\text{mA}}{h_{fe\ (min)}}$$

$$\text{Therefore } R_b(\text{k}\Omega) = \frac{(V_{min} - V_{reg} - V_{beT1}) \times h_{fe}}{8}$$

$$\simeq \frac{(V_{min} - 6) \times h_{fe}}{8}$$

Example. The circuit is to operate down to 6.5V with a transistor type whose minimum gain is 80

$$R_b = \frac{(6.5 - 6) \times 80}{8}$$

$$= 5k$$

Nearest value of 4k7 is used.

Although a great improvement on the shunt regulator, the circuit of Fig. 6c still does not achieve maximum battery life since V_{min} must always exceed the regulator voltage by V_{beT1} plus the voltage drop across R_b.

For the ultimate in battery life the circuit of Fig. 6d is suggested. This allows operation down to voltages as low as $V_{reg} + V_{CE(sat)T1}$ and, as an added bonus, it automatically detects the end of useful battery life, i.e. the point at which the regulator ceases to funtion.

T_1 is a PNP series regulator transistor controlled by pin 33 via T_2, which provides the required signal inversion. During normal operation the voltage drop across R_1 is small since the base current required by T_2 is only a few hundred nanoamps, and the voltage at pin 33 is not much above the V_{be} of T_2 (about 0.6V).

When the battery voltage drops to $V_{reg} + V_{CE(sat)T1}$ the voltage at the non-inverting input of the regulator amplifier will fall below V_{REF} and the shunt regulator output transistor will turn off causing the voltage at pin 33 to rise to about 80% of supply.

Pin 33 can conveniently be connected to a low battery indicator consisting of a CMOS EXOR gate, as shown in the dotted box. When pin 33 is low the output of the EXOR gate will be in phase with the backplane and the LO BAT indicator will be extinguished. When pin 33 is high the output will be out of phase with the backplane and LO BAT will be visible.

OSCILLATOR OPTIONS

The on-chip oscillator of the ZN450 may be used with various configurations of external components, as shown in Fig. 7. It will operate with only an external capacitor, which may be fixed, or variable to adjust the oscillator frequency. Alternatively the frequency may be adjusted by placing a variable resistor in series with the capacitor. Graphs of oscillator frequency versus capacitor and resistor values are given in Fig. 8. If absolute accuracy of the oscillator frequency is required then a crystal or ceramic resonator may be used as the frequency determining element. By making the integration time a whole number of mains cycles a degree of mains interference rejection can be provided. For example a 100kHz crystal gives an integration time of 200ms which is 10 cycles at 50Hz mains frequency or 12 cycles at 60Hz, the total measurement interval being 480ms or just over two conversions/second.

If mains interference is superimposed on the input signal it is important that its peak amplitude should be less than 25% of full-scale to avoid saturation of the DSM. If this is not the case then the ZN450 should be preceded by a lowpass filter to give additional mains rejection.

The final option is to overdrive the oscillator input from a TTL or CMOS gate, as shown in Fig. 7d.

In order to maintain an adequate drive to the comparator the value of C_{DSM} must also be changed in proportion to the oscillator period. A table of suitable values is given below.

Oscillator frequency (kHz)	C_{DSM} Min.	C_{DSM} Max.
50	200n	2μ
100	100n	1μ
150	68n	680n

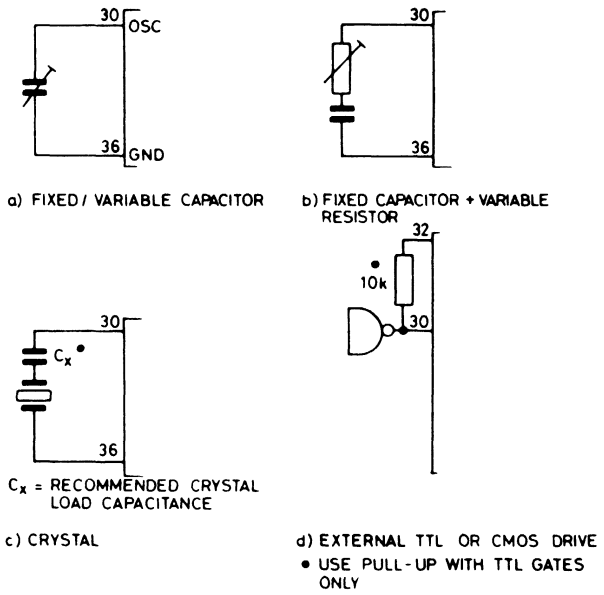


Fig. 7 Oscillator options

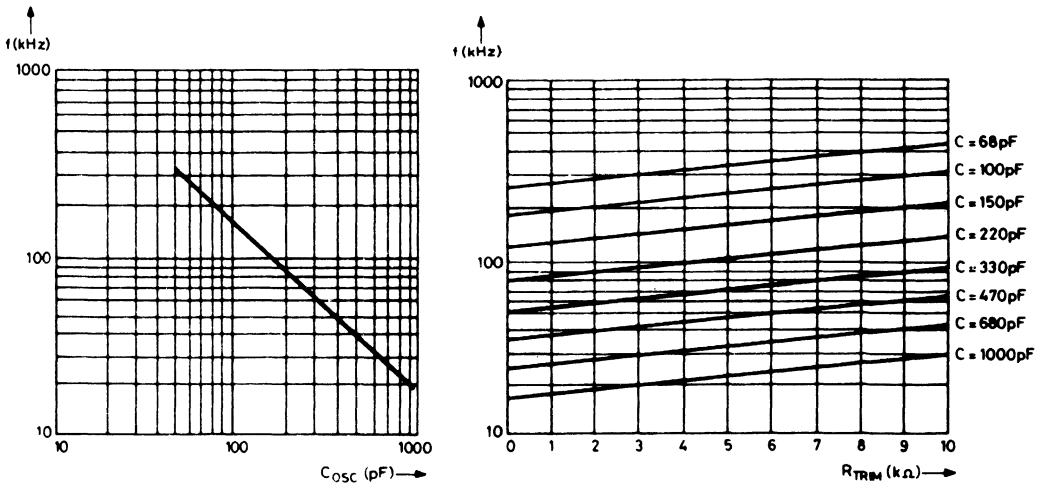


Fig. 8 Oscillator frequency v external capacitor and resistor

RANGE OUTPUT

To simplify the design of auto-ranging instruments, underrange and overrange detection circuits are provided in the ZN450. Overrange is indicated when the count exceeds 1999, whilst underrange is indicated for counts less than 150. This provides a degree of hysteresis to prevent the instrument jittering between ranges, which could occur if underrange was indicated at a count of 199 and there was a mismatch in the attenuators or other signal conditioning circuits.

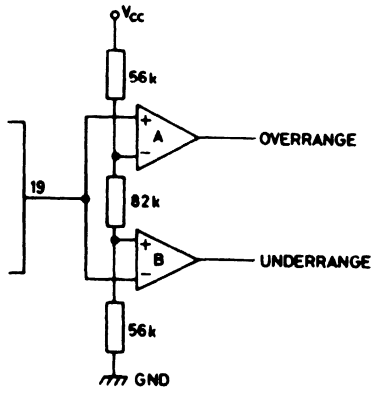
Because the pins of the ZN450 are fully utilised it is not possible to provide separate underrange and overrange pins, so a single three-state output is provided.

If the measurement is in range then pin 19 will be at $\frac{V_{CC}}{2} \pm 0.5V$ with a source resistance of approx. 40k.

For an overrange measurement pin 19 will go HIGH for 1000 clock pulses synchronous with the data store pulse at the end of the measurement. For an underrange measurement pin 19 will pulse LOW in a similar manner. In each case the output resistance is approx. 80k.

The range output can be fully decoded using a dual comparator, as shown in Fig. 9.

A visual overrange indication is also provided. In this condition the leading digit of the display shows a '1' whilst all other digits are blanked.



Range output	Output A	Output B
Underrange (GND)	0	⎍
In range (½ V_{CC})	0	0
Overrange (V_{CC})	⎍	0

Fig. 9 Decoding the range output

DISPLAY HOLD

The reference input, pin 37, also doubles as a display hold pin. If this pin is grounded then the display will continue to show the results of the last valid measurement until pin 37 is released. Display hold also resets the system counters and a new measurement begins immediately display hold is released. The method of activating display hold depends on whether or not the on-chip reference and shunt regulator are being utilised.

If an external reference voltage is used (pins 35 and 37 not joined) then display hold can be activated by grounding pin 37 with a single-pole switch, transistor or open-collector logic gate, provided that the external reference is not required to supply other circuits. If the on-chip regulator is to be used then pin 35 must, of course, be biased up with an external 22k resistor so that V_{REF} can supply the reference voltage for the regulator. If the on-chip reference is used but the on-chip regulator is not then display hold can be activated in a similar manner by grounding the junction of pin 35 and pin 37.

However, since the on-chip reference also provides the reference voltage for the on-chip regulator pin 35 must not be grounded if the regulator is in use or the supply voltage will drop to zero. If the on-chip reference and shunt regulator are both used then pin 37 must be disconnected from pin 35 before it is grounded to activate display hold. This is illustrated in Fig. 10. As pin 37 normally supplies the bias current for the on-chip reference this must be provided by an external 22k resistor when these pins are not linked.

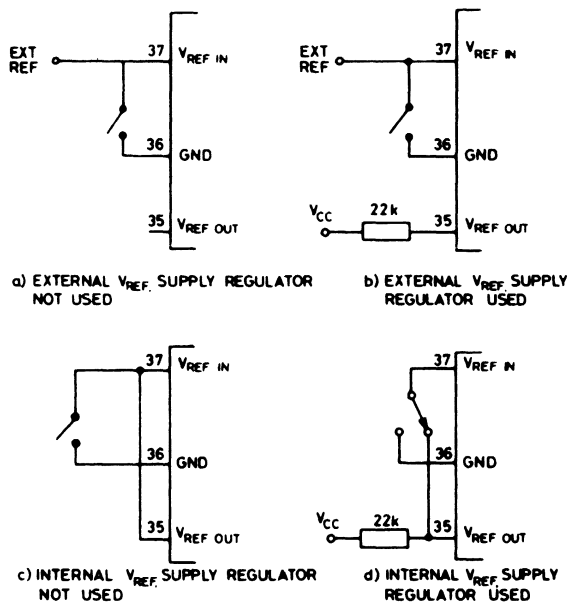


Fig. 10 Display and hold options

BACKPLANE OUTPUT

The backplane output normally provides a squarewave of the same frequency as, but 180° out of phase with, the active segment outputs. This provides the necessary a.c. drive to the L.C. display. By grounding the backplane output the a.c. drive to the segments may be inhibited and the segment outputs become normal active low (TRUE = 0) outputs. This facility is useful if the output data is to be used for some purpose other than display driving. An L.C. display should not be connected to the ZN450 in this condition as d.c. drive will eventually damage it.

DECIMAL POINT DRIVE

The ZN450 provides all the outputs necessary to drive the segments of a 3½ digit liquid crystal display. However, in order to drive decimal points and annunciators such as low battery indicators, some external components are required. To turn on a decimal point it is necessary to provide it with a drive signal of the same frequency as, but 180° out of phase with, the backplane output. For driving a single, fixed decimal point, the simple inverter circuit of Fig. 11a can be used.

If more than one decimal point is to be selected then it is necessary for the unused decimal points to be switched off by arranging their drive waveforms to be in phase with the backplane output. This is simply achieved using exclusive OR gates as shown in Fig. 11b.

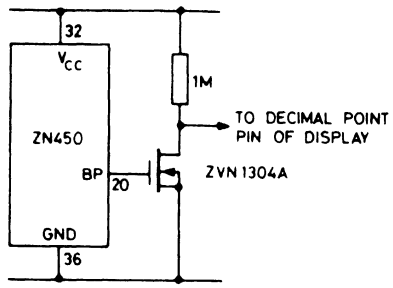
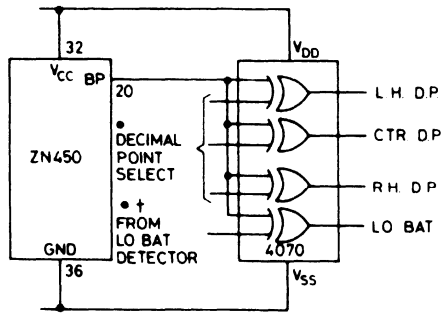


Fig. 11a Driving a fixed decimal point



*Logic 1 = ON
Logic 0 = OFF
†See also figure 6

Fig. 11b Decimal point select and 'lo bat' indicator drive using exclusive OR gates

A logic '1' on the input causes the output waveform to be out of phase with the backplane and the appropriate decimal point is activated. Conversely a logic '0' causes the output to be in phase with the backplane. A single 4070 CMOS quad-EXOR gate I.C. will provide the drive for the three decimal points of a 3½ digit liquid crystal display plus the drive to a low battery indicator. A suitable low battery detection circuit is shown in Fig. 6d.

EXTERNAL COMPONENTS

A basic 200mV DVM can be built using only ten external passive components, as shown in Fig. 12. In addition to these components it is good practice to include input protection resistors to limit the maximum input current to 50mA in the event of an input overload. The resistance and power rating of these components depends on the maximum voltage against which the inputs are to be protected.

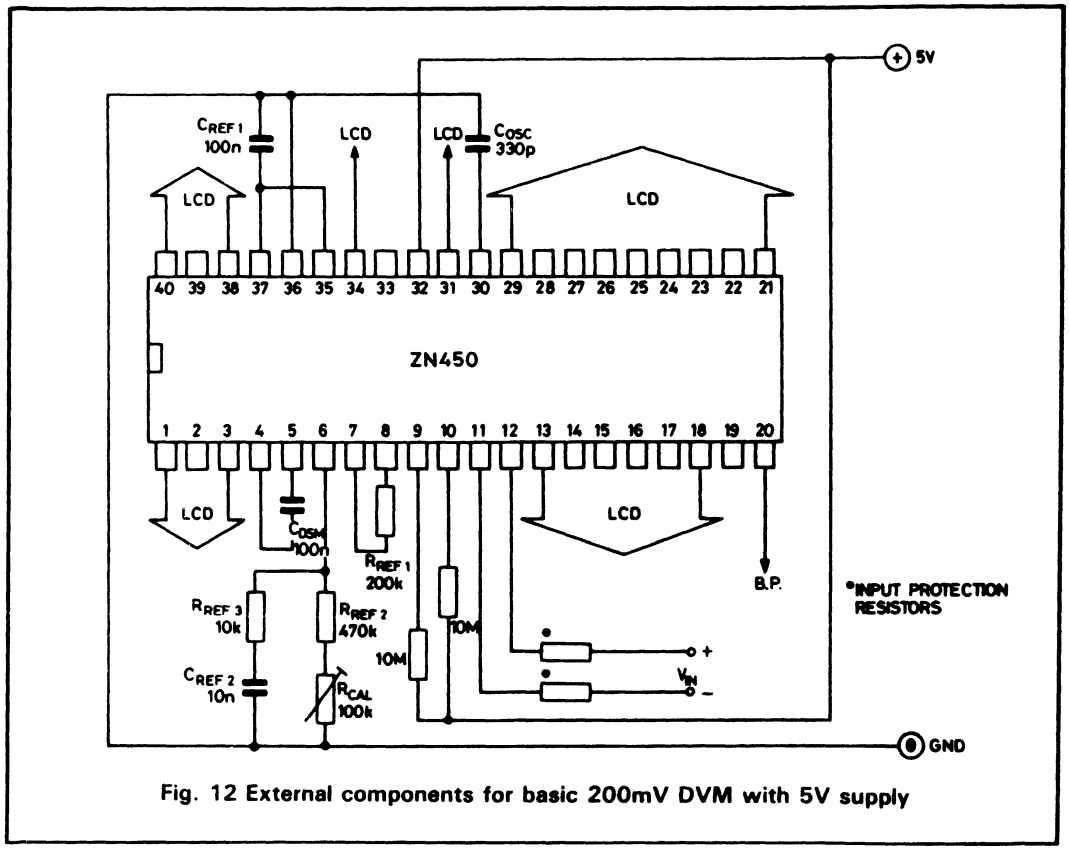


Fig. 12 External components for basic 200mV DVM with 5V supply

SIGNAL CONDITIONING

The ZN450 can be used with a wide variety of signal conditioning circuits and transducers to provide a digital dispay of any parameter that can be converted into a suitable d.c. voltage.

VOLTAGE MEASUREMENT

The most obvious signal conditioning circuit is a switched input attenuator which will allow d.c. voltages greater than 200mV to be measured. To minimise time-consuming calibration procedures it should be possible to calibrate the DVM on only one range to rely on the precision of the attenuator resistors to give accurate results on other ranges.

However, since the input resistance of the ZN450 is about 10MΩ its loading effect on the attenuator cannot be ignored. Fortunately this effect can be eliminated by designing an attenuator with a constant output resistance so that the ZN450 sees the attenuator as a 199.9mV (full-scale) source with a constant source resistance on all ranges.

Three suitable types of attenuator circuit are shown in Fig. 13, a ladder attenuator and two types of T attenuator. The ladder attenuator has the advantage that the input resistance is fairly constant and only 3 resistor values are required, but the switching is somewhat complicated.

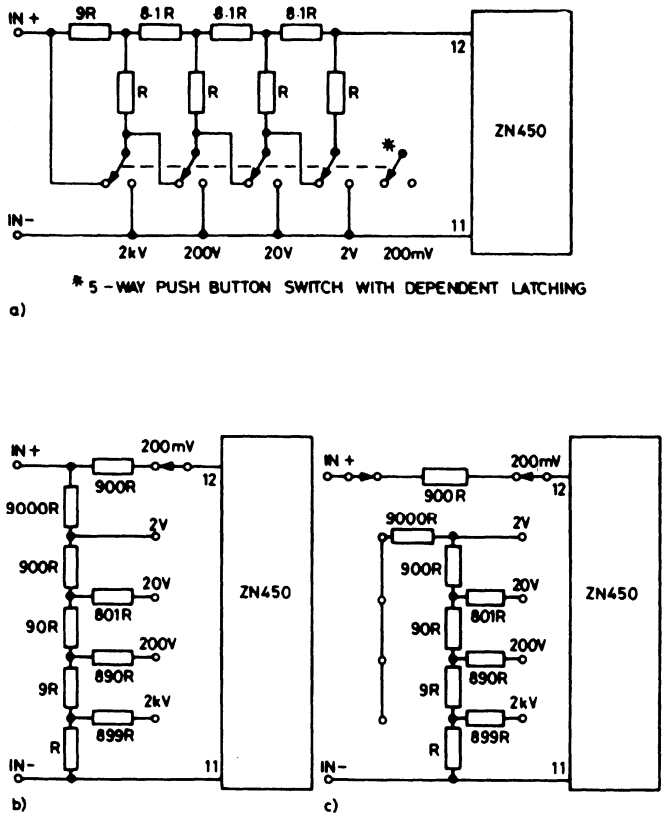


Fig. 13 Attenuators for multirange voltmeter

The T attenuator of Fig. 13b has the advantage of simplicity, using only a single-pole switch, but the resistor values are slightly odd. Furthermore the input resistance drops to about 5MΩ on the 200mV range since the attenuator appears in parallel with the ZN450s input resistance. This problem can be overcome by using a two-pole switch so that the attenuator is disconnected on the 200mV range as shown in Fig. 13c.

When designing signal conditioning circuits for use with the ZN450 care must be taken to ensure that the input offset current does not cause errors. The offset current generates an error voltage $I_{OS} \times R_O$ where R_O is the output resistance of the attenuator. There are two components in the offset current; that due to the ZN450 itself, typically, 100pA, and a component due to the mismatch of the 10MΩ input resistors, typically 150pA per kΩ mismatch. The offset current can be minimised by using well matched 10MΩ resistors, or can be nulled out entirely using the circuit of Fig. 14.

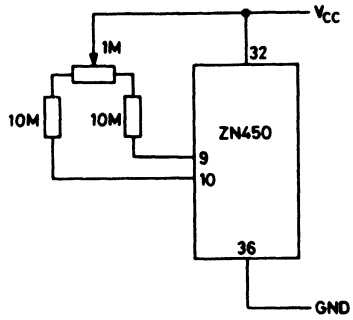


Fig. 14 Offset current nulling circuit

CURRENT MEASUREMENT

Measurement of d.c. current is also very simple. The current to be measured is allowed to flow through a shunt resistor connected across the input terminals of the ZN450, the voltage measured being equal to the product of the current and the shunt resistors.

Currents as low as 20μA full-scale can be measured before the input resistance and offset current of the ZN450 become significant.

For multi-range current measurement the preferred circuit is the so-called universal shunt, an example of which is show in Fig. 15.

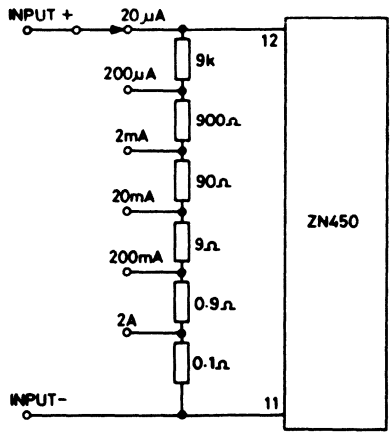


Fig. 15 Multirange ammeter circuit using universal shunt

Although the full-scale voltage drop of this circuit is 200mV it is perfectly feasible to design an ammeter with a smaller voltage drop by increasing the sensitivity of the ZN450. This has two advantages. Firstly, the voltage loss in the ammeter is reduced, which can be useful when making measurements in low-voltage circuits. Secondly, the power dissipation in the shunt resistors is reduced.

Example:

Measuring 20A full-scale with a 200mV voltage drop the required shunt resistor will be $\frac{0.2}{20} = 10\text{M}\Omega$ and the full-scale power dissipation will be 4 watts. With a 20mV drop the required resistor will be 1MΩ and the power dissipation 400mW.

TRANSDUCER BRIDGE CIRCUITS

The high sensitivity and true differential inputs of the ZN450 make it ideal for use with transducers, particularly those which function best in a bridge configuration. The regulated 5V supply can also provide a stable excitation voltage for passive transducers such as semiconductor pressure gauges, platinum resistance thermometers and semiconductor temperature sensors.

Fig. 16 shows a thermometer circuit using a silicon diode as the temperature sensor. The forward voltage drop has a temperature coefficient of approximately −2mV/°C when the device is run at a constant current. In the bridge circuit shown this gives an increase of about 1.28mV/°C at the +ve input of the ZN450. The full-scale reading of the ZN450 is set to about 256mV so that one digit corresponds to 0.1°C and the full-scale reading is 199.9°C.

The bridge configuration allows the forward voltage drop of the diode to be nulled out using P1 to give a reading of 000.0 at 0°C, whilst P2 adjusts the full-scale range of the ZN450 to read 100.0 at 100°C.

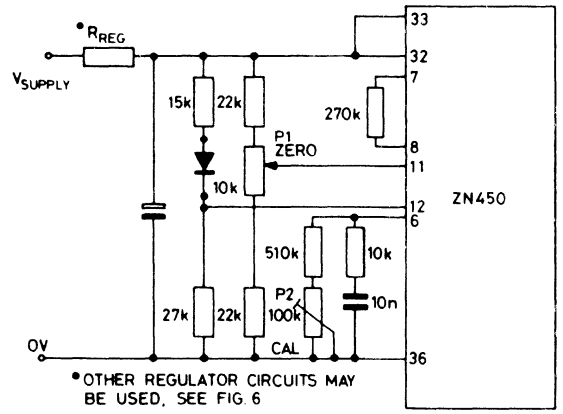


Fig. 16 Digital thermometer circuit

COMMON-MODE PERFORMANCE

The ZN450 has true differential inputs with a common-mode range of 1.8-3.8 volts and good common-mode rejection. However, if the full potential of the differential inputs is to be realised then care must be taken when designing with the ZN450.

When open-circuit, the inputs of the ZN450 are biased at about 2.8 volts above supply common. If a common-mode voltage other than this is applied to the inputs then care must be taken to ensure that any impedances between the inputs and the common-mode voltage (attenuators, series resistors, etc.) are the same for each input, otherwise the common-mode rejection will be impaired. This is illustrated in Fig. 17. Balancing the input impedances of differential inputs to ensure good common-mode rejection is, of course, normal practice.

This is generally a problem only in systems where the voltage to be measured is referenced to the ZN450's supply ground. In battery-powered applications no common-mode voltage exists between the measured voltage and the inputs, since the supply voltage of the ZN450 is floating. However, care must be taken in battery-powered systems to ensure good a.c. rejection.

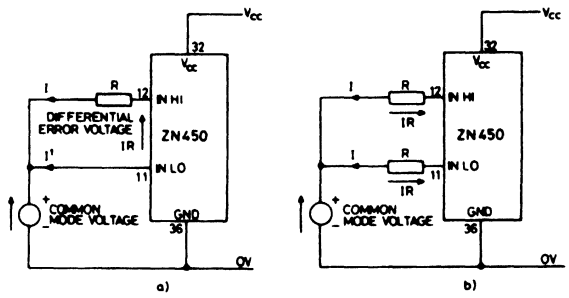


Fig. 17 – (a) Unbalanced input resistances impair common-mode rejection

(b) With balanced input resistances common-mode voltage does not cause differential error voltage

If the voltage being measured has a large a.c. common-mode signal superimposed upon it then the supply voltage of the ZN450 will normally float up and down with the a.c. component, thus keeping the inputs of the ZN450 within their common-mode range. However, the resistance between the a.c. signal at the inputs and the ZN450 supply rails is the 5MΩ common-mode resistance of the ZN450 inputs. If significant stray capacitance exists between the ZN450 supplies and ground (for example if the battery is close to an earthed metal surface) then this can form a low pass filter with the common-mode input resistance with the result that the ZN450 supply rails do not follow the a.c. common-mode voltage at the inputs. This is shown in Fig. 18.

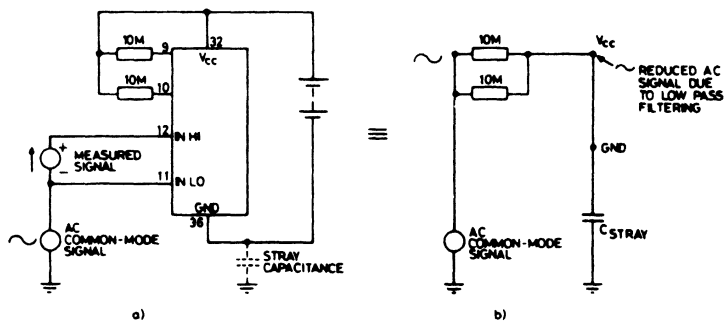


Fig. 18 – (a) Battery-powered ZN450 connected to signal with large A.C. common-mode signal (Supply regulator not shown)

(b) Equivalent A.C. circuit

The problem can be overcome in one of two ways. The simpler method, shown in Fig. 19 a), is to connect a capacitor between input low and supply ground. This provides a low impedance a.c. path between these two points so that the supply rails will track the a.c. common-mode voltage.

The value of this capacitor should be several times greater than the maximum stray capacitance. On the other hand, at switch-on it must charge up via the 10M input resistance of the ZN450, so it should not be too large. A value of 22n is about the optimum.

An alternative solution is to mount the DVM in a screened enclosure, the screening being connected to input LO. This has the effect of producing a stray capacitance between the ZN450 supply rails and screen. However, since the screen is not at a fixed potential, but follows the common-mode signal, the effect of this capacitance is bootstrapped out.

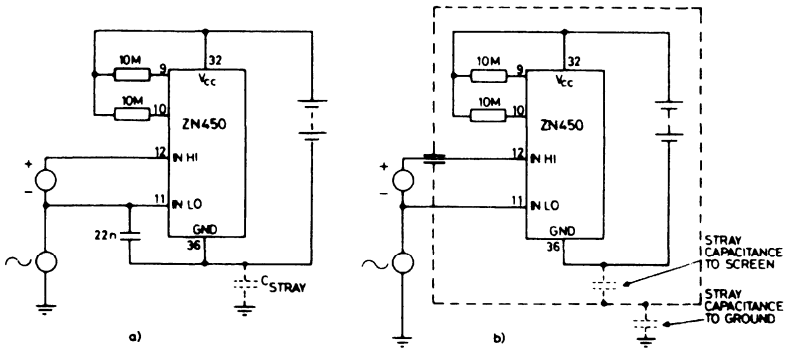


Fig. 19 Two methods of ensuring A.C. rejection in battery-powered circuits

A.C. MEASUREMENTS

To measure a.c. voltage or current it is first necessary to convert it into proportional d.c. voltage. The simplest way to do this is to interpose a precision active rectifier circuit between the attenuator or shunt and the inputs of the ZN450. Such a circuit produces d.c. voltage proportional to the mean of the rectified voltage rather than a true R.M.S. result and for true R.M.S. measurements an R.M.S. converter must be used. The rectifier can be calibrated to read R.M.S. but the result is true only if the input signals have a constant form factor.

A simple precision rectifier is shown in Fig. 20. It is completely a.c. coupled throughout by C2, C3 and C4, so the offset voltage of A1 does not appear at the output and no zero adjustment is required. To prevent the offset voltage of A1 causing it to saturate in the absence of an input signal, 100% d.c. feedback is provided by R3. R1 and R2 provide a d.c. bias path for the non-inverting input of A1, whilst C2 provides bootstrapping to increase the a.c. input impedance.

Amplifier A2 is a voltage follower biased into the middle of the ZN450's common-mode range to provide a low impedance analogue common point. The output of the rectifier is connected to a lowpass filter comprising R6 and C5. So that both inputs of the ZN450 see the same d.c. resistance R6 is placed in series with the input LO terminal and is made equal to R4 + R5. This in no way affects the performance of the filter. With the component values shown the circuit is calibrated to read R.M.S. for sinewave inputs, so the use of this type of waveform will be assumed throughout.

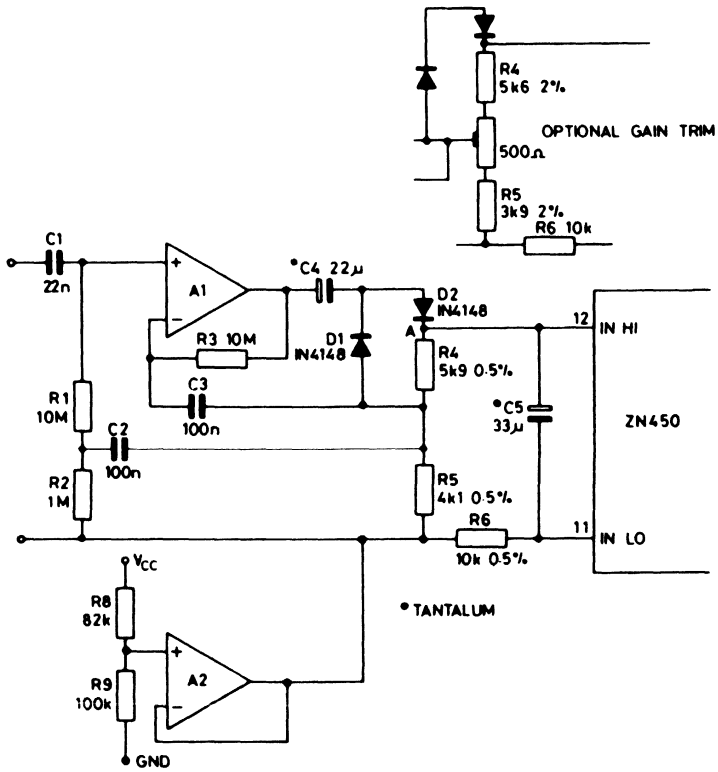


Fig. 20 Precision rectifier for A.C. measurements

The circuit functions as follows: when the input signal crosses zero in a positive going direction the output of A1 slews positive until D2 conducts after which the voltage at point A is defined by the equation:

$$V_A = G \times V_{IN}, \text{ where } G = \frac{R_4 + R_5}{R5}$$

and since $R_6 = R_4 + R_5$

$$G = \frac{R_6}{R_6 - R_4}$$

and $$R_4 = R_6\frac{(G-1)}{G}$$

This voltage tends to charge up C_5 in a positive direction via R_6. When the signal crosses zero in a negative going direction the output of A1 slews negative until D1 conducts, after which the output voltage at point B is equal to (minus) V_{IN}. This voltage tends to charge up C_5 in a negative direction via R_6 and R_4. Now, assuming the time constant R_6/C_5 is long compared to the period of the input waveform, the voltage on C_5 will eventually reach equilibrium. When this is the case the mean current flowing into C_5 during the positive half cycle must equal that flowing out of C_5 during the negative half cycle.

i.e. $$\frac{V_{A(MEAN)} - V_C}{R_6} = \frac{-V_{B(MEAN)} + V_C}{R_6 + R_4}$$

Now the mean value of a rectified sinewave signal is 0.9 times the R.M.S. value therefore

$V_{A(MEAN)} = 0.9G.\ V_{IN(RMS)}$

and $V_{B(MEAN)} = -0.9V_{IN(RMS)}$

In order for the ZN450 to read correctly V_C must equal V_{RMS} therefore

$V_A = 0.9G.V_C$

and $V_B = -0.9V_C$

therefore $\frac{V_C(0.9G-1)}{R_6} = \frac{1.9V_C}{R_6+R_4}$

substituting for R_4 and eliminating V_C

$$\frac{0.9G-1}{R_6} = \frac{1.9}{R_6 + R_6\frac{(G-1)}{G}}$$

eliminate R_6 $\quad 0.9G-1 = \frac{1.9G}{2G-1}$

$$(0.9G-1)(2G-1) = 1.9G$$

$$1.8G^2 - 4.8G + 1 = 0$$

Solving the above quadratic equation gives

$G = 2.439$

or $R_4 = 0.59R_6$

$$R_5 = \frac{R_6}{2.439}$$

These equations allow the values of R_4 and R_5 to be calculated for any value of filter resistor R_6. With the values shown the circuit is accurate to about $\pm 1.5\%$ over the frequency range 40Hz to 1kHz.

PLESSEY
Semiconductors

ZN451

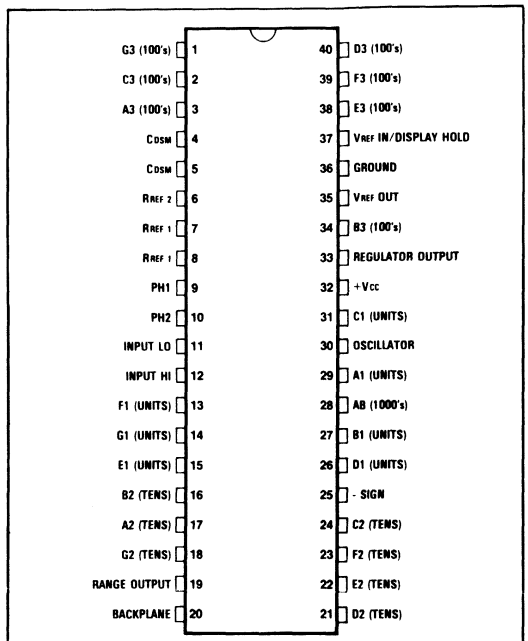
3½ DIGIT DVM IC WITH EXTERNAL AUTO-ZERO

The ZN451 is a complete digital voltmeter fabricated on a monolithic chip. A novel charge-balancing conversion technique ensures good linearity. The auto-zero function is completely digital in operation, thus obviating the need for a capacitor to store the error voltage. Output signals are provided to control external auto-zero switches so that op-amps or other signal conditioning circuits can be included in the auto-zero loop to boost input impedance and/or improve sensitivity to as low as 1.999mV full-scale.

This versatile IC can be used as the basis not only for digital voltmeters and multimeters but also in other instruments such as thermometers and pressure gauges where its sensitivity allows interfacing to low output transducers such as thermocouples and strain gauges.

FEATURES

- External Circuits may be included in the Auto-Zero Loop
- Full-Scale Reading 1.999mV or Lower
- Measures Sum or Difference of Two Inputs
- Digital Auto-Zero with Guaranteed Zero Reading for 0V Input
- True Polarity at Zero for Null Detection
- True Differential Inputs
- Direct Drive of Liquid Crystal Display
- On-Chip Clock and Precision Reference
- Underrange/Overrange Indication
- Low Power Consumption, less than 35mW
- Wide Supply Voltage Range, Single Supply Rail



Pin connections - top view

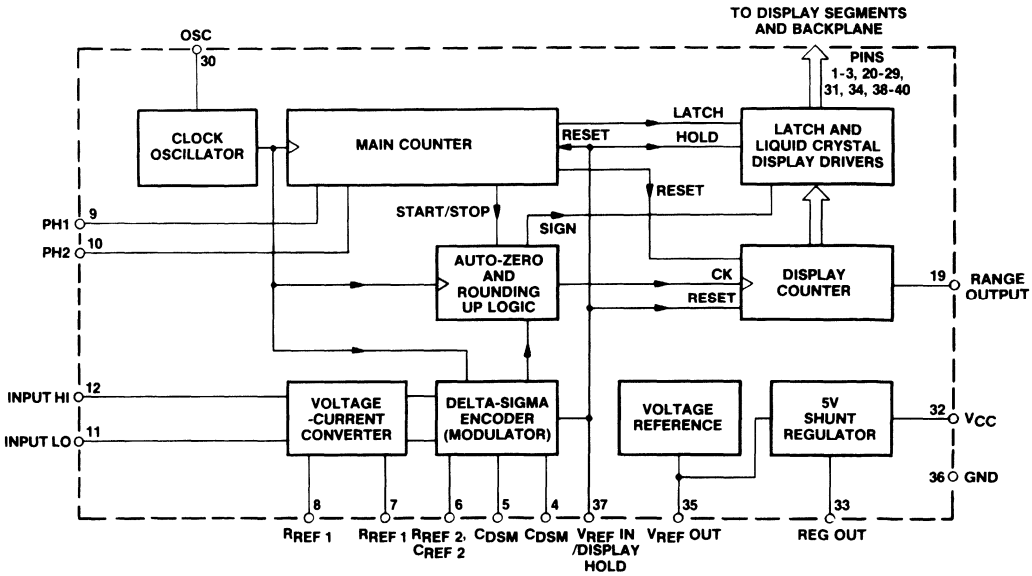


Fig.1 ZN451 System diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	-0.5 to +7.0V
Max. voltage, all other inputs	-0.5 to (V_{CC} +0.5)V
Operating temperature range	0°C to 70°C
Storage temperature range	-55°C to +125°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5V, T_{amb} = +25°C unless otherwise specified)

Parameter	Min.	Typ.	Max.	Unit	Conditions
Full-scale reading	-1999	–	+1999		
Zero reading	-000.0	±000.0	+000.0	digital reading	V_{IN} = 0, V_{FS} = 200mV
Rollover error	-2	0	+2	count	$-V_{IN}$ = $+V_{IN}$ = ±200mV conversion time ≥ 0.5 sec.
Linearity	-1	0	+1	count	V_{FS} = 200mV conversion time ≥ 0.5 sec.
Common mode range	1.8	–	3.8	V	
Common mode rejection	–	120	–	μV/V	
Supply rejection	–	100	–	μV/V	
Input offset current	–	0.1	1	nA	
Input resistance	–	20	–	MΩ	
Zero temperature coefficient	–	–	1	μV/°C	
Full-scale temperature coefficient	Determined by tracking of external resistors				Ref. T.C. = 0ppm/°C
Oscillator frequency range	–	–	300	kHz	
Conversion time (48000 oscillator periods)	0.25	–	–	seconds	
Voltage reference					
Output voltage	1.26	1.3	1.35	V	
Temperature coefficient	–	±50	±80	ppm/°C	
Knee current	–	–	150	μA	
Maximum sink current	1	2	–	mA	
Supply voltage					
(a) Direct	4.5	5	5.5	V	
(b) Using on-chip shunt regulator	6.0	–	–	V	
(c) Using external NPN transistor	6.5	–	–	V	
(d) Using two transistor regulator	5.5	–	–	V	
Supply current	–	4	6.5	mA	
Shunt regulator					
Output voltage	4.5	5	5.5	V	
Sink current	–	–	15	mA	
Display outputs					
Peak voltage	–	$\pm V_{CC}$	–		
D.C. component	–	–	±25	mV	
Backplane frequency	–	$\frac{1}{2000}$	–	oscillator frequency	

GENERAL DESCRIPTION

The ZN451 utilises a charge-balancing conversion principle, which offers a number of advantages over the more common dual-slope integration method.

These include a fixed conversion time which is independent of the analogue input voltage, completely digital auto-zero and inherently bipolar operation. Linearity is also extremely good over the entire input voltage range, unlike some dual-slope designs where stray capacitance can cause problems around zero.

The auto-zero loop of the ZN451 is external to the device so that op-amps and other signal-conditioning circuits can be included within it and thus have their zero errors removed.

The conversion time of the ZN451 is divided into two periods, Phase 1 and Phase 2, unlike the dual-slope system which has three distinct phases, signal integrate, reference integration and auto-zero.

The heart of the ZN451 is the delta-sigma encoder, a simplified circuit of which is shown in Fig. 2.

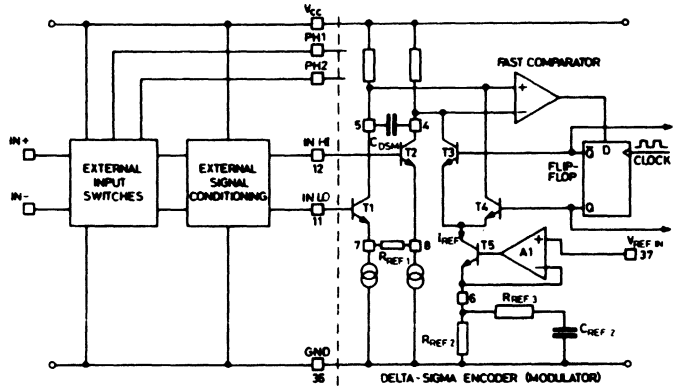


Fig. 2 Simplified circuit of the delta-sigma encoder

The delta-sigma encoder of the ZN451 consists of a voltage-current converter comprising T_1 and T_2, a reference generator A_1/T_5 and a feed-back loop containing a fast comparator, D-type flip-flop and current switches T_3 and T_4. These can switch a current $I_{REF} = \frac{V_{REF}}{R_{REF2}}$ into the collector circuit of either T_1 or T_2, depending on the state of the flip-flop.

The polarity of the voltage across capacitor C_{DSM} is monitored by the comparator, whose output is sampled on every clock pulse by the flip-flop. The outputs of the flip-flop switch I_{REF} into the collector circuit of either T_1 or T_2 so as to oppose the existing voltage on C_{DSM} i.e. to maintain the average charge acquired by C_{DSM} at zero, thus keeping the circuit in equilibrium.

Assuming perfect symmetry in the circuit, with zero volts applied between the bases of T_1 and T_2 their collector currents will be equal, and the only charge acquired by C_{DSM} will be that put on it by I_{REF}. The flip-flop will thus change state on every clock pulse so that C_{DSM} will alternately acquire charge quanta of $+I_{REF}T_C$ and $-I_{REF}T_C$ (where T_C is the clock period) and the nett charge acquired will be zero. The output of the flip-flop will thus be a square-wave with a 50% duty cycle.

During the measurement the voltage to be measured is applied between the bases of T_1 and T_2 and is converted into a current $I_{IN} = \frac{V_{IN}}{R_{REF1}}$ flowing in R_{REF1}. This produces a different current $2I_{IN}$ in the collector currents of T_1 and T_2, so that the charge acquired by C_{DSM} is no longer equal and opposite ($\pm I_{REF}$) but is now $(I_{REF} - 2I_{IN})\ T_C$ when T_4 is turned on and $(-I_{REF} - 2I_{IN})\ T_C$ when T_3 is turned on.

In order to maintain equilibrium the flip-flop will now no longer change state on every clock pulse but will remain in one state for a longer period than it remains in the opposite state. i.e. $N_1 T_C(I_{REF} - 2I_{IN}) + (N - N_1)T_C(-I_{REF} - 2I_{IN}) = 0$ where N_1 is the number of clock pulses for which the flip-flop Q output is a '1' and N is the total number of clock pulses over which the measurement is made and assuming N is so large that quantising error can be ignored.

Thus $N_1(I_{REF} - 2I_{IN}) = (N - N_1)(I_{REF} + 2I_{IN})$

And

$$\frac{2N_1 - N}{N} = \frac{2I_{IN}}{I_{REF}} \text{ i.e. } N_1 - \frac{N}{2} = \frac{NI_{IN}}{I_{REF}} = \frac{NV_{IN}R_{REF2}}{R_{REF1}V_{REF}}$$

In other words, if a counter is allowed to count N_1 and $\frac{N}{2}$ is subtracted from it (by initially presetting the counter to $-\frac{N}{2}$ then the result is directly proportional to V_{IN}, assuming N, V_{REF1} and R_{REF2} are fixed. With zero input voltage the DSM duty-cycle should be 50%, N_1 should equal $\frac{N}{2}$ and the accumulated count should be zero. In practice, of course, this will not be the case due to offsets and component mismatching in the DSM. Fortunately, an interesting property of the DSM allows the zero error to be removed digitally.

If the DSM output is taken from the $\overline{Q}$ output of the flip-flop instead of the Q output then the number of pulses counted over a period of N clock pulses will be not N_1 but $N\text{-}N_1$. Thus, if the counter is preset to $-N$ instead of $-\frac{N}{2}$ the number accumulated in the counter after N clock pulses will be $-N_1$. In other words, taking the $\overline{Q}$ output of the DSM and presetting the counter to $-N$ gives a result proportional to minus the input voltage. This is what occurs during phase 1.

Clearly, if the input voltage is the same during phase 1 and phase 2 the counter will accumulate a count of $-N_1$ during phase 1 and add a further N_1 pulses during phase 2, giving a total count of zero. If the input voltage is zero during both phases the system will measure minus the zero error during phase 1 and plus the zero error during phase 2, thus giving an automatic zero reading.

Obviously when measuring an actual input voltage the DSM must not see the same voltage during both phases, otherwise a zero reading will always result whatever the input. The input voltage must thus be switched, and this can be achieved in two ways. Most obvious is to disconnect the input voltage during phase 1 and connect it during phase 2, so that the result is proportional to $-V_{OS} + (V_{OS} + V_{IN}) = V_{IN}$. Alternatively the polarity of the input voltage can be reversed during phase 1 so that the result is proportional to $-(V_{OS} - V_{IN}) + (V_{OS} + V_{IN}) = 2V_{IN}$. This of course means that the component values must be calculated for twice the required full-scale reading, i.e. for 200mV full-scale the components would be calculated for 400mV. This can be achieved simply by doubling the value R_{REF1}.

The second method has advantages where a large input overload margin is required before the DSM saturates. This occurs when its duty-cycle is 0% or 100%, i.e. when $I_{IN} = \pm\frac{I_{REF}}{2}$ and N_1 = zero or N. (N = 5000 in the ZN451).

Overrange occurs at a reading of ± 2000. The duty-cycle of the DSM at this point depends on the input switching method used.

Whatever method is used, with zero input voltage the counter will count 2500 clock pulses during phase 1 and 2500 during phase 2 to give a reading of zero (assuming negligible zero-error). Using the first input switching method the signal is measured only during phase 2, so an additional 2000 clock pulses must be counted during phase 2, i.e. a total of 4500 clock pulses must be counted during phase 2.

Substituting in $I_{IN} = (N_1 - \frac{N}{2})I_{REF}$ to find the required value of I_{IN} for overrange $I_{IN} = 0.4 \times I_{REF}$FS.

The overload margin before the DSM saturates is thus $\frac{1}{10}I_{REF}$ or 25% of full-scale.

Using the second input switching method the input signal is measured during both phases, so for a full-scale reading an additional 1000 clock pulses will be counted due to the input voltage in each phase, giving a clock total of 3500 clock pulses in each phase.

Therefore substituting $I_{IN} = (N_1 - \frac{N}{2})I_{REF}$ to find the required I_{IN} for overrange.

$I_{IN} = 0.2\ I_{REF}$.

The overload margin before the DSM saturates is thus $0.3\ I_{REF}$ or 150% of full-scale. i.e. input switching method (b) gives six times the overload margin of method (a).

Input switching method (b) has several other interesting properties, some of which can usefully be exploited.

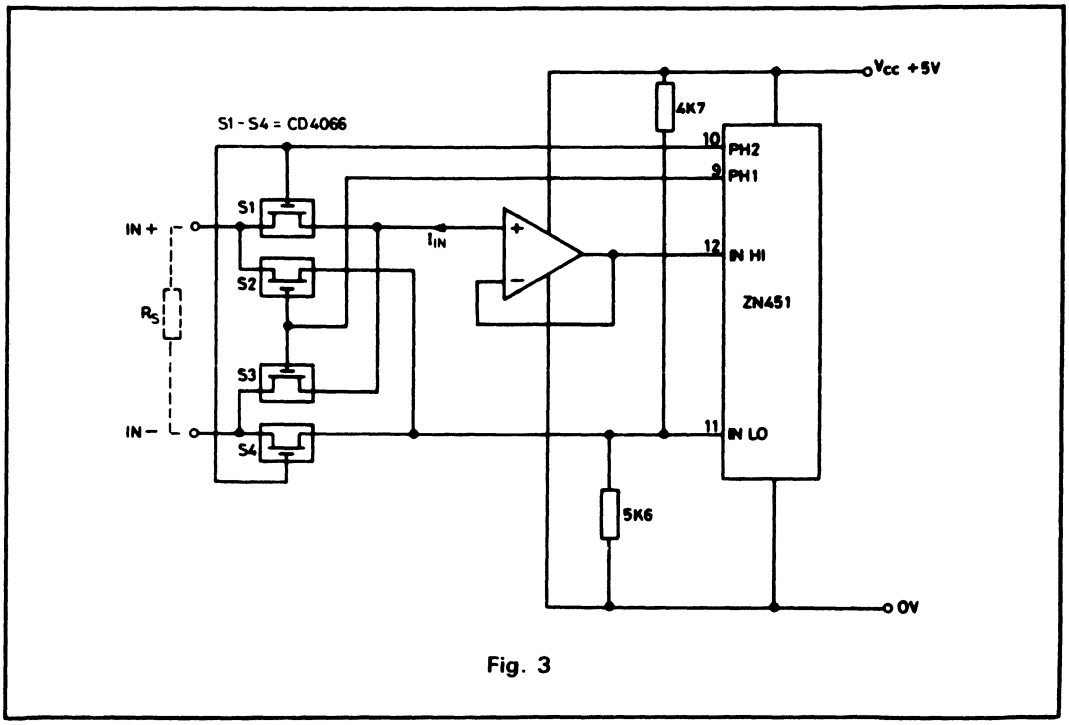


Fig. 3

Fig. 3 shows the simplest possible configuration using an op-amp as a voltage follower to boost the input resistance. Suppose this is a J-FET op-amp with an input current of around 100pA. Suppose a 10M resistor is connected between input + and input –. The input current of the op-amp will generate a voltage of 1mV across this resistor. However, this will not cause a zero error since the direction of current flow, and hence the polarity of the voltage, is the same during phase 1 and phase 2.

Therefore, using switching method (b), high resistance sources will not cause zero errors, subject to the proviso that the error voltage does not cause saturation of the DSM.

The two measurement phases of the ZN451 can also be used to perform other functions. By re-configuring the input switches to measure one input voltage during phase 1 and a second input voltage during phase 2 it is possible to measure the sum or difference of the two voltages, depending on their relative polarity. This is shown in Fig. 4.

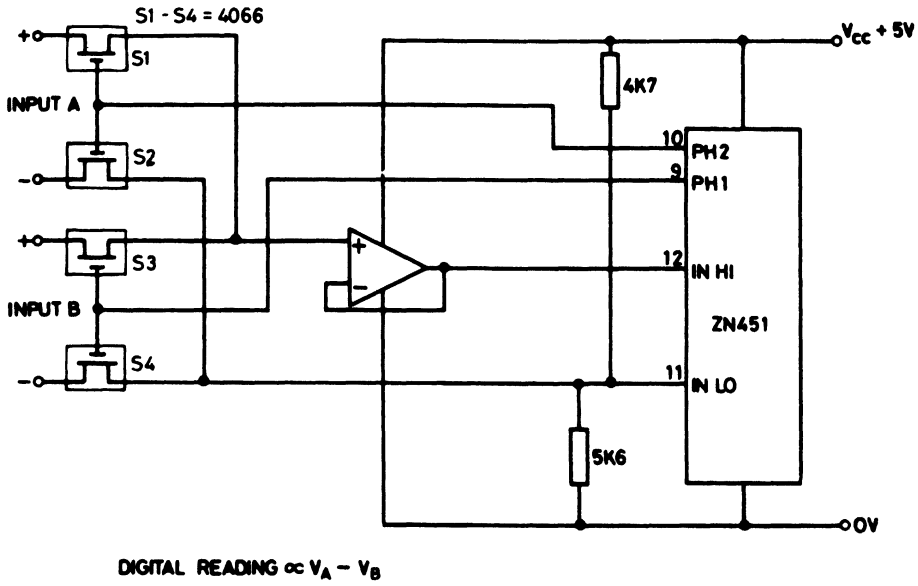


Fig. 4

TIMING DIAGRAM

The value of N chosen for the ZN451 is 5000, so each phase of the measurement should take 5000 clock pulses, a total of 10,000 for the whole measurement. However, the display counter of the ZN451 is preceded by a divide-by-four counter which performs several functions.

Firstly it provides two guard bits so that quantising errors between phase 1 and phase 2 measurements do not give rise to spurious zero errors of ± 1, but are confined to the (non-displayed) guard bits.

Secondly, it provides information to the polarity and rounding up logic, which drives the – sign. The divide-by-four stage means that the display counter sees only one-quarter of the pulses from the DSM and each phase must thus run for 20,000 clock pulses. Furthermore, each measurement phase is separated by a pause of 4000 clock periods to allow the input switches to settle. One measurement cycle thus takes a total of 48,000 clock periods.

Fig. 5 is a timing diagram of the ZN451 which clearly shows the two measurement phases and the operation of the DSM. Two control signals PH_1 and PH_2 indicate which measurement phase is active. These outputs are CMOS compatible and can be used directly to drive input switches such as the 4066.

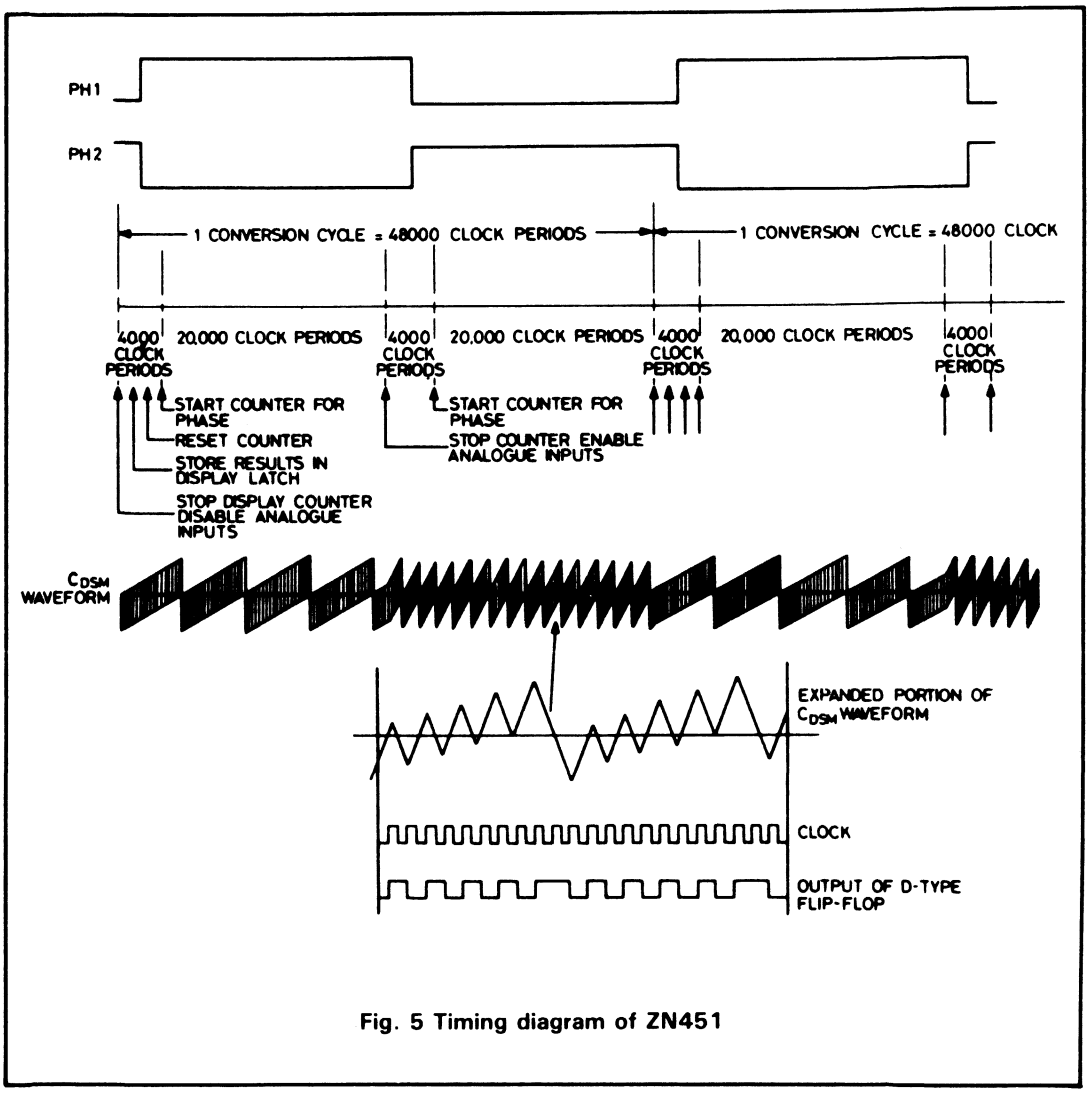


Fig. 5 Timing diagram of ZN451

REFERENCE LOOP AND SUPPLY REGULATOR

The reference current defining loop is shown in more detail in Fig. 6.

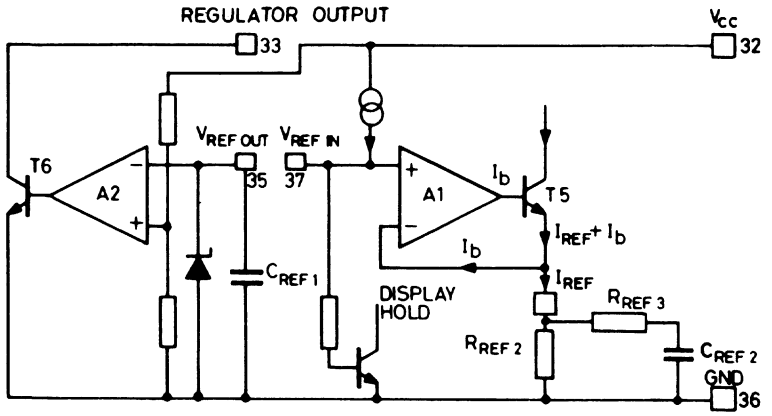


Fig. 6 Reference current loop and supply regulator

A reference input voltage applied to the non-inverting input of A_1 causes the output of A_1 to bias T_5 such that the inverting input of A_1 assumes the same potential and a current $\frac{V_{REF\ IN}}{R_{REF2}}$ flows in R_{REF2}. By making the input bias current of A_1 the same as the base current of T_5 this base current flows into the inverting input of A_1 instead of through R_{REF2}. The reference current flowing in the collector of T_5 is therefore almost identical to the current flowing in R_{REF2}. The reference loop is stabilised by C_{REF2} and R_{REF3}.

A highly stable on-chip bandgap reference of approximately 1.28V is provided and this may be used by linking $V_{REF\ OUT}$ to $V_{REF\ IN}$ when the reference will be biased on by the 150μA current source connected to the non-inverting input of A_1. The on-chip reference is stabilised by C_{REF1}. The on-chip reference also provides the reference voltage for the on-chip supply regulator A_2. This compares V_{REF} against $\frac{V_{CC}}{4}$ and controls V_{CC} with transistor T_6 such that the two are kept equal, i.e. $V_{CC}=5V$. The supply regulator can be configured as a shunt or series regulator using only a few external components. If $V_{REF\ OUT}$ is not connected to $V_{REF\ IN}$ but supply regulation is still required then the on-chip reference must be biased on by a 22k resistor to V_{CC}.

SUPPLY VOLTAGE OPTIONS

The ZN451 is designed to be extremely flexible with regard to supply voltage and four power supply options are possible allowing operation over a wide range of supply voltages. These options are illustrated in Fig. 7.

The first option is to ignore the on-chip regulator and to connect an externally stabilised voltage of 4.5 to 5.5V direct to pin 32, for example a 5V logic supply.

For supply voltages greater than 6V the on-chip shunt regulator (pin 33) may be used by linking pins 32 and 33. When using the shunt regulator an external resistor must be placed in series with the supply to limit the regulator current as shown in Fig. 7b. The value of this resistor is given by:

$$R=\frac{V_{supply}-5\ \text{volts}}{6.5}\quad\left(k\Omega=\frac{V}{mA}\right)$$

which allows for the maximum 6.5mA current consumption of the I.C.

If the supply voltage is unstabilised then R should be calculated using the minimum supply voltage that will be encountered. The current drawn by this configuration increases with supply voltage as the shunt regulator sinks more current in order to maintain V_{CC} at 5V. The maximum allowable supply voltage is thus determined by the 15mA maximum rating of the shunt regulator, assuming very little current is drawn by the DVM circuitry, i.e.

$$V_{max} = 15(mA) \times R(k\Omega) + 5 \text{ volts}$$

$$= (3V_{min} - 10) \text{ volts}$$

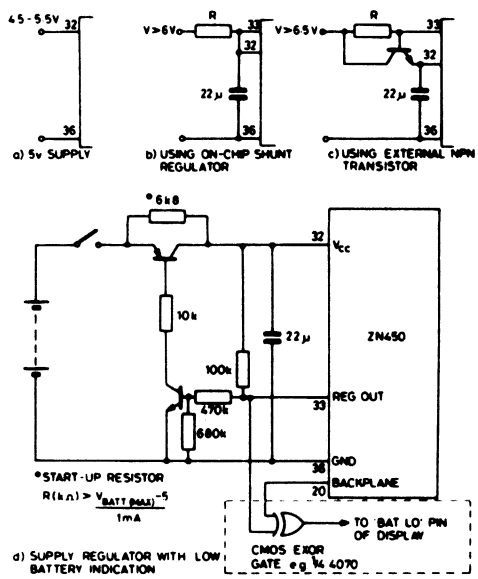


Fig. 7 Supply voltage options

Since the current drawn by the shunt regulator increases with supply voltage this configuration is not recommended for battery operation where long battery life is a prime criterion, as the current drawn from a new battery could be up to 2.3 times the maximum current consumption of the DVM.

For battery operation a series regulator circuit is recommended which can be constructed using one or two external transistors controlled by pin 33. The simplest series regulator, shown in Fig. 7c, uses a single NPN transistor and allows operation down to about 6.5V. Current consumption of this circuit is the normal current consumption of the DVM plus the base current of the transistor.

The base resistor must be chosen such that it can supply sufficient base drive when the supply voltage is a mimimum assuming

(a) Maximum DVM current of 6.5mA

(b) Maximum shunt regulator voltage of 5.5V

(c) Minimum gain of the transistor

$$\text{Now base current } I_b \text{ (mA)} = \frac{V_{min} - V_{reg} - V_{beT1}}{R_b}$$

$$\text{required base current} = \frac{6.5\text{mA}}{h_{fe\ (min)}}$$

$$\text{Therefore } R_b(\text{k}\Omega) = \frac{(V_{min} - V_{reg} - V_{beT1}) \times h_{fe}}{6.5}$$

$$= \frac{(V_{min} - 6) \times h_{fe}}{6.5}$$

Example. The circuit is to operate down to 6.5V with a transistor type whose minimum gain is 80

$$R_b = \frac{(6.5 - 6) \times 80}{6.5}$$

$$= 6.1\text{k}$$

Nearest value of 5k6 is used.

Although a great improvement on the shunt regulator, the circuit of Fig. 7c still does not achieve maximum battery life since V_{min} must always exceed the regulator voltage by V_{beT1} plus the voltage drop across R_b.

For the ultimate in battery life the circuit of Fig. 7d is suggested. This allows operation down to voltages as low as $V_{reg} + V_{CE(sat)T1}$ and, as an added bonus, it automatically detects the end of useful battery life, i.e. the point at which the regulator ceases to funtion.

T_1 is a PNP series regulator transistor controlled by pin 33 via T_2, which provides the required signal inversion. During normal operation the voltage drop across R_1 is small since the base current required by T_2 is only a few hundred nanoamps, and the voltage at pin 33 is not much above the V_{be} of T_2 (about 0.6V).

When the battery voltage drops to $V_{reg} + V_{CE(sat)T1}$ the voltage at the non-inverting input of the regulator amplifier will fall below V_{REF} and the shunt regulator output transistor will turn off causing the voltage at pin 33 to rise to about 80% of supply.

Pin 33 can conveniently be connected to a low battery indicator consisting of a CMOS EXOR gate, as shown in the dotted box. When pin 33 is low the output of the EXOR gate will be in phase with the backplane and the LO BAT indicator will be extinguished. When pin 33 is high the output will be out of phase with the backplane and LO BAT will be visible.

OSCILLATOR OPTIONS

The on-chip oscillator of the ZN451 may be used with various configurations of external components, as show in Fig. 8. It will operate with only an external capacitor, which may be fixed, or variable to adjust the oscillator frequency. Alternatively the frequency may be adjusted by placing a variable resistor in series with the capacitor. Graphs of oscillator frequency versus capacitor and resistor values are given in Fig. 9. If absolute accuracy of the oscillator frequency is required then a crystal or ceramic resonator may be used as the frequency determining element. By making the integration time a whole number of mains cycles a degree of mains interference rejection can be provided. For example a 100kHz crystal gives an integration time of 200ms which is 10 cycles at 50Hz mains frequency or 12 cycles at 60Hz, the total measurement interval being 480ms or just over two conversions/second.

If mains interference is superimposed on the input signal it is important that its peak amplitude should not be large enough to cause saturation of the DSM. If this is not the case then the ZN451 should be preceded by a lowpass filter to give additional mains rejection.

The final option is to overdrive the oscillator input from a TTL or CMOS gate, as shown in Fig. 8d.

In order to maintain an adequate drive to the comparator the value of C_{DSM} must also be changed in proportion to the oscillator period. A table of suitable values is given below.

Oscillator frequency (kHz)	C_{DSM} Min.	C_{DSM} Max.
50	200n	2μ
100	100n	1μ
150	68n	680n

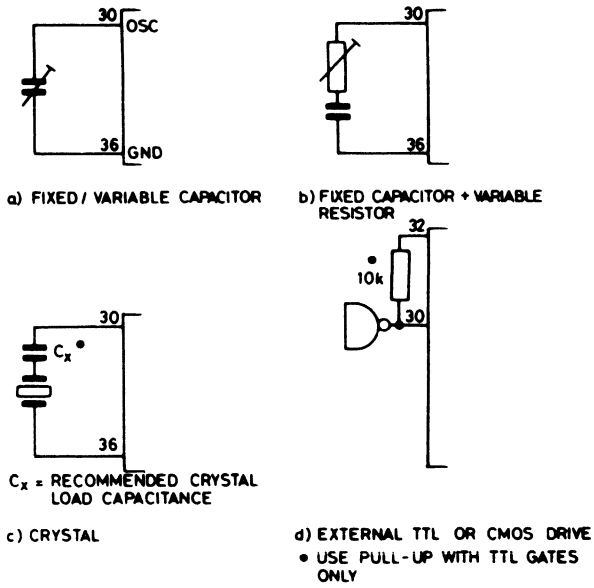


Fig. 8 Oscillator options

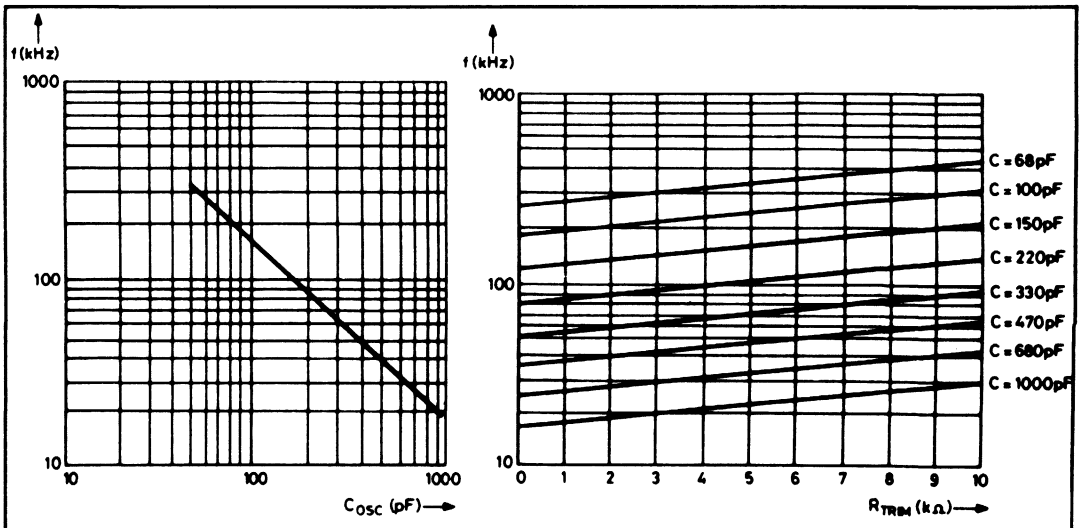


Fig. 9 Oscillator frequency v external capacitor and resistor

RANGE OUTPUT

To simplify the design of auto-ranging instruments, underrange and overrange detection circuits are provided in the ZN451. Overrange is indicated when the count exceeds 1999, whilst underrange is indicated for counts less than 150. This provides a degree of hysteresis to prevent the instrument jittering between ranges, which could occur if underrange was indicated at a count of 199 and there was a mismatch in the attenuators or other signal conditioning circuits.

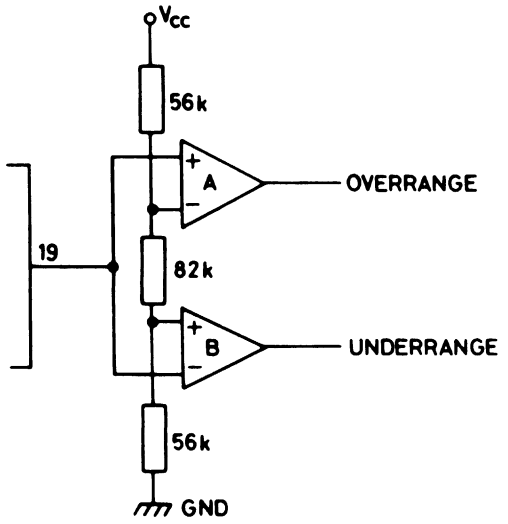
Because the pins of the ZN451 are fully utilised it is not possible to provide separate underrange and overrange pins, so a single three-state output is provided.

If the measurement is in range then pin 19 will be at $\frac{V_{CC}}{2} \pm 0.5V$ with a source resistance of approx. 40k.

For an overrange measurement pin 19 will go HIGH for 1000 clock pulses synchronous with the data store pulse at the end of the measurement. For an underrange measurement pin 19 will pulse LOW in a similar manner. In each case the output resistance is approx. 80k.

The range output can be fully decoded using a dual comparator, as shown in Fig. 10.

A visual overrange indication is also provided. In this condition the leading digit of the display shows a '1' whilst all other digits are blanked.



Range output	Output A	Output B
Underrange (GND)	0	⎍
In range (½ V_{CC})	0	0
Overrange (V_{CC})	⎍	0

Fig. 10 Decoding the range output

DISPLAY HOLD

The reference input, pin 37, also doubles as a display hold pin. If this pin is grounded then the display will continue to show the results of the last valid measurement until pin 37 is released. Display hold also resets the system counters and a new measurement begins immediately display hold is released. The method of activating display hold depends on whether or not the on-chip reference and shunt regulator are being utilised.

If an external reference voltage is used (pins 35 and 37 not joined) then display hold can be activated by grounding pin 37 with a single-pole switch, transistor or open-collector logic gate, provided that the external reference is not required to supply other circuits. If the on-chip regulator is to be used then pin 35 must, of course, be biased up with an external 22k resistor so that V_{REF} can supply the reference voltage for the regulator. If the on-chip reference is used but the on-chip regulator is not then display hold can be activated in a similar manner by grounding the junction of pin 35 and pin 37.

However, since the on-chip reference also provides the reference voltage for the on-chip regulator pin 35 must not be grounded if the regulator is in use or the supply voltage will drop to zero. If the on-chip reference and shunt regulator are both used then pin 37 must be disconnected from pin 35 before it is grounded to activate display hold. This is illustrated in Fig. 11. As pin 37 normally supplies the bias current for the on-chip reference this must be provided by an external 22k resistor when these pins are not linked.

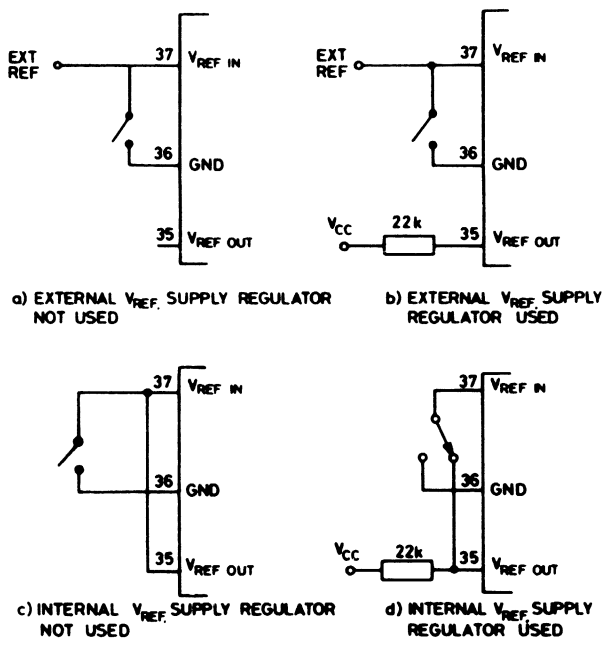


Fig. 11 Display hold options

BACKPLANE OUTPUT

The backplane output normally supplies a squarewave of the same frequency as, but 180° out of phase with, the active segment outputs. This provides the necessary a.c. drive to the L.C. display. By grounding the backplane output the a.c. drive to the segments may be inhibited and the segment outputs become normal active low (TRUE = 0) outputs. This facility is useful if the output data is to be used for some purpose other than display driving. An L.C. display should not be connected to the ZN451 in this condition as d.c. drive will eventually damage it.

DECIMAL POINT DRIVE

The ZN451 provides all the output necessary to drive the segments of a 3½ digit liquid crystal display. However, in order to drive decimal points and annunciators such as low battery indicators, some external components are required. To turn on a decimal point it is necessary to provide it with a drive signal of the same frequency as, but 180° out of phase with, the backplane output. For driving a single, fixed decimal point, the simple inverter circuit of Fig. 12a can be used.

If more than one decimal point is to be selected then it is necessary for the unused decimal points to be switched off by arranging their drive waveforms to be in phase with the backplane output. This is simply achieved using exclusive OR gates as shown in Fig. 12b.

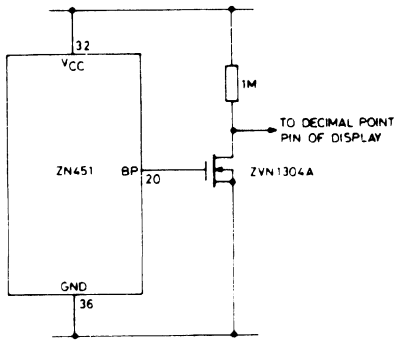


Fig. 12a Driving a fixed decimal point

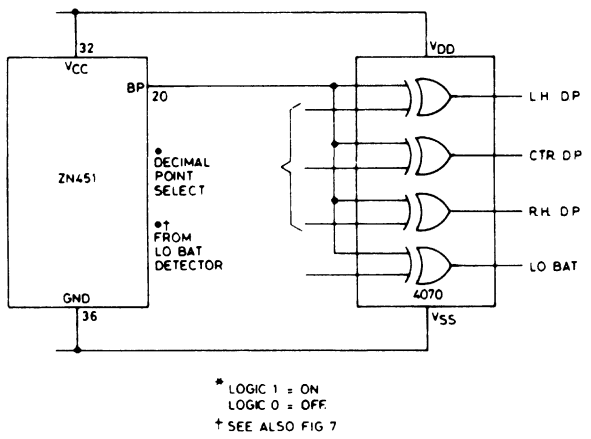


Fig. 12b Decimal point select and 'LO Bat' indicator drive using exclusive OR gates

A logic '1' on the input causes the output waveform to be out of phase with the backplane and the appropriate decimal point is activated. Conversely a logic '0' causes the output to be in phase with the backplane. A single 4070 CMOS quad-EXOR gate I.C. will provide the drive for the three decimal points of a 3½ digit liquid crystal display plus the drive to a low battery indicator. A suitable low battery detection circuit is shown in Fig. 7d.

CALCULATION OF FULL-SCALE RANGE

The component values for any full-scale range depend on the input switching method used. Using method (a) the input voltage is measured only during phase 2, so the equation

$$\frac{NV_{IN}R_{REF2}}{V_{REF}R_{REF1}} = N_1 - \frac{N}{2} \text{ holds.}$$

Since N = 5000 and full-scale reading = ± 1999 this equation can be rewritten as

$$V_{IN}\text{ (full-scale)} = \frac{\pm 1999\ V_{REF}R_{REF1}}{5000\ R_{REF2}}$$

$$= \frac{\pm 0.4\ V_{REF}R_{REF1}}{R_{REF2}}$$

from which required values of R_{REF1} and R_{REF2} can be calculated for any required full-scale input voltage, using either the internal reference of 1.3V or an external reference.

Using input switching method (b) the input voltage is measured during both phases so the displayed count is twice as large for the same input voltage and component values.

The describing equation thus becomes

$$V_{IN}\text{ (full-scale)} = \frac{\pm 0.2\ V_{REF}R_{REF1}}{R_{REF2}}$$

Using input switching method (b) the same full-scale range as method (a) can be obtained if the value of R_{REF1} is doubled or the input signal is attenuated by a factor of two.

These equations are in fact not exact since they do not take account of the reference amplifier offset voltage, which is typically ± 5mV. This offset means that I_{REF} is not precisely $\frac{V_{ref}}{R_{REF2}}$. r_e of T_1 and T_2 in the voltage-current converter also appears in series with R_{REF2} (typically 5k). In practice this is not a problem since the tolerance of the on-chip reference means that a calibration adjustment must be provided anyway. Using the on-chip reference voltage of 1.26-1.35 volts the recommended component values for a full-scale reading of 199.9mV would be R_{REF1} = 200k or 400k, R_{REF2} = 500k (min.), 520k (max.). Allowing for the use of 2% tolerance components for R_{REF1} and R_{REF2} an adequate adjustment range for calibration purposes will be provided if R_{REF2} is made up of a 470k resistor in series with a 100k multiturn trimmer. Full-scale ranges less than 200mV can be accommodated by reducing the value of R_{REF1}, thus producing the same full-scale input current for a smaller input voltage. The limitations on the minimum value of R_{REF1} are caused by non-linearity in the voltage-current converter, offsets in the auto-zero switches, and the fact that r_e becomes a much larger proportion of R_{REF1}. These factors place a practical limit of about 20k on R_{REF1}. As R_{REF1} is reduced, the gain temperature coefficient will also tend to increase.

Similarly full-scale ranges greater than ± 200mV can be accommodated by increasing the value of R_{REF1}. The maximum input voltage that can be applied is limited by the common-mode range of the differential inputs.

The full-scale range can also be adjusted by varying R_{REF2} which determines the reference current, and indeed placing a preset in series with R_{REF2} is the recommended method of calibration.

I_{REF} can also be varied by using an adjustable external reference voltage instead of the internal reference, which makes ratiometric operation possible.

The maximum value of I_{REF} is limited to about 3μA since above this value the voltage-current converter becomes non-linear. The minimum value of I_{REF} is not quite so well defined as it is determined by deterioration in the performance of current switches T_3 and T_4 at low collector currents. The minimum useable value of I_{REF} is typically 500nA. This means that the upper and lower limits are $\frac{V_{REF}}{500nA}$ and $\frac{V_{REF}}{3\mu A}$ respectively. The upper and lower limits on V_{REF} itself are determined by the common-mode range of the reference current amplifier A_1 which is 1 to 1.5V. Ratiometric operation with a variable V_{REF} within these limits is possible provided that the upper or lower limit of I_{REF} is not exceeded.

PRACTICAL APPLICATIONS AND DESIGN PRECAUTIONS

Since the input switching of the ZN451 is external to the device it is possible to include op-amps and other signal conditioning circuits within the auto-zero loop and thus eliminate their zero errors.

The two methods of input switching are shown in Figs. 13a and 13b. In Fig. 13a a series switch and shunt switch disconnect the input signal during phase 1. In Fig. 13b a switch bridge reverses the polarity of the input signal during phase 1.

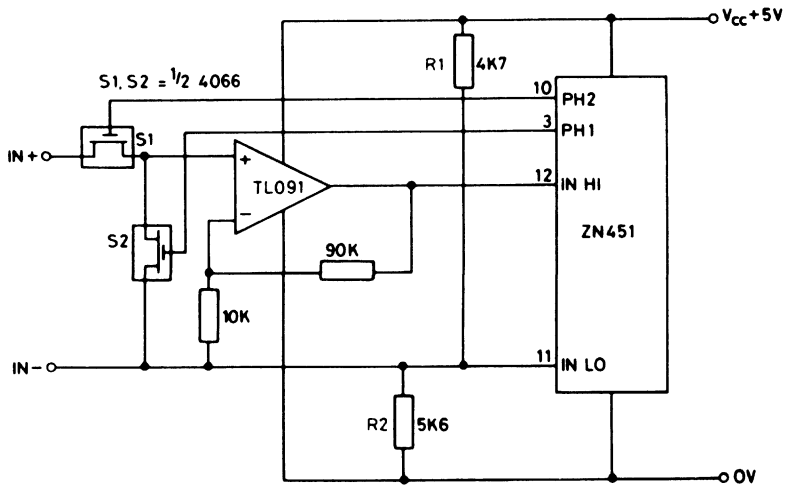


Fig. 13a

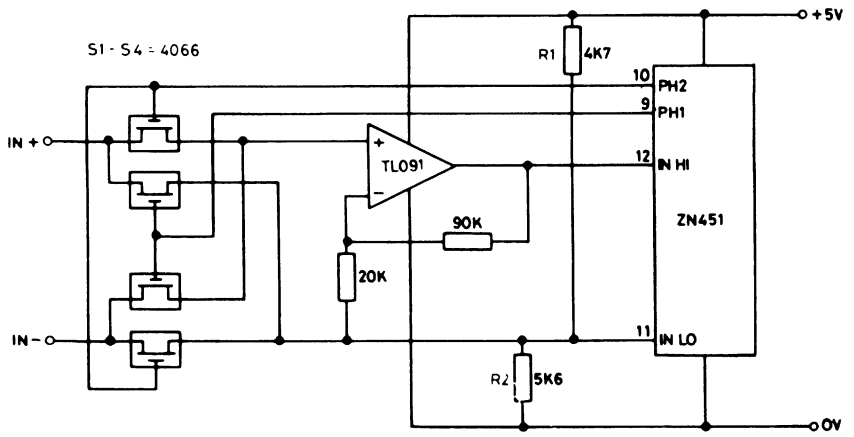


Fig. 13b

Two practical circuits for 20mV full-scale DVM are given in Figs.. 13a and 13b. In the circuit of Fig. 13b note that the gain of the op-amp is 5 since the effective full-scale sensitivity of the ZN451 is 100mV, whereas in Fig. 13a it is 200mV. The same result could be achieved by making the op-amp gain 10 in both cases but doubling the value of R_{REF1} in Fig. 13b.

These simple circuits can be used to illustrate some design precautions that must be observed when using the ZN451.

1) The output voltage of the signal conditioning circuits should be within the common-mode range of the ZN451.

2) The common-mode and differential input voltages must be within the input range of the switches and signal conditioning circuits.

These two criteria are met in Figs. 13a and 13b by providing an analogue common point at approximately +2.5V by means of R_1 and R_2. Assuming battery operation of the ZN451 this analogue common point will float up and down with the common mode voltage of the input signal thus keeping the input voltage within the common-mode range of ZN451 and the input circuits.

3) The offset error at the input of the ZN451, when added to the full-scale input voltage, must not cause saturation of the DSM. Using input switching method (b) this means that the zero error can be 150% of the full-scale range of the DVM.

When designing signal conditioning circuits care must be taken to ensure that this limit is not exceeded.

In many circuits the principal source of zero error will be the offset voltage of the op-amp, in which case a good rule of thumb is that the input offset voltage should not exceed the full-scale input voltage, to allow some overload margin to be retained.

However, in some signal conditioning circuits there may be sources of zero error other than the op-amp, in which case care must be taken to meet the offset criteria at the ZN451 inputs. An example of such a circuit is given in Fig. 15.

Using low-cost monolithic op-amps it is a simple matter to design for full-scale inputs of ±20mV or less. For inputs below 2mV more expensive instrumentation amplifiers must be used. Alternatively the offset can be nulled out when calibrating the DVM, leaving the auto-zero to cope with long-term and temperature drift of the zero.

4) There should be no rapid temperature fluctuations in the signal conditioning circuits as this could cause the zero error to vary from phase 1 to phase 2.

Example, with full-scale input of 1.999mV and an op-amp with an offset tempco of 10μV/°C a 0.1°C change in temperature between phase 1 and phase 2 will cause a zero error of 1μV = 1 count.

This is likely to be a problem only with very small full-scale ranges. It can be reduced by thermally insulating the signal conditioning circuits or by plotting them to increase the thermal inertia so that the temperature can only change slowly.

5) With very small input voltages thermal e.m.f.'s may become a problem. In this case care should be taken to ensure that the input + and input − signal paths to the signal conditioning circuits are identical so that thermal e.m.f.'s cancel out. Such precautions may include the use of identical input switches in series with both the input + and input − leads.

Although Fig. 13b shows the simplest way of implementing input switching method (b), using only one op-amp, this configuration may have disadvantages in some applications, since the input LO terminal of the ZN451 is tied permanently to analogue common, whilst the input voltage is reversed. This means that the supply rails of the ZN451 shift up and down with respect to the input signal common. This is generally not a problem in battery-powered circuits unless the signal source impedance is very high, when charging and discharging of stray capacitance may cause errors.

Fig. 14 shows a circuit in which the signal 0V is connected to a fixed analogue common whilst the inputs of the ZN451 are reversed. In order that the input impedanced seen by the signal is the same during both measurement phases both inputs of the ZN451 are driven from identical op-amp circuits. These are shown as voltage followers but can be given greater than unity gain by adding the dotted components.

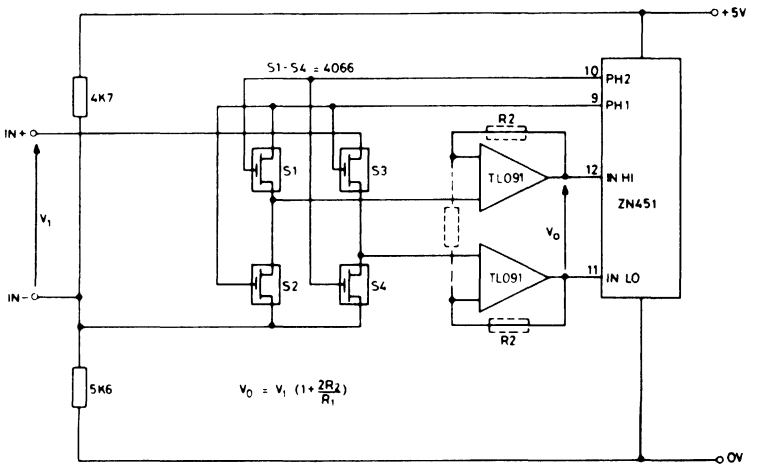


Fig. 14

In some systems it may be necessary for analogue common to be the 0V supply rail or some other voltage not within the common-mode range of the ZN451.

This can be achieved by offsetting the output voltage of the signal-conditioning circuits to bring it within the common-mode range of the ZN451. Also if the input voltage falls outside the V_{CC} and 0V rails of the ZN451 the supply voltage to the analogue switches must be such that they can accommodate the signal, and the PH_1 and PH_2 outputs of the ZN451 must be level-shifted in order to control the switches. An example of such a circuit is shown in Fig. 15. This is a $\pm$200mV DVM operating from $\pm$5V with the 0V rail as analogue common.

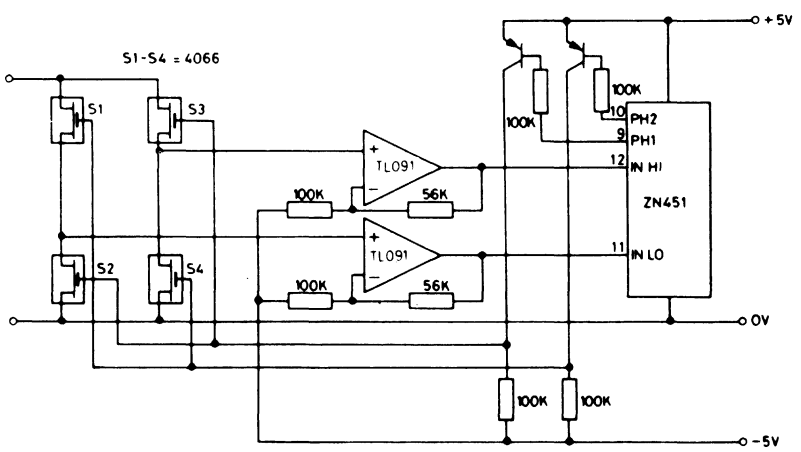


Fig. 15

The ZN451 operates from the +5 and 0V rails whilst the input switches and op-amps operate from ±5V. Two PNP transistors convert the 0 to +5V swing of the PH_1 and PH_2 outputs to a ±5V swing. Since they also invert the outputs the PH_1 and PH_2 outputs are transposed.

The two op-amps are connected in a non-inverting configuration but with the feed-back network returned to −5V instead of 0V. By making the op-amp gain 1.56 this gives an off-set of approx. +2.8V with a 0V input which brings the output within the common-mode range of the ZN451.

Since the op-amp gain is 1.56 the values of R_{REF1} and R_{REF2} must be chosen for ±312mV full-scale to give a full-scale input range of ±200mV.

In this circuit there are two sources of zero error for which the ZN451 must compensate: firstly the offset voltages of the two op-amps multiplied by their gain; secondly and more significant the difference in the quiescent op-amp output voltages caused by gain mis-matching between the two op-amps.

$$\pm \{5 \times (\text{max. gain } A_1 - \text{min. gain } A_2)\}$$

$$= \pm \left\{ 5 \times \left(\frac{98 + 57}{98} - \frac{102 + 55}{102} \right) \right\}$$

$$= \pm 212\text{mV}$$

This is 68% of the full-scale input range of the ZN451, which is acceptable.

ADDITIONAL INPUT CONDITIONING

For use in a multirange instrument such as a DVM, additional signal conditioning circuits will be required for the measuring of a.c. and d.c. voltages, a.c. and d.c. current, and resistance. Some suggested circuits are shown on the following pages.

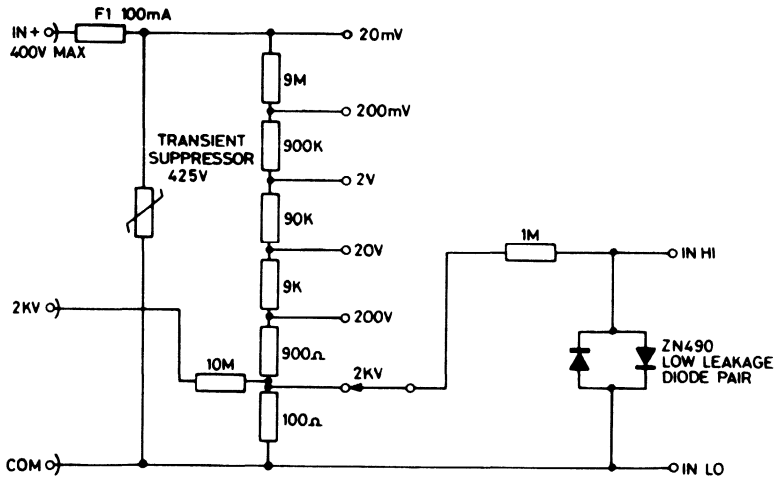


Fig. 16

Fig. 16 shows an input attenuator for the measurement of voltages from 20mV to 2kV. This has a standard input resistance of 10M.

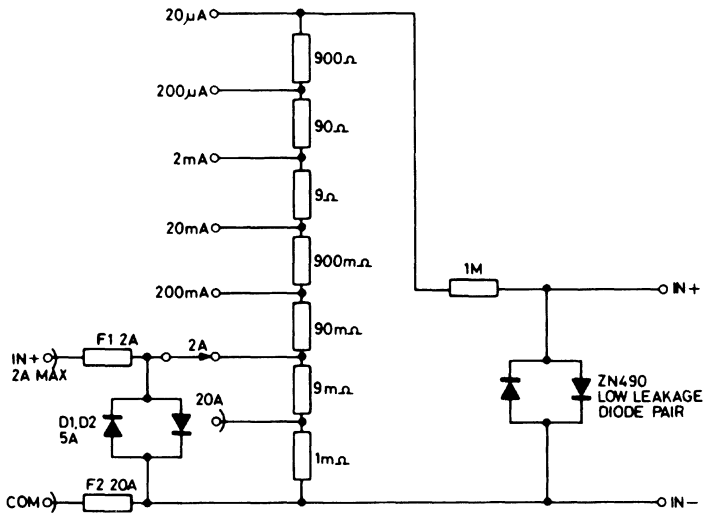


Fig. 17

Fig. 17 shows a universal shunt for the measurement of currents from 20μA to 20A with a full-scale voltage drop of ± 20mV.

Resistance can be measured by passing a known, constant current through an unknown resistor and measuring the voltage drop across it.

An ohmmeter circuit is given in Fig. 18.

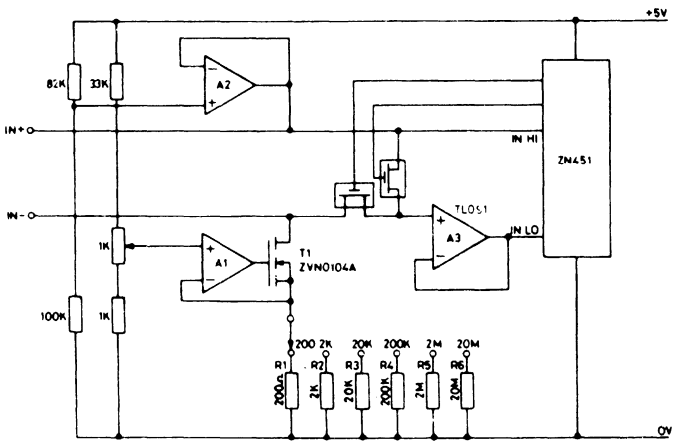


Fig. 18

Op-amp A_1 and Mosfet T_1 form a constant current sink whose output current is defined by resistors R_1-R_6 and a reference voltage derived from the stabilised + 5V rail.

Op-amp A_2 provides a low impedance analogue common point which can source the current from the + 5V rail without its voltage changing. The maximum full-scale voltage drop across the resistor under test is 200mV.

A.C. MEASUREMENTS

To measure a.c. voltage or current it is first necessary to convert it into a proportional d.c. voltage. The simplest way to do this is to interpose a precision active rectifier circuit between the attenuator or shunt and the inputs of the ZN451. Such a circuit produces d.c. voltage proportional to the mean of the rectifier voltage rather than a true R.M.S. result and for true R.M.S. measurements an R.M.S. converter must be used. The rectifier can be calibrated to read R.M.S. but the result is true only if the input signals have a constant form factor.

A simple precision rectifier circuit is shown in Fig. 19. It is completely a.c. coupled throughout by C_2, C_3 and C_4, so the offset voltage of A_1 does not appear at the output and no zero adjustment is required. To prevent the offset voltage of A_1 causing it to saturate in the absence of an input signal, 100% d.c. feedback is provided by R_3.

R_1 and R_2 provide a d.c. bias path for the non-inverting input of A_1, whilst C_2 provides bootstrapping to increase the a.c. input impedance.

Amplifier A_2 is a voltage follower biased into the middle of the ZN451's common-mode range to provide a low impedance analogue common point. The output of the rectifier is connected to a lowpass filter comprising R_6 and C_5. These components are chosen to give a time constant of 300ms which allows input frequencies down to 40Hz whilst maintaining an acceptably short response time.

With the component values shown the circuit is calibrated to read R.M.S. for sine-wave input, so the use of this waveform will be assumed throughout.

The circuit functions as follows: when the input signal crosses zero in a positive going direction the output of A_1 slews positive until D_2 conducts, after which the voltage at point A is defined by the equation: $V_A = G\,V_{IN}$, where G is the gain defined by R_4 and R_5 shunted by R_2. This voltage attempts to charge up C_5 via R_6 in a positive direction.

When the signal crosses zero in a negative-going direction the output of A_1 slews negative until D_1 conducts, after which the output voltage at point B is equal to (minus) V_{IN}. This voltage attempts to charge up C_5 in a negative direction via R_4 and R_6.

When the circuit has reached equilibrium there will be a constant d.c. voltage (V_C) on C_5 with negligible a.c. ripple (otherwise it could not be measured by the DVM without flicker of the display).

This means that the mean current flowing into C_5 during the positive half-cycle must exactly equal that flowing out of C_5 during the negative half-cycle.

$$\text{i.e. } \frac{V_A(\text{MEAN}) - V_C}{R_6} = \frac{-V_B(\text{MEAN}) + V_C}{R_6 + R_4}$$

Now the mean value of a rectifier sinewave is 0.9 times the R.M.S. value therefore

$$V_A(\text{MEAN}) = 0.9.G.\ V_{IN\ (RMS)}$$

$$\text{and } V_B(\text{MEAN}) = -0.9\ V_{IN\ (RMS)}$$

For the DVM to read correctly V_C must equal $V_{IN\ (RMS)}$

$$\text{therefore } V_A = 0.9.G.V_C$$

$$\text{and } V_B = -0.9.V_C$$

$$\text{thus } \frac{V_C(0.9G - 1)}{R_6} = \frac{1.9V_C}{R_6 + R_4}$$

$$\frac{0.9G - 1}{R_6} = \frac{1.9}{R_6 + R_4}$$

R_4 and R_6 can be chosen arbitrarily provided that the values are "sensible", and that the time constant R_6, C_5 is correct.

Therefore, choosing a value of 200k for R_6 and 10k for R_4 and substituting these values in the above equation.

$$\frac{0.9G - 1}{200} = \frac{1.9}{21.0}$$

$$189G - 210 = 380$$

$$G = \frac{590}{189}$$

$$= 3.122$$

Therefore the value of the parallel combination of R_5 and R_2 is 4.712k. Since $R_2 = 1M$ $R_5 = 4.73k$.

Using the component values shown the circuit is accurate at about $\pm$ 1.5% over the frequency range 40Hz to 1KHz.

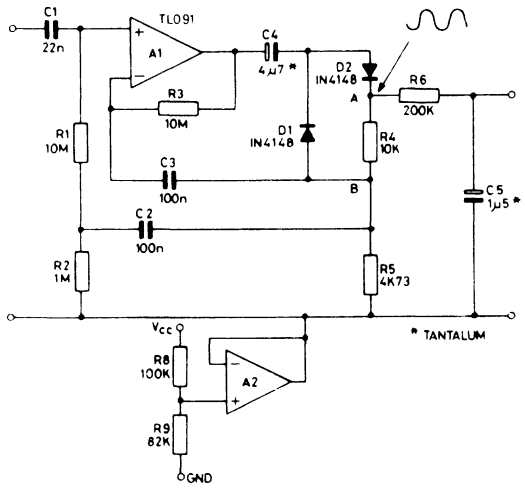


Fig. 19

ORDERING INFORMATION

Device type	Operating temperature	Package
ZN451E	0°C to +70°C	DP40
ZN451CJ	0°C to +70°C	DC40

ZN454E

TRIPLE 4-BIT VIDEO D-A CONVERTER

The ZN454 consists of three 4-bit D-A converters, providing a colour palette of 4096 possible display colours. The required logic translators, control logic, a reference voltage source and reference amplifier are also integrated on-chip.

Each D-A converter accepts 4-bit digital video data and SYNC/BLANK signals directly from a TTL source and produces a composite video output to directly drive a 75Ω line terminated by a 75Ω load at both ends.

The ZN454 is ideally suited for pixel colour generation in graphics display systems requiring 4-bit colour resolution. The high linearity of each DAC ensures excellent colour contrast and the fast update rate allows the device to be interfaced to monitors with a resolution of up to 1024 x 1280 pixels assuming a standard refresh rate of 60Hz.

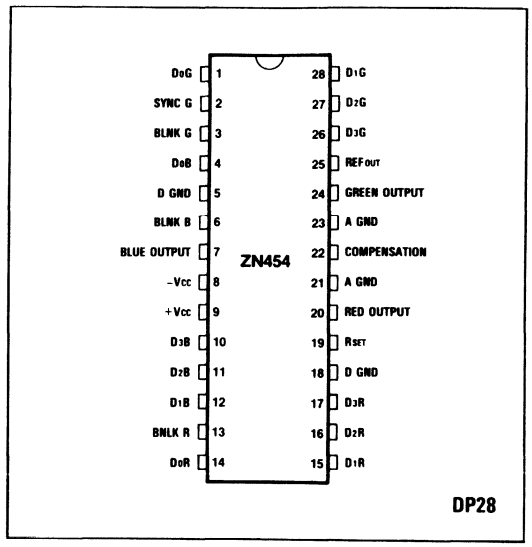


Fig.1 Pin connections - top view

FEATURES

- 3 Video DAC's - Ideal for Colour Graphics
- Fast, 8ns Settling Time
- Update Rates to 100MHz
- Low Glitch Energy
- ¼ LSB Linearity Error
- On-Chip Reference Source
- Composite Sync and Blank Inputs
- TTL Compatible Inputs
- Generates Standard Video Signal Output Across a Doubly Terminated 75 Ohm Load
- 28 Pin DIL Package

GENERAL CIRCUIT DESCRIPTION

Each D-A converter of the ZN454 uses high speed switches to steer current from precision current sources to either analog ground or to the analog output - as governed by the digital inputs (see Fig.4). The analog output voltage is now obtained from these weighted current sources producing the desired voltage drop across the 37.5Ω load impedance. The gain of the D-A converters is adjustable via RSET.

Since the ZN454 utilises current output DAC's the output impedance is inherently high. Thus a 75Ω resistance is required (adjacent to each DAC output) to shunt this high impedance and provide the correct impedance for driving a 75Ω line terminated in 75Ω at the monitor. The desired 1V p-p composite signal will now be developed across this effective 37.5Ω output impedance.

The grey scale output current of each DAC has 16 levels from 0 to -17mA nominally (see Fig.3). This develops 16 levels of output voltage from 0 to -643mV across the specified 37.5Ω load impedance. the 'REFERENCE WHITE' level (0V) corresponds to the digital input code 1111 and the 'REFERENCE BLACK' (-643mV) to 0000.

A logic '1' on the BLANK input overrides the data inputs and drives the output to 71mV more negative than the 'REFERENCE BLACK' level. This corresponds to the 'BLANKING' (or 'blacker-than-black') level.

Activating the SYNC input (logic '1') with the BLANK input 'high' drives the output to 286mV more negative than the 'BLANKING' level. This voltage (nominally -1V) corresponds to the 'SYNC' level.

GAIN ADJUSTMENT (RSET)

RSET provides a means of adjusting the current in the weighted current sources. An amplifier compares the voltage developed across RSET, with the reference voltage. If RSET is increased/decreased the amplifier output causes the current through RSET to decrease/increase (to bring the voltage across RSET back in line with the reference voltage). This also causes the current in each of the current sources to decrease/increase (see Fig.3). In this manner the magnitude of the output waveform can be varied to obtain the desired levels.

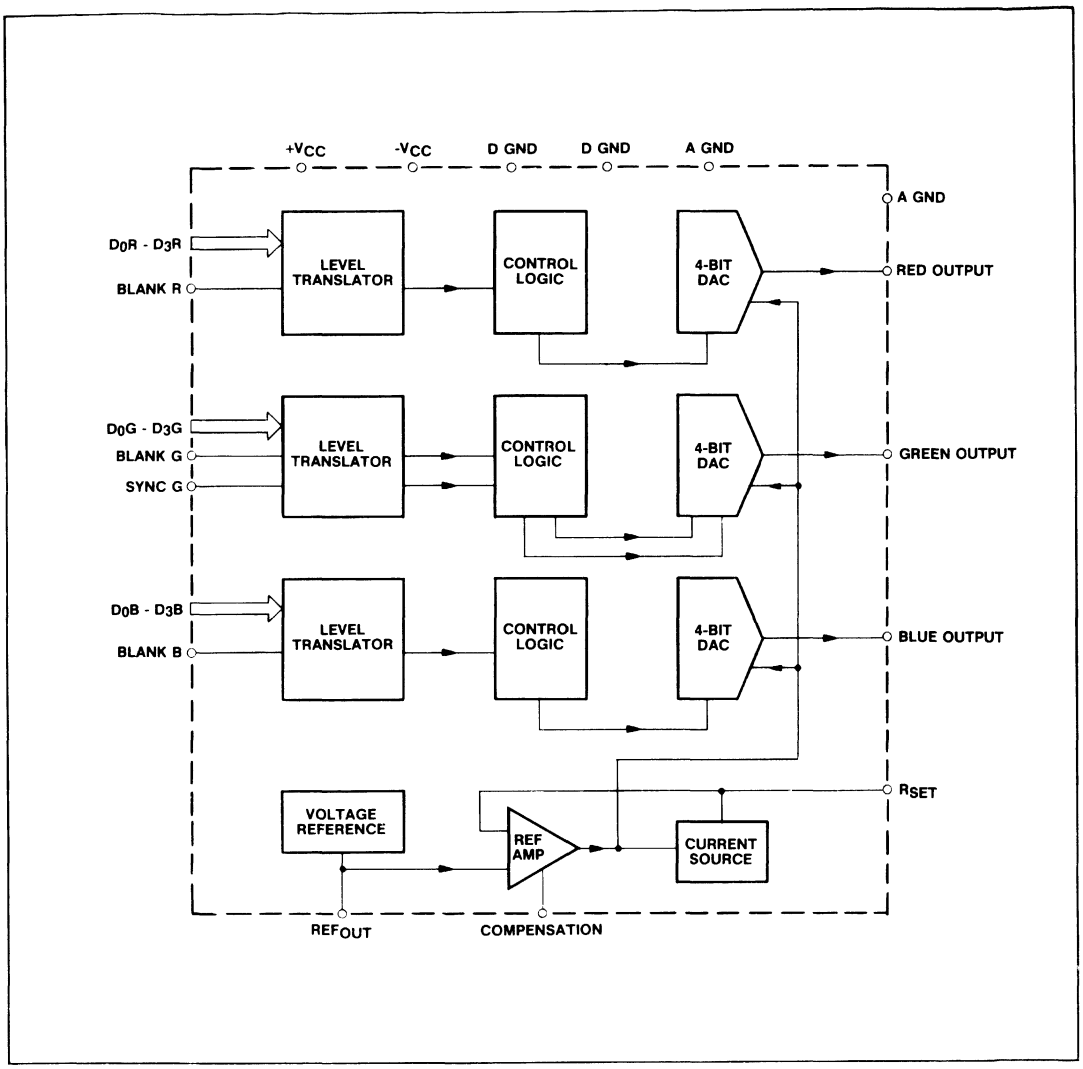


Fig.2 Block diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage, $+V_{CC}$	+6V
Supply voltage, $-V_{CC}$	-6V
Logic input voltage	$+V_{CC}$
Operating temperature range	0°C to 70°C
Storage temperature range	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25°C, V_{CC} = ±5V, R_L = 37.5Ω and R_{SET} = 180Ω

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Resolution		4			Bits	
LSB weight (current)			1.13		mA	Note 1
LSB weight (voltage)			43		mV	
Accuracy						
Linearity error			±0.25	±0.5	LSB	
Differential linearity error				±0.5	LBS	Note 2
Offset error			-5.0	-15.0	mV	
Gain error				±5	% of nom.FSR	
Speed performance - Grey scale output						
Rise/fall times (voltage)			3		ns	10-90% of final value
Settling time (voltage)			8		ns	Note 3
Maximum update rate			100		MHz	Note 4
Slew rate			180		V/μs	10-90% of final value
Glitch energy			60		pV-s	Note 5
Temperature coefficient						
Offset			10		ppm/°C	Measured with
Gain			500		ppm/°C	internal reference
Data, sync and blank inputs						
Logic compatibility			**TTL**			
High level input voltage	V_{IH}	2.0			V	
Low level input voltage	V_{IL}			0.8	V	
High level input current	$I_{IH(1)}$			+20	μA	V_{CC} = max, V_{in} = 5.5V
	$I_{IH(2)}$			±10	μA	V_{CC} = max, V_{in} = 2.4V
Low level input current	I_{IL}			-1.6	mA	V_{CC} = max, V_{in} = 0.4V
Coding (see Fig.2)			**Complementary binary**			
Output - Grey scale						
Voltage range			0.64		V	Note 1
Current range			17		mA	
Output - Composite sync						
Voltage range			286		mV	
Current range			7.6		mA	
Output - Composite blanking						
Voltage range			71		mV	
Current range			1.9		mA	
Output voltage compliance		0		1.5	V	
Internal voltage reference						
Output voltage	V_{REF}		-1.26		V	
Output voltage tolerance				±5.0	%	
Output voltage TC			200		ppm/°C	0°C to 70°C
Power supply requirements						
Supply voltage	+V_{CC}	4.5	5.0	5.5	V	
	-V_{CC}	-4.5	-5.0	-5.5	V	
Supply current	+I_{CC}		22.5		mA	
	-I_{CC}		136.0		mA	

NOTES
1. LSB and full-scale output levels adjustable with R_{SET}. 2. Monotonicity guaranteed over full operating temperature range.
3. The settling time was measured as the time between the start of the output rising/falling edge to where the output entered and remained within ±½ LSB of the final value. The value quoted is for a transition from reference white to reference black and vice versa, and does not include the inherent input propagation delay (2-3ns). See section describing settling time measurement.
4. The maximum update rate is limited by the full-scale settling time to rated accuracy.
5. Measurement of glitch energy is discussed in a later section of this data sheet.

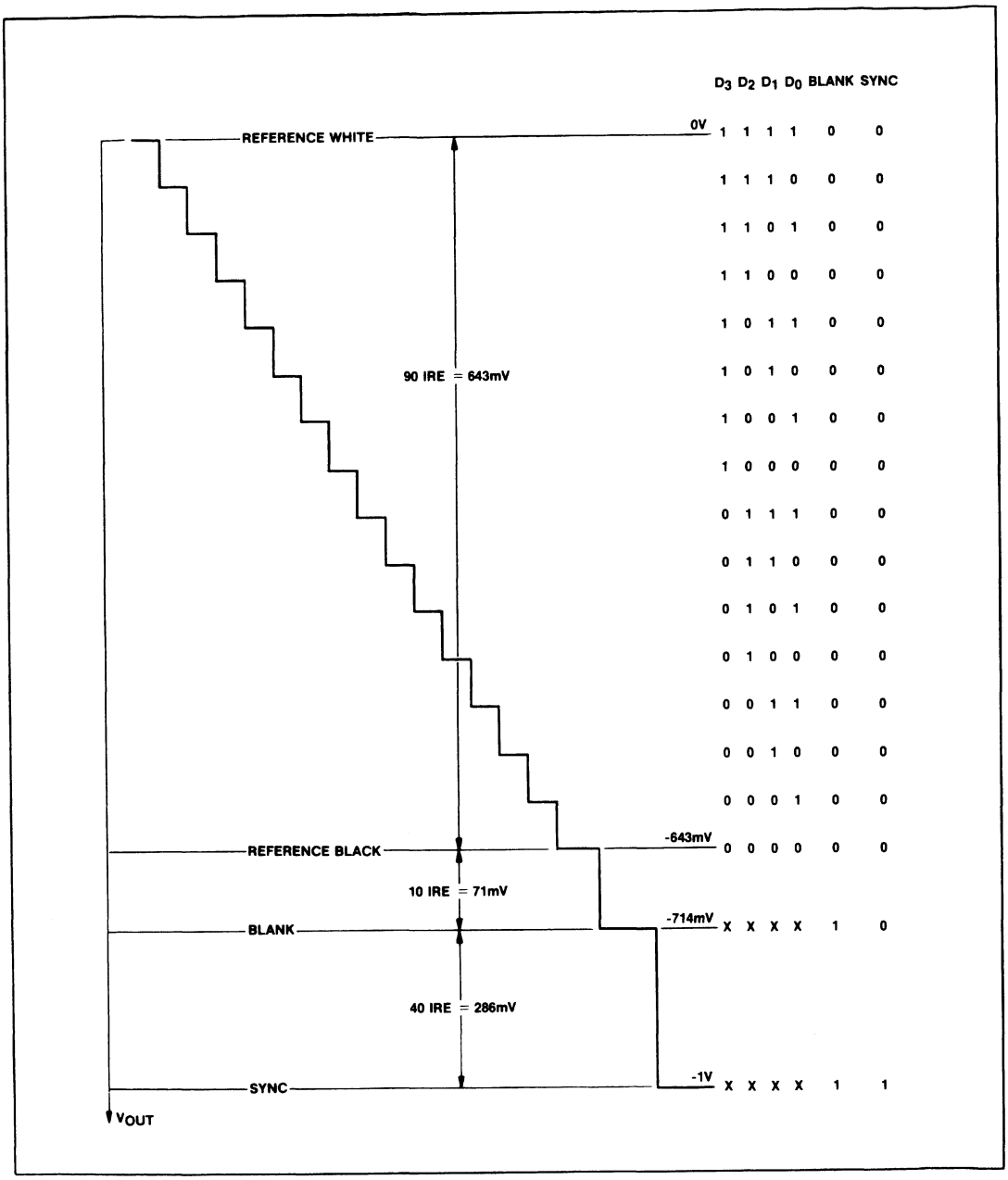


Fig.3 Typical composite video output waveform

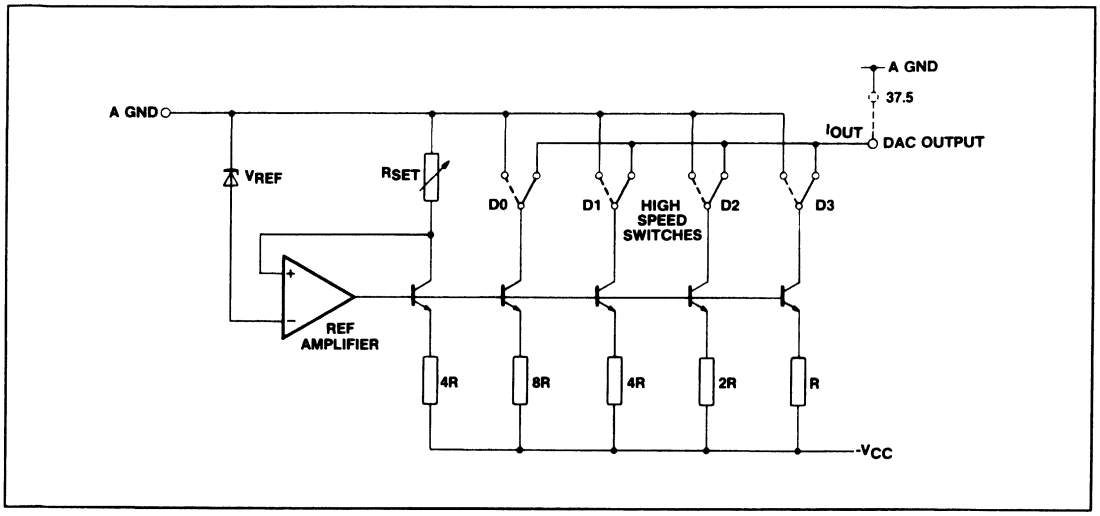


Fig.4 Current source array (schematic)

DIGITAL INPUTS

The digital inputs are high speed level translators (see Fig.5).

The ZN454 requires very few external components for normal operation. Fig.6 illustrates the external component connections.

LAYOUT CONSIDERATIONS

When using the ZN454, as with any other device of this kind, certain precautions must be taken to obtain the best performance.

Some of the requirements are:

1. A ground plane board providing a good earth and with good power supply connections, to keep noise to a minimum.

2. Good decoupling - especially around all the fast switching circuits - including a 0.1μF capacitor from both the +5V and -5V supplies positioned close to the ZN454. The ground connections for these capacitors should be adjacent.

3. Some physical separation between the digital input tracks to minimise crosstalk.

4. Matched digital input signal paths to avoid introducing any unnecessary time skew between the inputs. This would cause glitches on the DAC outputs with changing codes. Also the outputs from the driving device will have to be well matched for the same reason.

5. 75Ω resistors close to the DAC outputs, to provide the correct impedance for driving 75Ω lines.

SETTLING TIME AND GLITCH ENERGY MEASUREMENT

In a finished design the ZN454 would be soldered directly into the board to obtain the best performance possible. However for evaluation purposes a socket really needs to be used. This will give some degradation in performance but useful results can still be obtained.

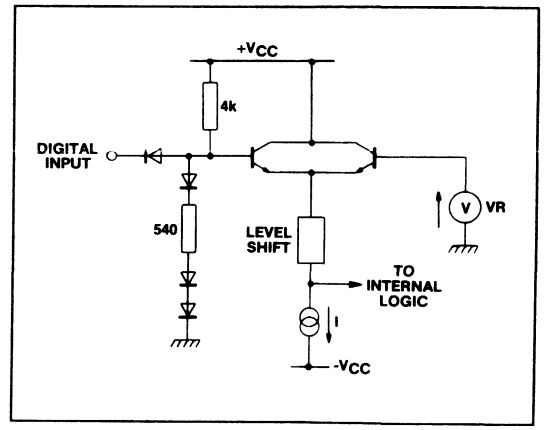


Fig.5 Equivalent circuit of sync, blank and data inputs

Measurement of settling time and glitch energy is not a straightforward task and all of the recommendations previously noted must be adhered to. If these parameters are to be measured using an oscilloscope, great care must be taken to avoid corrupting the analog outputs e.g. conventional probes cannot simply be clipped onto the outputs as this would cause reflections giving rise to errors. Instead the ZN454 needs a 75Ω termination near the chip, a 75Ω cable - also grounded close to the chip - connecting to a 75Ω lead through termination at the oscilloscope. Optimum cable length is about 6 inches but it may need trimming around this. Also the oscilloscope obviously needs to have sufficient bandwidth to cope with the rise and fall times encountered.

The digital circuits driving the DAC's must not introduce too much noise, or time skew between the bit inputs. This

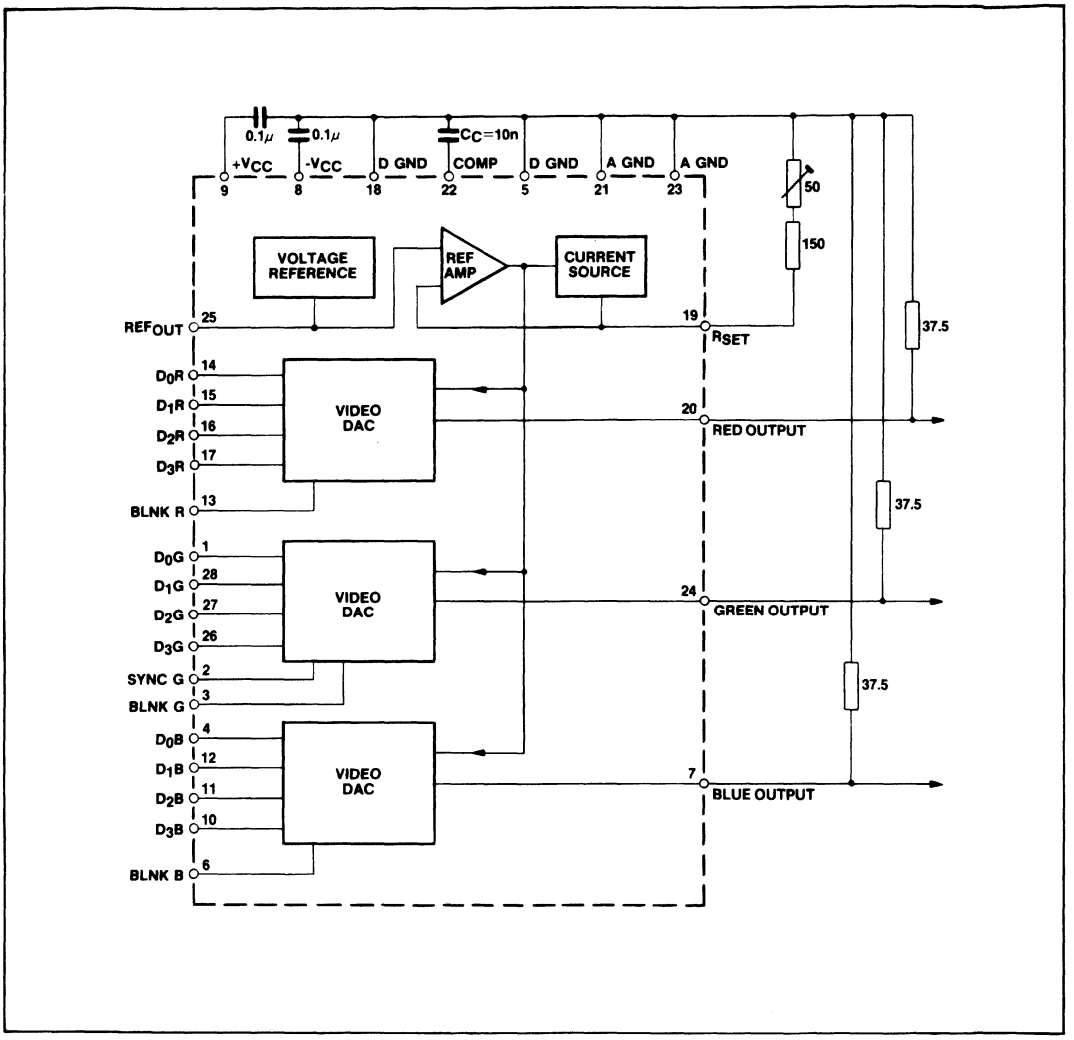


Fig.6 External component connections

can considerably affect the results. However, a convenient way of minimising these problems for evaluation purposes, is to drive the digital inputs directly from a pulse generator. Full-scale transitions of the grey scale can now be monitored by wiring the inputs to a given DAC in parallel (terminating in 50Ω) and clocking with the pulse generator. Each output can now be examined in turn. The circuit diagram is as in Fig.6 except that the sync and blank inputs will be tied low. The 37.5Ω terminations on the DAC output, and the digital input signals are provided as described above. Fig.7 shows an actual full-scale (grey scale) output transition measured using the above procedure, giving a settling time of 5.12ns.

Glitch energy measurements, at the major transition for example, can also be measured by driving the digital inputs directly from a pulse generator but it will need to have well matched complementary outputs. Also the lead lengths from the generator to the digital inputs will have to be well matched (and terminated in 50Ω). This is so because this measurement is especially critical of any time skew between the input signals. Indeed even an ideal DAC would produce glitches if there were timing differences between these changing input signals. These time skew errors which would manifest themselves as exaggerated glitches on the DAC output, are referred to the point at which the input signals cross the digital input thresholds (≏1.5V nom.). Thus the characteristics of the driving signals will have some effect on the amplitude of the glitches, which may be minimised by careful design. The circuit arrangement for measuring the glitch energy is as above but with the digital inputs being switched through different codes. Fig.8 shows an actual mid-scale glitch, measured using the above procedure.

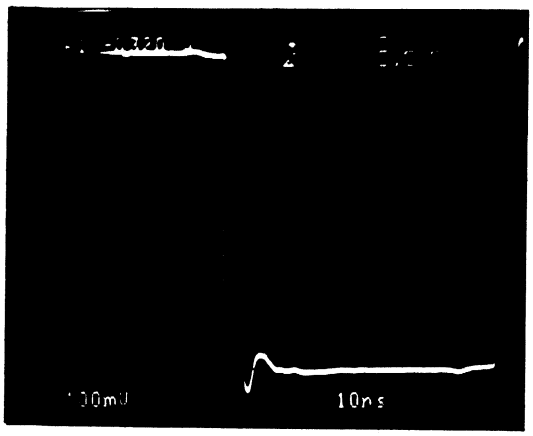


Fig.7 Full-scale output transition - settling time

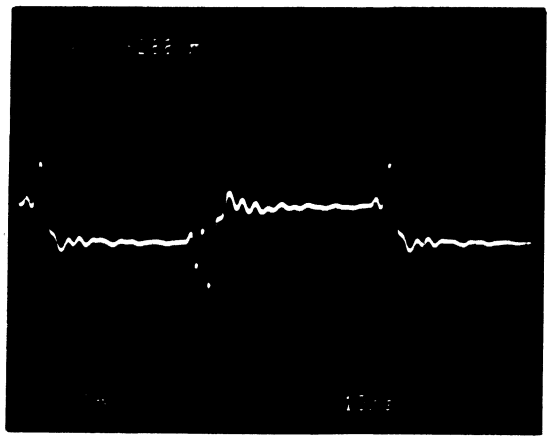


Fig.8 Mid-scale output glitch

GLOSSARY OF VIDEO TERMS

Raster scan

The method of sweeping a CRT one line at a time to generate and display images.

Composite video signal

The VIDEO signal plus the BLANK and SYNC signals.

Video signal

The portion of the composite VIDEO SIGNAL which varies in grey scale levels between 'reference white' and 'reference black' - this is the portion which is visually observed.

Sync signal

The portion of the video waveform that synchronises the raster scanning process.

Grey scale

The discrete levels between and including 'reference white' and 'reference black' - there are 16 levels for a 4-bit DAC.

Blanking level

The level separating the SYNC portion from the VIDEO portion. Usually referred to as the FRONT PORCH or BACK PORCH, this is the level which will shut off the electron guns resulting in the blackest possible display.

Sync level

The negative peak level of the sync signal.

Reference black level

The maximum negative level of the VIDEO signal.

Reference white level

The maximum positive level of the VIDEO signal.

ZN455CJ

TRIPLE 4-BIT VIDEO MEMDAC

The ZN455 consists of three 4-Bit Video D to A converters each with a 16 x 4 colour map allowing the simultaneous display of 16 colours from a palette of 4096 colours. The ZN455 has two levels of pipeline to allow a high pixel rate and to ease system timing requirements. The first level is prior to each of the video RAM's on the ECL address bus and the output data from these RAM's is latched at the second level prior to being converted.

The ZN455 offers a versatile microprocessor and video controller interface and each output directly drives a doubly terminated 75Ω transmission line. The incorporation of a bandgap reference source, composite video controls, address latches and DAC input latches make this device the ideal choice for high performance bit-mapped colour graphics systems.

FEATURES

- 3 Video DAC's
- On-Chip Colour Look-Up Tables
- Update Rates to 100MHz
- Fast, 8ns DAC Settling Time
- Low Glitch Energy
- ¼ LSB Linearity Error
- On-Chip Data Latches
- On-Chip Voltage Reference Source
- TTL/ECL Compatible Inputs
- Composite Sync and Blanking Control Inputs
- Generates Standard (RS330, RS343) Video Signal Output Across a Doubly Terminated 75 Ohm Load
- 28 Pin DIL Package

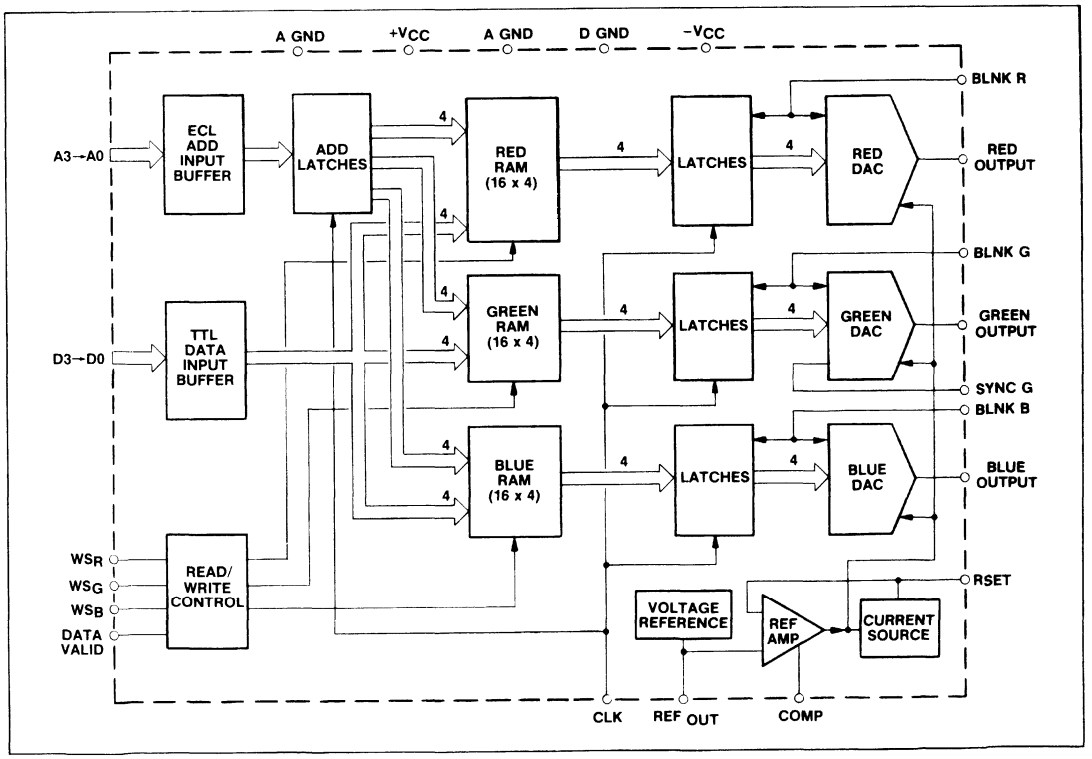


Fig.1 System diagram

PLESSEY
Semiconductors

ZN501AJ/ZN502E/CJ

10-BIT MICROPROCESSOR COMPATIBLE A-D CONVERTERS

The ZN501 and ZN502 range of successive approximation A-D converters combine several innovations to provide this function on a fully monolithic silicon integrated circuit. The chip consists of a current switching array (requiring no trim), successive approximation logic, 2.5V precision reference, reference amplifier, comparator and three-state output buffers.

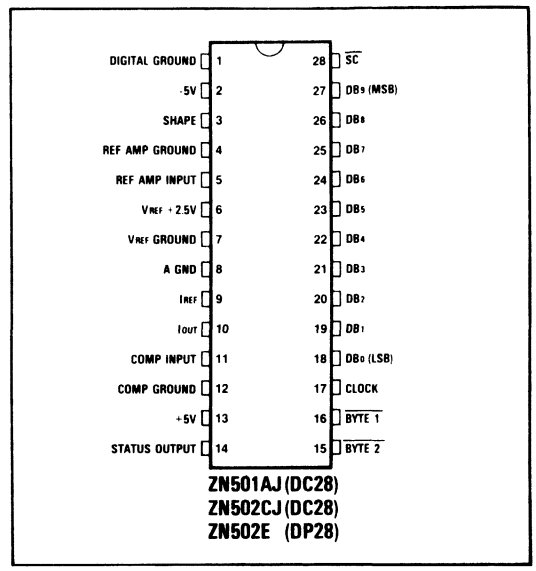
With the aid of $\overline{\text{BYTE 1}}$ and $\overline{\text{BYTE 2}}$ the 10 bits of O/P data can be read as a 10-bit word or as 8- and 2-bit words.

FEATURES

- Choice of Linearity: ½ LSB - ZN501, 1 LSB ZN502
- Three-State Outputs, TTL Compatible
- 15 microseconds Typical, 20 microseconds Guaranteed Conversion Time
- Input Range as Desired
- Asynchronous $\overline{\text{START CONVERT}}$
- +5V, -5V Supplies, Microprocessor and TTL/CMOS Compatible
- Commercial or Military Temperature Ranges
- Full 8- or 16-Bit MICRO-Bus Interface
- Available in Ceramic or Moulded Package

ORDERING INFORMATION

Device type	Operating temperature	Package
ZN502E	0°C to +70°C	DP28
ZN502CJ	0°C to +70°C	DC28
ZN501AJ	-55°C to +125°C	DC28



ZN501AJ (DC28)
ZN502CJ (DC28)
ZN502E (DP28)

Pin connections - top view

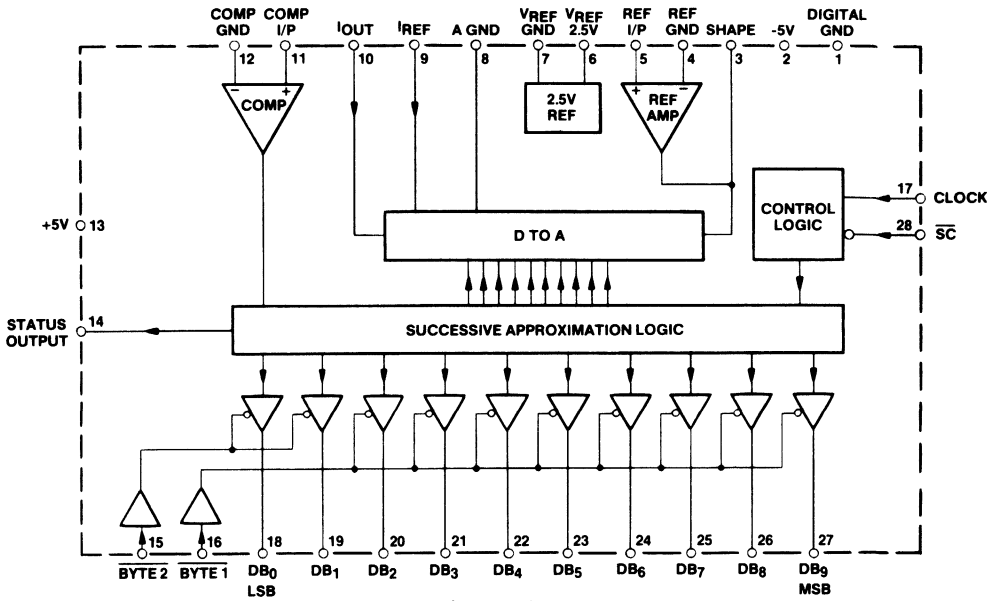


Fig.1 System diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC+}	+7V
Supply voltage V_{CC-}	-7V
Logic input voltage	+Vcc and 0V
Operating temperature range	0°C to 70°C (ZN502E, ZN502CJ)
	-55°C to +125°C (ZN501AJ)
Storage temperature range	-55°C to +125°C

ELECTRICAL CHARACTERISTICS (at +5 and −5V supplies and internal reference unless otherwise specified).

		T_{amb} = +25°C			Over Spec			
Parameter	Version	Min.	Typ.	Max.	Min.	Max.	Units	Conditions
	ZN501AJ							
Linearity error				±0.5		±0.5	LSB	
Diff. linearity error				±0.75		±0.75	LSB	Note 1
Unipolar offset			±0.55	±1.0		±1.0	LSB	Ext. Ref.
			±0.55	±1.0		±1.0	LSB	Int. Ref.
Bipolar offset			±0.55	±1.0		±1.0	LSB	Ext. Ref.
			±0.55	±1.0		±1.0	LSB	Int. Ref.
Gain error			±0.55				LSB	Ext. Ref.*
			±3				LSB	Int. Ref.*
TEMPERATURE COEFFICIENTS (T_{min} to T_{max})								
Unipolar offset			7 typ., 10 max.				ppm/°C	Ext. Ref.
			7 typ., 10 max.				ppm/°C	Int. Ref.
Bipolar offset			7 typ., 10 max.				ppm/°C	Ext. Ref.
			7 typ., 10 max				ppm/°C	Int. Ref.
Gain			10 typ.				ppm/°C	Ext. Ref.
			50 typ.				ppm/°C	Int. Ref.
	ZN502CJ							
Linearity error				±1.0		±1.0	LSB	
Diff. linearity error				±1.0		±1.0	LSB	Note 1
Unipolar offset			±0.55	±1.0		±1.0	LSB	Ext. Ref.
			±0.55	±1.0		±1.0	LSB	Int. Ref.
Bipolar offset			±0.55	±1.0		±1.0	LSB	Ext. Ref.
			±0.55	±1.0		±1.0	LSB	Int. Ref.
Gain error			±0.55				LSB	Ext. Ref.*
			±3				LSB	Int. Ref.*

*See note 4

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	Version	T_{amb} = +25°C Min.	Typ.	Max.	Over Spec Min.	Max.	Units	Conditions
TEMPERATURE COEFFICIENTS (T_{min} to T_{max})								
Unipolar offset			15 typ., 20 max.				ppm/°C	Ext. Ref.
			15 typ., 20 max.				ppm/°C	Int. Ref.
Bipolar offset			15 typ., 20 max.				ppm/°C	Ext. Ref.
			15 typ., 20 max.				ppm/°C	Int. Ref.
Gain			20 typ.				ppm/°C	Ext. Ref.*
			50 typ.				ppm/°C	Int. Ref.*
	ZN502E	Parameter values as for ZN502CJ						
	All types							
Resolution		10	–	–	–	–	bits	
Conversion time (min)		10	15	20	15	20	μs	Note 2
DAC reference I_{ref}		0.25	0.5	1.0	0.25	1.0	mA	Note 5
Nominal analogue input range		−2.5	–	+2.5	–	–	V	Note 3
Supply rejection		–	0.1	–	–	–	% per V	
Supply voltage $+V_{CC}$		+4.5	+5	+5.5	+4.5	+5.5	V	
$-V_{CC}$		−4.5	−5	−5.5	−4.5	−5.5	V	
Supply current $+I_{CC}$		–	30	40	–	–	mA	$+V_{CC}$ = +5V
$-I_{CC}$		–	21	28	–	–	mA	$-V_{CC}$ = −5V
Power consumption		–	255	340	–	–	mW	
INTERNAL VOLTAGE REFERENCE								
Output voltage	All types	–	2.480	–	–	–	V	
Output voltage tolerance	ZN501AJ	–	–	±3.0	–	–	%	
	ZN502CJ	–	–	±5.0	–	–	%	
	ZN502E	–	–	±5.0	–	–	%	
V_{REF} temp. coeff.	All types	–	–	–	26	50	ppm/°C	
Slope impedance		–	0.75	–	–	–	Ω	
Max. load current		–	±2.0	–	–	–	mA	
LOGIC	All types							
$\overline{\text{START CONVERT}}$ $\overline{\text{SC}}$								
High level inpV V_{ih}		2.0	–	–	2.0	–	V	
Low level inpV V_{il}		–	–	0.8	–	0.8	V	
High level inpl I_{ih}		–	18.0	–	–	–	μA	V_{CC} = ±5.5V V_{in} = 5.5V
High level inpl I_{ih}		–	8.0	–	–	–	μA	V_{CC} ±5.5V V_{in} = 2.4V
Low level inpl I_{il}		–	4.0	–	–	–	μA	V_{CC} ±5.5V V_{in} +0.4V

*See note 4

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	Version	$T_{amb} = +25°C$ Min.	Typ.	Max.	Over Spec Min.	Max.	Units	Conditions
LOGIC	All types							
$\overline{BYTE}$ 1 and 2								
High level inpV V_{ih}		2.0	–	–	2.0	–	V	
Low level inpV V_{il}		–	–	0.8	–	0.8	V	
High level inpI I_{ih}		–	18.0	–	–	–	μA	$V_{CC} = \pm 5.5V$ $V_{in} = 5.5V$
High level inpI I_{ih}		–	12.0	–	–	–	μA	$V_{CC} = \pm 5.5V$ $V_{in} = 2.4V$
Low level inpI I_{il}		–	2.0	–	–	–	μA	$V_{CC} = \pm 5.5V$ $V_{in} = 0.4V$
CLOCK	All types							
CLOCK high period		0.5	–	–	–	–	μs	
Max. clock frequency		550	730	1100	550	730	KHz	
High level inpV V_{ih}		2.0	–	–	2.0	–	V	
Low level inpV V_{il}		–	–	0.8	–	0.8	V	
High level inpI I_{ih}		–	15.0	–	–	–	μA	$V_{CC} = \pm 5.5V$ $V_{in} = 5.5V$
High level inpI I_{ih}		–	5.0	–	–	–	μA	$V_{CC} = \pm 5.5V$ $V_{in} = 2.4V$
Low level inpI I_{il}		–	3.0	–	–	–	μA	$V_{CC} = \pm 5.5V$ $V_{in} = 0.4V$
High level OPV V_{oh}	All types	2.4	–	–	2.4	–	V	$V_{CC} = \pm 5V$
Low level OPV V_{ol}		–	–	0.4	–	0.4	V	
High level OPI I_{oh}		–	–	−700	–	–	μA	
Low level OPI I_{ol}		–	–	2.0	–	–	mA	
Three-state DISABLE output leakage		–	–	±2.0	–	–	μA	$V_{out} = 1.3V$
$\overline{BYTE}$ input to data output delays		–	200	260	–	–	ns	
ENABLE/DISABLE								
Delay time TE1		100	220	260	–	–	ns	Note 6
TEO		60	80	100	–	–	ns	
TD1		100	120	140	–	–	ns	
TDO		30	60	100	–	–	ns	
$\overline{SC}$ pulse width		100	–	–	–	–	ns	
$\overline{SC}$ input to STATUS		–	180	–	–	–	ns	

Note 1 No missing codes over full temperature range at appropriate accuracy.

Note 2 The maximum conversion time is 20μs. This corresponds to a clock rate of 550KHz based on 11 clock periods per conversion cycle (see timing diagram). This provides an update rate of 50KHz.

Note 3 Single polarity and other input ranges may be provided by different input resistor values.

Note 4 Gain error is trimmable to zero with the aid of R3.

Note 5 The full scale D-A output current $I_{out} = 4$ times I_{ref}. For optimum performance $I_{ref} = 0.5mA$.

Note 6 Refer to Fig. 9.

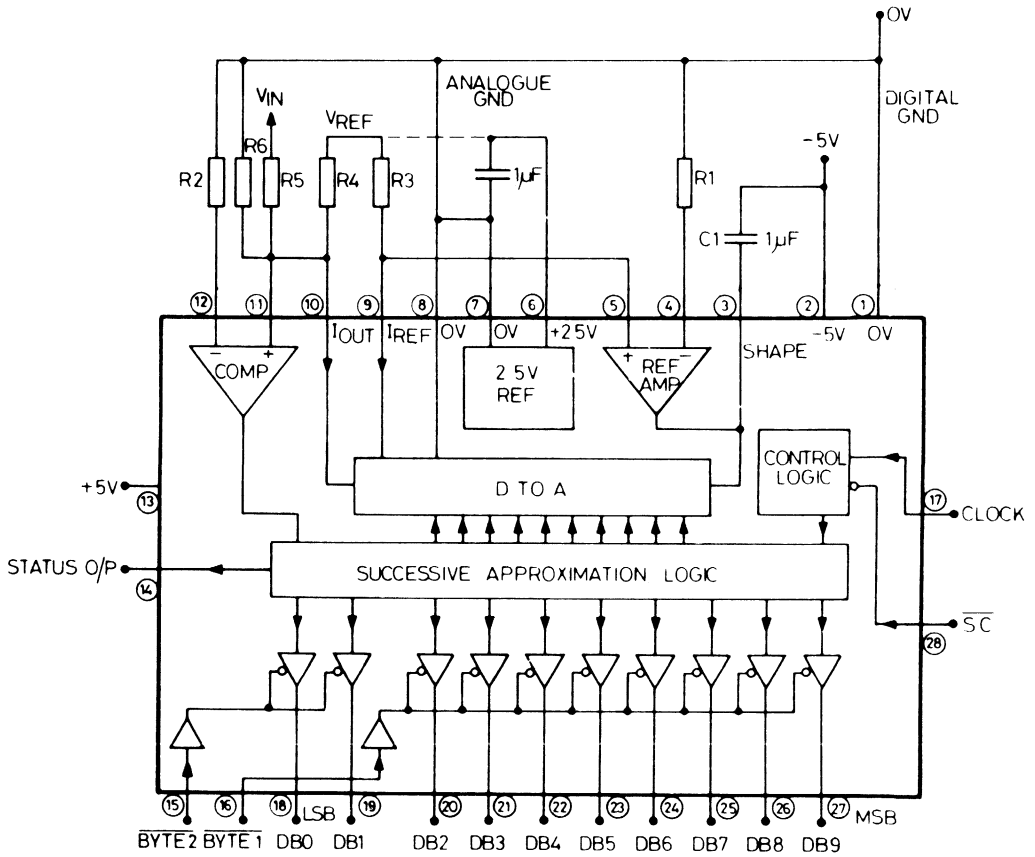


Fig. 2 Typical external components

GENERAL CIRCUIT OPERATION

The ZN501 utilises the successive approximation technique. Upon receipt of a negative-going pulse at the $\overline{SC}$ input the STATUS output goes low, and the D-A converter input is set to the MSB. The resulting analogue output is compared with the unknown analogue input signal by means of the comparator. So if the analogue input is the larger, the MSB is left in circuit and if not the MSB is removed. On the second clock pulse this sequence is repeated for the next most significant bit and so on until all the 10-bits have been compared. On the 11th negative clock edge STATUS goes high indicating that the conversion is complete.

During a conversion $\overline{BYTE}$ 1 and $\overline{BYTE}$ 2 will normally be held high to keep the 3-state buffers in their high impedance state. Data can be read out by taking either $\overline{BYTE}$ 1 or $\overline{BYTE}$ 2 low, thus enabling the three-state outputs. $\overline{BYTE}$ 1 controls the 8 MSB's and $\overline{BYTE}$ 2 controls the 2 LSB's. Readout is non-destructive.

CONVERSION TIMING

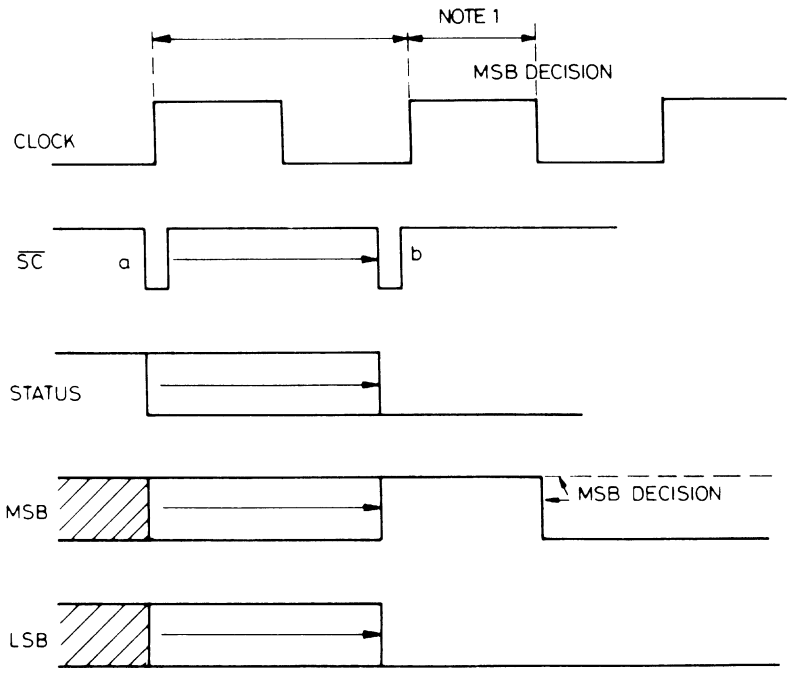
The ZN501 will accept a low-going $\overline{\text{START CONVERT}}$ pulse, which can be completely asynchronous with respect to the clock, and will produce valid data between 10.5 and 11.5 clock pulses later depending on the relative timing of the CLOCK and $\overline{\text{START CONVERT}}$ signals.

The converter is cleared by a low-going $\overline{\text{START CONVERT}}$ pulse, which sets the most significant bit and resets all the other bits and STATUS. Whilst the $\overline{\text{START CONVERT}}$ input is low the MSB output of the D-A converter is continuously compared with the analogue input, but otherwise the converter is inhibited. After the $\overline{\text{START CONVERT}}$ input goes high again the MSB decision is made and the successive approximation routine runs to completion.

The $\overline{\text{SC}}$ pulse can be as short as 100ns; however the MSB must be allowed to settle for at least (625ns) before the MSB decision is made. To ensure that this criterion is met even with short $\overline{\text{SC}}$ pulses the converter waits, after the $\overline{\text{SC}}$ input goes high, for a rising clock edge followed by a falling clock edge, the MSB decision being taken on the falling clock edge. This ensures that the MSB is allowed to settle for at least half a clock period, or (625ns) at maximum clock frequency. The clock high period and the $\overline{\text{SC}}$ pulse width must comply with this settling time i.e. clock high period + $\overline{\text{SC}}$ pulse width $\geqslant$625ns.

During a conversion the $\overline{\text{SC}}$ input is not locked out and if it is pulsed low at any time the conversion will restart.

At the end of a conversion STATUS waits 1 clock cycle before going high, so indicating that data is valid. The data outputs can be thus enabled anytime during a conversion and valid data will be available on the rising edge of the STATUS signal.



(Expanded inset)

Fig. 3 Expanded timing diagram

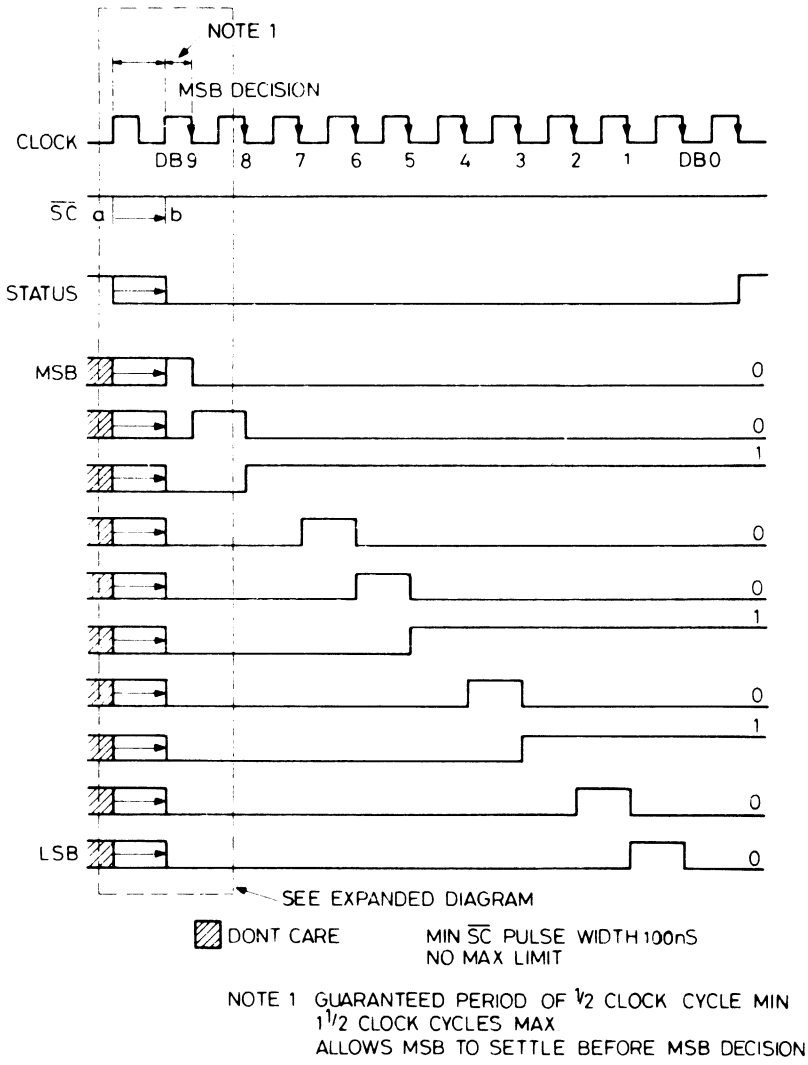


Fig. 4 Timing diagram

CONTINUOUS CONVERSION

The converter can be made to cycle by inverting the STATUS output and feeding back to the $\overline{SC}$ input. To ensure that the converter starts reliably after power up an initial start pulse is required. This can be ensured by using a NOR gate instead of an inverter and feeding it with a positive going pulse which can be derived from a simple RC network that gives a single pulse when power is applied.

The propagation delay of the NOR gate determines the period over which STATUS remains high, during which time the data can be stored into latches. The time available for storing the data can be increased by inserting delays into the inverter path.

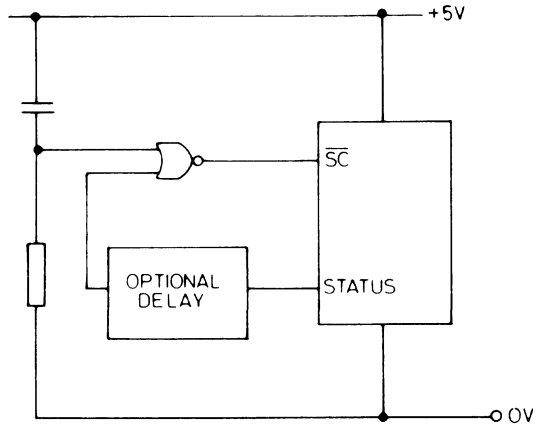


Fig. 5 Circuit for continuous conversion

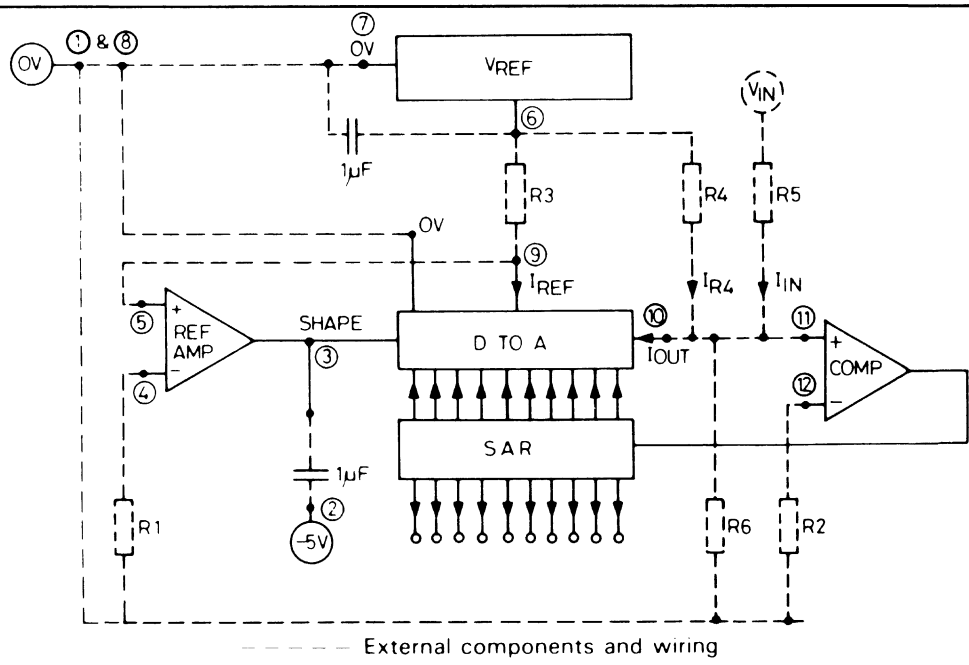


Fig. 6 External component connections

CALCULATION OF EXTERNAL RESISTORS

If $V_{in\ max}$ is the voltage for the logic output to be all 1's.

$V_{in\ min}$ is the voltage for the logic output to be all 0's.

$$I_{out} = I_{R4} + I_{in}$$

$$I_{out} = \frac{V_{ref}}{R4} + \frac{V_{in}}{R5}$$

$I_{out} = 0$ (When $V_{in} = V_{in\ min}$)

$$\frac{V_{in\ min}}{R5} = -\frac{V_{ref}}{R4}$$

$$R4 = -\frac{V_{ref}\ R5}{V_{in\ min}}$$

I_{out}(f.s.) = 2mA: (When $V_{in} = V_{in\ max}$)

$$\frac{V_{in\ max}}{R5} + \frac{V_{ref}}{R4} = I_{out}(f.s.)$$

$$-\frac{V_{in\ min}}{R5} + \frac{V_{in\ max}}{R5} = I_{out}(f.s.)$$

$$R5 = \frac{V_{in\ max} - V_{in\ min}}{I_{out}(f.s.)}$$

It is important for gain stability that I_{out}(f.s.) of 2mA be kept constant, and this is done by the reference amplifier loop.

The current sources in the D-A itself cannot be checked directly so a number of reference current sources are distributed across the chip to monitor conditions all along the array.

$$\text{So } I_{ref} = 0.5\text{mA}$$

$$R3 = \frac{V_{ref}}{0.5\text{mA}}$$

I_{out}(f.s.) is four times I_{ref}.

R3 can affect gain stability and thus requires to be of high quality.
(Also slight variation in its value can act as a gain control).

R4 and R5 can affect offset stability and thus requires to be of high quality.
(Also slight variations in the value of R4 can act as an offset control).

R1 and R2 supply the bias currents of the reference amplifier and comparator.

$$\text{So } R1 = R3$$

and R2 = parallel combination of R4, R5 and R6

R6 should be chosen such that the parallel combination of R4, R5 and R6 is about 1.25KΩ as this determines the D-A time constant and hence conversion time.

(THE FOLLOWING IS A TABLE OF VALUES TO GIVE EXAMPLES OF THE ABOVE EQUATIONS):

$V_{in\ max}$	$V_{in\ min}$	V_{ref}	R1 (1)	R2 (1)	R3	R4	R5	R6 (1)
+ 2.5	2.5	2.5	5K	1.25K	5K	2.5K	2.5K	∞
+ 2.5	2.5	5*	10K	1.25K	10K	5.0K	2.5K	5.0K
+ 2.5	0	2.5	5K	1.25K	5K	∞	1.25K	∞
+ 5.0	0	2.5	5K	1.25K	5K	∞	2.5K	2.5K
+ 4.0	2.0	2.5	5K	1.25K	5K	3.75K	3.0K	5.0K
+ 4.0	2.0	12*	24K	1.25K	24K	3.75K	3.0K	5.0K
+ 10	10	2.5	5K	1.25K	5K	2.5K	10K	3.33K
+ 10	0	2.5	5K	1.25K	5K	∞	5K	1.66K

Note 1 Nearest prefered value may be used for R1, R2 and R6

*Note 2 External reference

For unipolar operation where R4 approaches (∞) and a zero adjustment is required, the following offset circuit is suggested in place of R4.

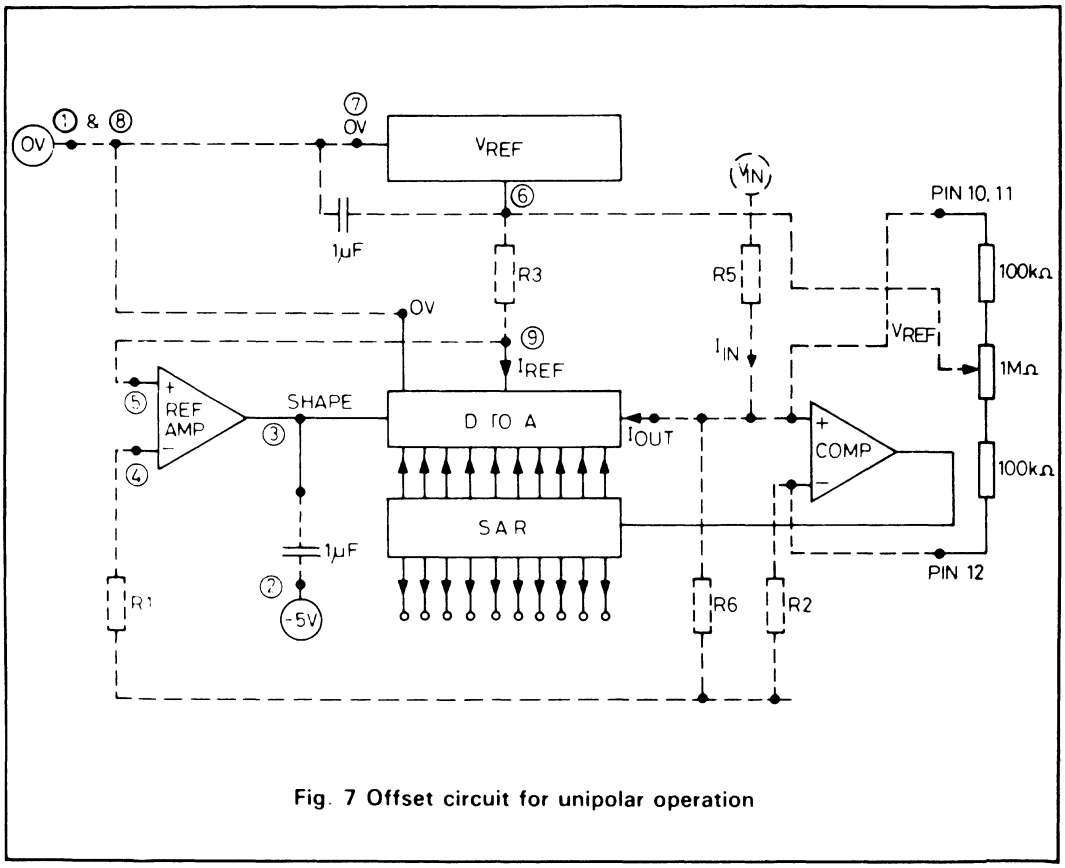


Fig. 7 Offset circuit for unipolar operation

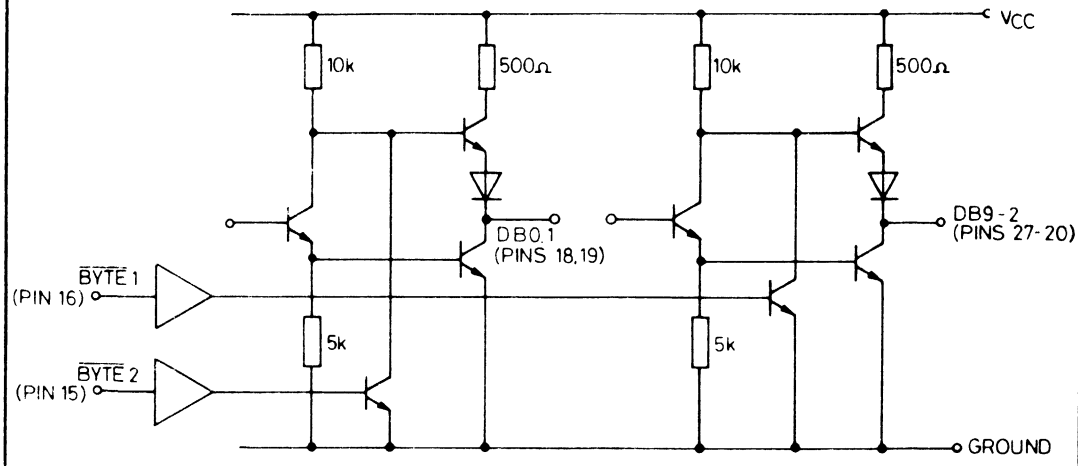
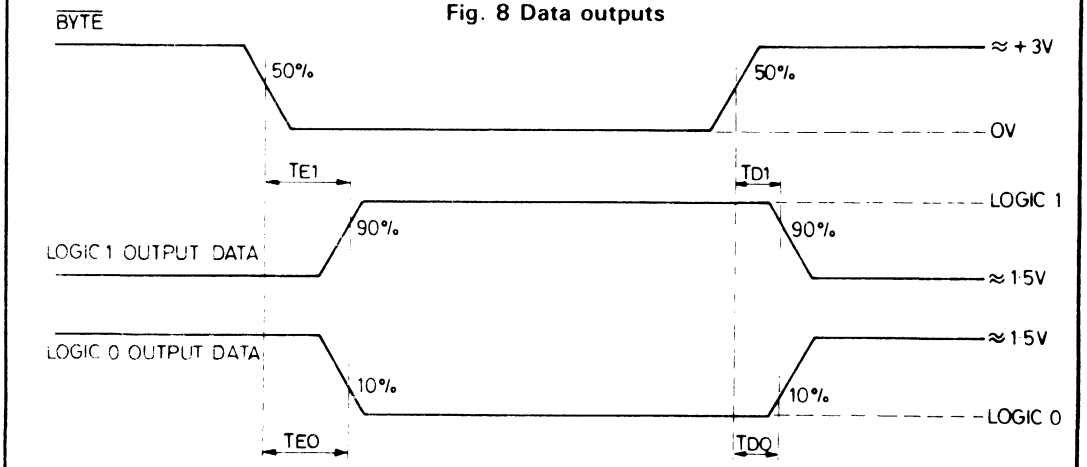


Fig. 8 Data outputs



TE = BYTE ENABLE DELAY TIME (CL = 50pF)
TD = BYTE DISABLE DELAY TIME (CL = 10pF)

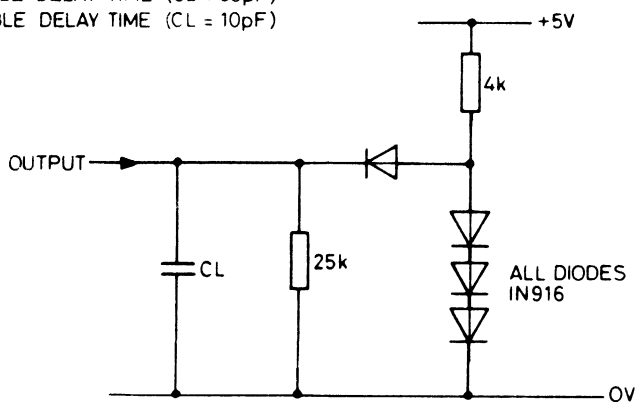


Fig. 9 Output enable/disable delays

DATA OUTPUTS

The ZN501 has true three-state output buffers on chip, hence eliminating the need for external buffers and latch circuitry.

The two $\overline{\text{BYTE}}$ select pins $\overline{\text{BYTE}}$ 1 and $\overline{\text{BYTE}}$ 2, control outputs DB9 to DB2, and outputs DB1 to DB0 respectively.

$\overline{\text{BYTE}}$ 1 and $\overline{\text{BYTE}}$ 2 will normally be held high during a conversion to keep the three-state buffers in their high impedance state, and when data is ready, which will be signalled by a high going STATUS pulse, it can easily be read out by taking $\overline{\text{BYTE}}$ 1 and $\overline{\text{BYTE}}$ 2 low.

(A test circuit and timing diagram for the output enable/disable delays are given).

The STATUS output shown utilises a 5K internal pullup resistor for CMOS/TTL compatibility.

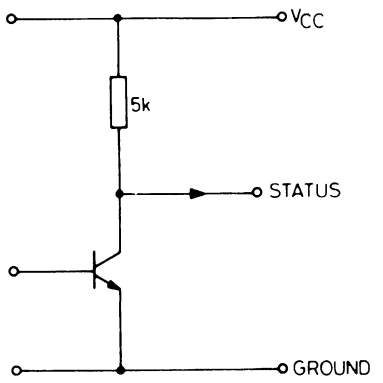


Fig. 10 Status output

DATA BUS CONNECTIONS

The ZN501 can be connected directly to an 8-bit microprocessor bus, where the two LSB's would normally be hardwired to the desired upper bits, usually the 2 MSB's. Hence the data would be transferred in two words with control of them, from $\overline{\text{BYTE}}$ 1 and $\overline{\text{BYTE}}$ 2.

For use with a 16-bit microprocessor, $\overline{\text{BYTE}}$ 1 and $\overline{\text{BYTE}}$ 2 would be tied together and all 10 bits would be enabled simultaneously. The 10-bit word could then be placed at either the higher or lower end of the 16-bit bus.

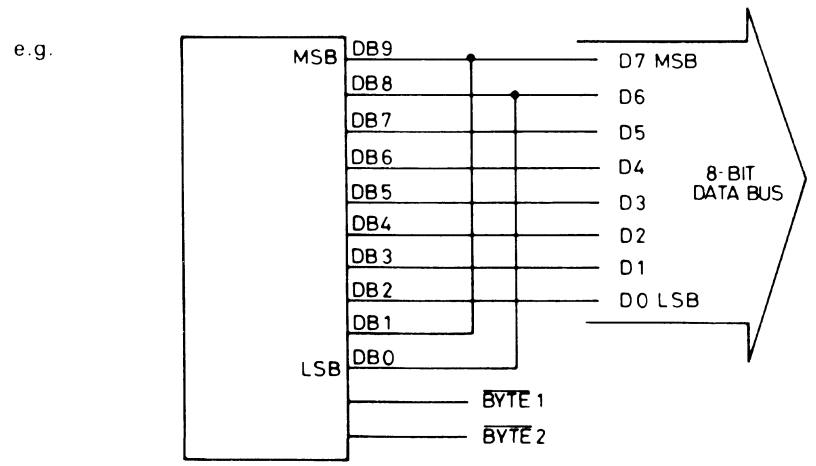


Fig. 11 Data bus connections

$\overline{BYTE}$ 1	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2
	D7	D6	D5	D4	D3	D2	D1	D0
$\overline{BYTE}$ 2	DB1	DB0	X	X	X	X	X	X

DATA TRANSFERRED IN TWO WORDS

UNIPOLAR ADJUSTMENT PROCEDURE

(i) Apply continuous $\overline{START\ CONVERT}$ pulse at intervals long enough to allow a complete conversion and monitor the digital outputs.

OFFSET SETTING

(ii) Apply ½LSB to V_{in} and adjust the offset CIRCUIT until DBO (LSB) just flickers between 0 and 1 with all the other bits at 0.
i.e. for transition 0000000000 to 0000000001.

GAIN SETTING

(iii) Apply full-scale minus 1.½LSB to V_{in} and adjust gain until DBO (LSB) just flickers between 0 and 1 with all other bits at 1.
i.e. for transition 1111111111 to 1111111110.

Note: R3 GAIN ADJUSTMENT.

UNIPOLAR SETTING-UP POINTS

Input range +FS	½LSB	F.S. – 1.½LSB
+2.5V	1.22mV	2.4963V
+5.0V	2.441mV	4.9926V

$1LSB = \frac{FS}{1024}$

UNIPOLAR LOGIC CODING

Analogue input (Nominal code centre value)	Digital output code MSB LSB
FS - 1LSB	1111111111
FS - 2LSB	1111111110
¾.FS	1100000000
½.FS + LSB	1000000001
½.FS	1000000000
½.FS - 1LSB	0111111111
¼.FS	0100000000
1LSB	0000000001
0	0000000000

BIPOLAR ADJUSTMENT PROCEDURE

(i) Apply continuous $\overline{\text{START CONVERT}}$ pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

OFFSET SETTING

(ii) Apply −(FS − ½.LSB) to V_{in} and adjust offset control until DBO (LSB) output just flickers between 0 and 1 with all other bits at 0.
i.e. for transistions 0000000000 to 0000000001.

Note: R4 OFFSET ADJUSTMENT.

GAIN SETTING

(iii) Apply +(FS − 1½.LSB) to V_{in} and adjust gain until DBO (LSB) just flickers between 0 and 1 with all other bits at 0.
i.e. for transition 1111111111 to 1111111110.

Note: R3 GAIN ADJUSTMENT.

BIPOLAR SETTING-UP POINTS

Input range ±FS	−(FS − ½.LSB)	+(F.S. − 1.½.LSB)
±2.5V	−2.4976V	+2.4927V
±5.0V	−4.9951V	+4.9854V

$$1LSB = \frac{2FS}{1024}$$

BIPOLAR LOGIC CODING

Analogue input (Nominal code centre value)	Digital output code MSB LSB
+(FS − 1LSB)	1111111111
+(FS − 2LSB)	1111111110
+(½.FS)	1100000000
+(1LSB)	1000000001
0	1000000000
−(1LSB)	0111111111
−(½.FS)	0100000000
−(FS − 1LSB)	0000000001
−FS	0000000000

PLESSEY
Semiconductors

ZN503AJ/ZN504CJ/ZN504E

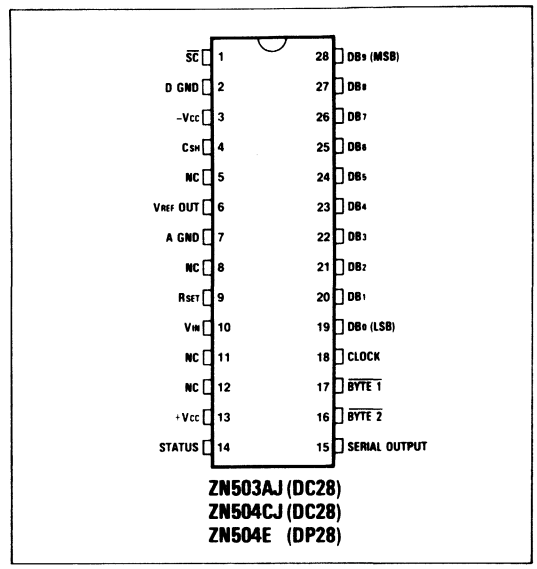
10-BIT MICROPROCESSOR-COMPATIBLE A-D CONVERTERS WITH PARALLEL/SERIAL OUTPUT

The ZN503/4 range of fast successive approximation A-D converters combine several innovations on a monolithic silicon integrated circuit. This 28 pin device consists of a current switching array (requiring no trim), successive approximation logic, 2.5V precision reference, reference amplifier, comparator and 3-state parallel and serial output buffers.

The ZN503/4 has 3 pin-programmable input ranges and only two external components are required to perform a full 10-bit A-D conversion. No user trims ae required and the provision of a serial output makes the device ideal for high resolution remote sensing applications.

FEATURES

- Choice of Linearity: ½ LSB - ZN503
  1 LSB - ZN504
- 15 microseconds Typical, 20 microseconds Guaranteed Conversion Time
- 3-State Parallel and Serial Outputs
- Only 2 External Components Required
- 3 Pin-Programmable Input Ranges
- Asynchronous $\overline{\text{START CONVERT}}$ Pulse
- Microprocessor, TTL and CMOS Compatible
- Full 8 or 16-Bit Micro-Bus Interface
- Available in 28 Pin Moulded or Ceramic DIL



ZN503AJ (DC28)
ZN504CJ (DC28)
ZN504E (DP28)

Pin connections - top view

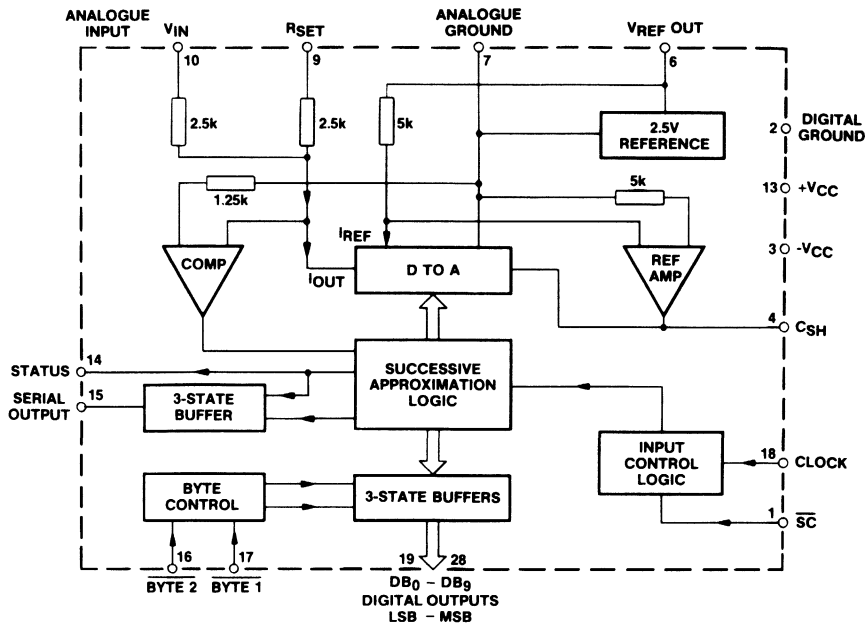


Fig.1 System diagram

ORDERING INFORMATION

Device type	Operating temperature	Package
ZN504E	0°C to +70°C	DP28
ZN504CJ	0°C to +70°C	DC28
ZN503AJ	-55°C to +125°C	DC28

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC+}	+7V
Supply voltage V_{CC-}	-7V
Logic input voltage	+V_{CC} and 0V
Operating temperature range	0°C to +70°C (ZN504E, ZN504CJ) -55°C to +125°C (ZN503AJ)
Storage temperature range	-55°C to +125°C

ELECTRICAL CHARACTERISTICS (at +5 and −5V supplies and internal reference unless otherwise specified).

		T_{amb} = +25°C			Over spec.			
Parameter	Version	Min.	Typ.	Max.	Min.	Max.	Units	Conditions
	ZN503AJ							
Linearity error		–	–	±0.5	–	±0.5	LSB	
Diff. linearity error		–	–	±0.5	–	±0.5	LSB	Note 1
Unipolar offset		–	±1.0	±2.0	–	±2.0	LSB	Note 2
Bipolar offset		–	±1.0	±2.0	–	±2.0	LSB	Note 2
Gain error		–	±4.0	–	–	–	LSB	Note 2
TEMPERATURE COEFFICIENTS (T_{min} to T_{max})								
Unipolar offset			10 typ., 15 max.				ppm/°C	
Bipolar offset			10 typ., 15 max.				ppm/°C	
Gain			60 typ.				ppm/°C	
	ZN504CJ							
Linearity error		–	–	±1.0	–	±1.0	LSB	
Diff. linearity error		–	–	±0.75	–	±0.75	LSB	Note 1
Unipolar offset		–	±1.0	±2.0	–	±2.0	LSB	Note 2
Bipolar offset		–	±1.0	±2.0	–	±2.0	LSB	Note 2
Gain error		–	±4.0	±6.0	–	–	LSB	Note 2
TEMPERATURE COEFFICIENTS (T_{min} to T_{max})								
Unipolar offset			20 typ., 30 max.				ppm/°C	Note 2
Bipolar offset			20 typ., 30 max.				ppm/°C	Note 2
Gain			60 typ.				ppm/°C	Note 2
	ZN504E		Parameter values as for ZN504CJ					
	All types							
Resolution		10	–	–	–	–	bits	
Conversion time (min)		10	15	20	15	20	μs	Note 4

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	Version	T_{amb} = +25°C			Over spec		Units	Conditions
		Min.	Typ.	Max.	Min.	Max.		
Nominal analogue input ranges	All types		0 to +2.5				V	Note 5, 8
			0 to +5.0				V	Note 6, 8
			−2.5 to +2.5				V	Note 7, 8
Supply rejection		−	0.1	−	−	−	% per V	
Supply voltage $+V_{CC}$		+4.5	+5.0	+5.5	+4.5	+5.5	V	
$-V_{CC}$		−4.5	−5.0	−5.5	−4.5	−5.5	V	
Supply current $+I_{CC}$		−	36	44	−	−	mA	$+V_{CC}$ = +5V
$-I_{CC}$		−	23	32	−	−	mA	$-V_{CC}$ = −5V
Power consumption		−	295	380	−	−	mW	
INTERNAL VOLTAGE REFERENCE								
Output voltage	All types	−	2.480	−	−	−	V	
Output voltage tolerance	ZN503AJ	−	−	±3.0	−	−	%	
	ZN504CJ	−	−	±3.0	−	−	%	
	ZN504E	−	−	±5.0	−	−	%	
V_{REF} temp. coeff.	All types	−	−	−	26	50	ppm/°C	
Slope impedance		−	0.75	−	−	−	Ω	
Max. ext. load current		−	±2.0	−	−	−	mA	
LOGIC $\overline{\text{START CONVERT}}$ $\overline{\text{SC}}$	All types							
High level input voltage		2.0	−	−	2.0	−	V	
Low level input voltage		−	−	0.8	−	0.8	V	
High level input current		−	18	−	−	−	μA	V_{CC} = ±5.5V V_{in} = 5.5V
High level input current		−	8.0	−	−	−	μA	V_{CC} = ±5.5V V_{in} = 2.4V
Low level input current		−	4.0	−	−	−	μA	V_{CC} = ±5.5V V_{in} + 0.4V
LOGIC $\overline{\text{BYTE}}$ 1 and 2	All types							
High level input voltage		2.0	−	−	2.0	−	V	
Low level input voltage		−	−	0.8	−	0.8	V	
High level input current		−	18	−	−	−	μA	V_{CC} = ±5.5V V_{in} = 5.5V
High level input current		−	12	−	−	−	μA	V_{CC} = ±5.5V V_{in} = 2.4V
Low level input current		−	2.0	−	−	−	μA	V_{CC} = ±5.5V V_{in} = 0.4V

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	Version	T_{amb} = +25°C			Over spec.		Units	Conditions
		Min.	Typ.	Max.	Min.	Max.		
CLOCK	All types							
CLOCK high period		0.5	–	–	–	–	μs	
Max. clock frequency		550	730	1100	550	730	KHz	
High level input voltage		2.0	–	–	2.0	–	V	
Low level input voltage		–	–	0.8	–	0.8	V	
High level input current		–	15	–	–	–	μA	V_{CC} = ±5.5V V_{in} = 5.5V
High level input current		–	5.0	–	–	–	μA	V_{CC} = ±5.5V V_{in} = 2.4V
Low level input current		–	1.5	–	–	–	μA	V_{CC} = ±5.5V V_{in} = 0.4V
DATA OUTPUTS								
High level output voltage	All types	2.4	–	–	2.4	–	V	I_{OH} = −700μA
Low level output voltage		–	–	0.4	–	0.4	V	I_{OL} = 2mA
High level output current		–	–	−700	–	–	μA	V_{OH} = 2.4V
Low level output current		–	–	2.0	–	–	mA	V_{OL} = 0.4V
3-state DISABLE output leakage		–	–	±2.0	–	–	μA	V_{out} = 1.3V
ENABLE/DISABLE								
Delay time TE1		100	220	260	–	–	ns	Note 3
TEO		60	80	100	–	–	ns	
TD1		100	120	140	–	–	ns	
TDO		30	60	100	–	–	ns	
$\overline{SC}$ pulse width		100	–	–	–	–	ns	
$\overline{SC}$ input to STATUS		–	180	–	–	–	ns	
STATUS OUTPUT								
High level O/P Voltage		2.4	–	–	–	–	V	I_{OH} = 40μA
Low level O/P Voltage		–	–	0.4	–	–	V	I_{OL} = 1.6mA
High level O/P current		–	–	−350	–	–	μA	V_{OH} = 2.4V
Low level O/P current		–	–	1.6	–	–	mA	V_{OL} = 0.4V

Note 1 No missing codes over full temperature range at appropriate accuracy.

Note 2 No user trims are available for either zero or gain error.

Note 3 Refer to Fig. 9.

Note 4 The maximum conversion time is 20μs. This corresponds to a clock rate of 550KHz based on 11 clock periods per conversion cycle (see Fig. 4). This provides an update rate of 50KHz.

Note 5 R_{set} (pin 9) connected to analogue input (pin 10).

Note 6 R_{set} (pin 9) connected to analogue ground (pin 7).

Note 7 R_{set} (pin 9) connected to $V_{REF\ OUT}$ (pin 6).

Note 8 The scaling resistors used to define the 3 analogue input ranges are fabricated on-chip to improve thermal tracking. These resistors are accurately matched but each has an absolute tolerance of typically ±30%.

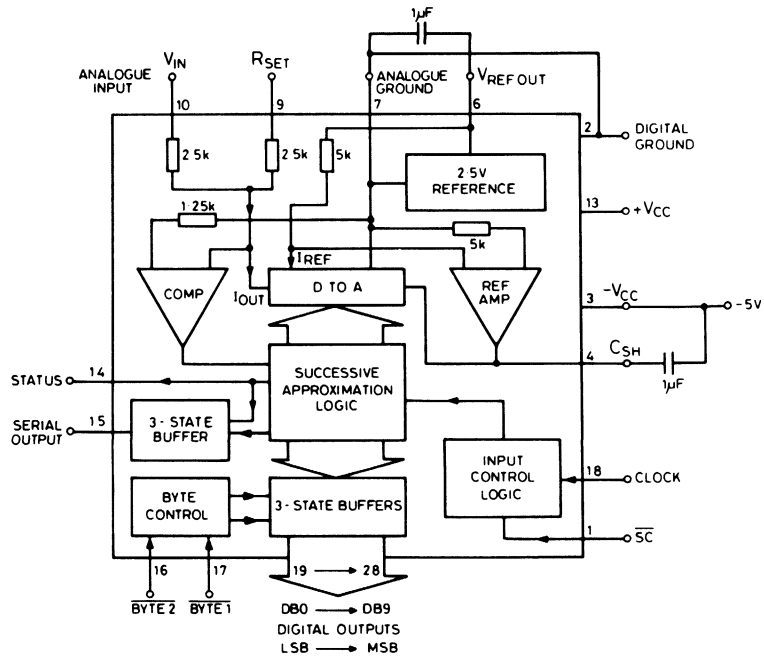


Fig. 2 Typical external components

GENERAL CIRCUIT OPERATION

The ZN503/4 utilises the successive approximation technique. Upon receipt of a negative-going pulse at the $\overline{SC}$ input the STATUS output goes low, and the D-A converter input is set to the MSB. The resulting analogue output is compared with the unknown analogue input signal by means of the comparator. If the analogue input is the larger, the MSB is left in circuit and if not the MSB is removed. On the second clock pulse this sequence is repeated for the next most significant bit and so on until all the 10-bits have been compared. On the 11th negative clock edge STATUS goes high indicating that the conversion is complete and that the data is valid.

Parallel and serial outputs

The ZN503/4 is micro-bus compatible with the 3-state parallel output buffers enabled by two byte control pins. During a conversion $\overline{BYTE}$ 1 and $\overline{BYTE}$ 2 will normally be held high to keep the 3-state buffers in their high impedance state. At the end of conversion STATUS returns high and data can be read out by taking either $\overline{BYTE}$ 1 and/or $\overline{BYTE}$ 2 low thus enabling the appropriate data outputs. $\overline{BYTE}$ 1 controls the 8 MSB's and $\overline{BYTE}$ 2 the 2 LSB's. Readout is non-destructive.

The serial output operates in a different manner in that its 3-state output buffer is enabled when STATUS is low, i.e. during a conversion. Data appears at the serial output after each bit decision and is valid at the subsequent positive edges of the clock.

CONVERSION TIMING

Parallel output

The ZN503/4 will accept a low-going $\overline{\text{START CONVERT}}$ pulse, which can be completely asynchronous with respect to the clock and will produce valid data between 10.5 and 11.5 clock pulses later depending on the relative timing of the CLOCK and $\overline{\text{START CONVERT}}$ signals.

The converter is cleared by a low-going $\overline{\text{START CONVERT}}$ pulse, which sets the most significant bit and resets all the other bits and STATUS. Whilst the $\overline{\text{START CONVERT}}$ input is low the MSB output of the D-A converter is continuously compared with the analogue input, but otherwise the converter is inhibited. After the $\overline{\text{START CONVERT}}$ input goes high again the MSB decision is made and the successive approximation routine runs to completion.

The $\overline{\text{SC}}$ pulse can be as short as 100ns; however the MSB must be allowed to settle for at least 625ns before the MSB decision is made. To ensure that this criterion is met even with short $\overline{\text{SC}}$ pulses the converter waits, after the $\overline{\text{SC}}$ input goes high, for a rising clock edge followed by a falling clock edge, the MSB decision being taken on the falling clock edge. This ensures that the MSB is allowed to settle for at least half a clock period, or 625ns at maximum clock frequency. The clock high period and the $\overline{\text{SC}}$ pulse width must comply with this settling time i.e. clock high period + $\overline{\text{SC}}$ pulse width $\geqslant$ 625ns.

During a conversion the $\overline{\text{SC}}$ input is not locked out and if it is pulsed low at any time the conversion will restart.

At the end of a conversion STATUS waits 1 clock cycle before going high, so indicating that data is valid. The data outputs can thus be enabled anytime during a conversion and valid data will be available on the rising edge of the STATUS signal.

Serial output

The serial output will remain in a high impedance state until a low going $\overline{\text{START CONVERT}}$ pulse is received, which can be completely asynchronous with respect to the clock. On the negative edge of this pulse the STATUS output goes low indicating to the user that the conversion has commenced. Whilst the $\overline{\text{START CONVERT}}$ is held low, the serial output will remain in an indeterminate state and the converter will be inhibited. Once the $\overline{\text{START CONVERT}}$ input returns high the MSB decision is made between ½ and 1½ clock periods later. The serial output data is then available on positive edges of the clock, beginning with the MSB. Once the LSB decision has been made, the output returns to a high impedance state on the next negative edge of the clock, which is indicated by the STATUS output going high. The conversion takes between 10.5 and 11.5 clock periods depending on the relative timing of the CLOCK and $\overline{\text{START CONVERT}}$ pulses.

Serial data can easily be transferred into a 10-bit shift register on positive going clock edges after the STATUS signal has gone low. If the STATUS output is used to gate the clock to the shift register, it would contain all 10-bits of valid data after the STATUS returns high. A typical circuit diagram is shown in Fig. 3.

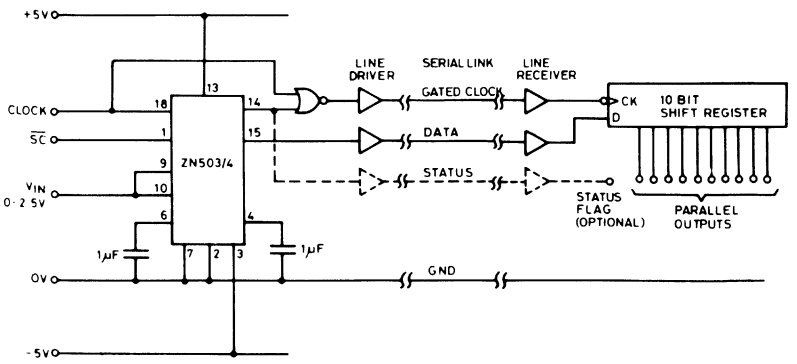


Fig. 3 A typical application of the serial output

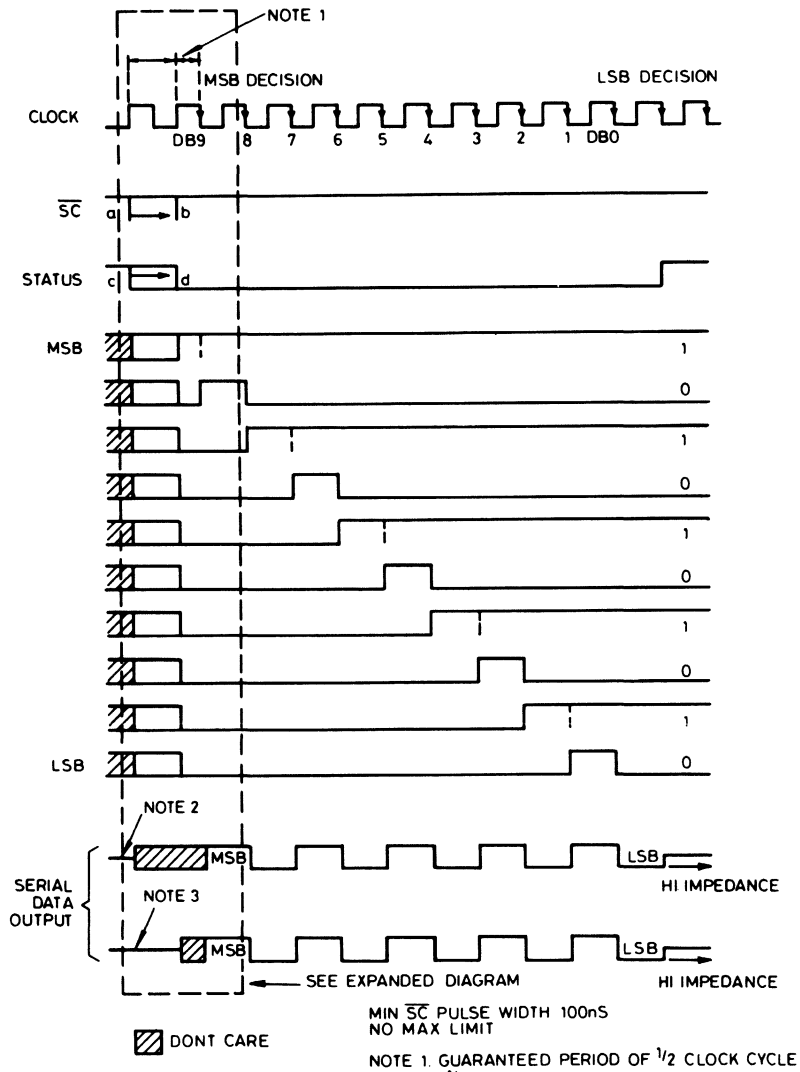


Fig. 4 Timing diagram

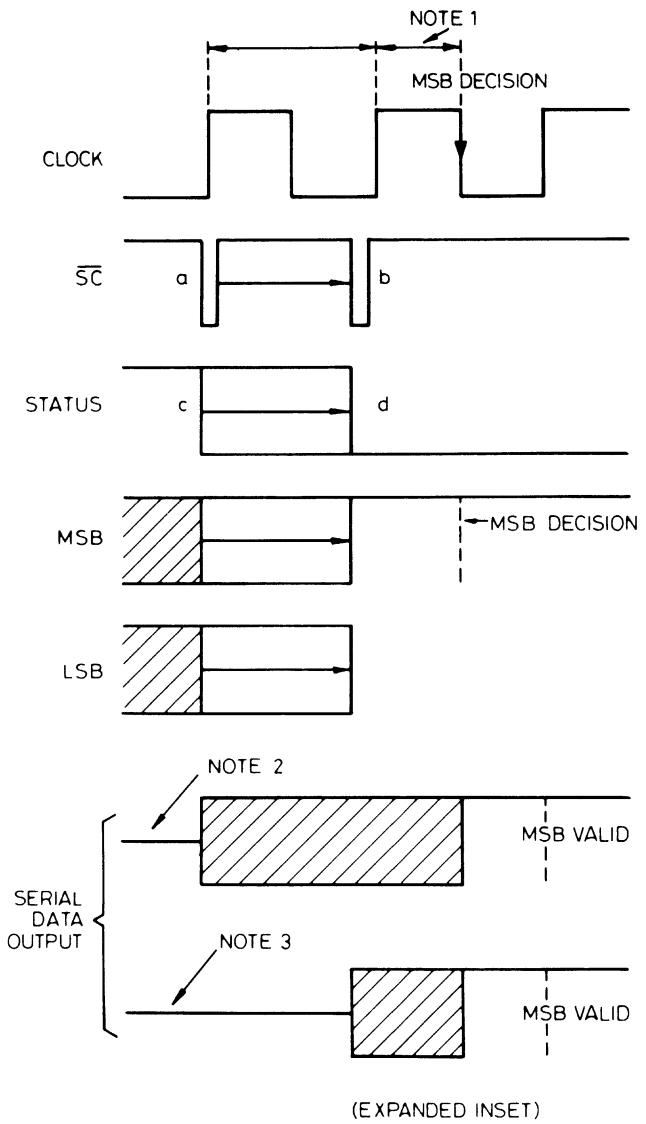


Fig. 5 Expanded timing diagram

CONTINUOUS CONVERSION

The converter can be made to cycle by inverting the STATUS output and feeding it back into the $\overline{SC}$ input. To ensure that the converter starts reliably after power up an initial start pulse is required. This can be ensured by using a NOR gate rather than of an inverter and feeding it with a positive going pulse which can be derived from a simple RC network that gives a single pulse when power is applied.

The propagation delay of the NOR gate determines the period over which STATUS remains high, during which time the data can be stored into latches. The time available for storing the data can be increased by inserting delays into the inverter path.

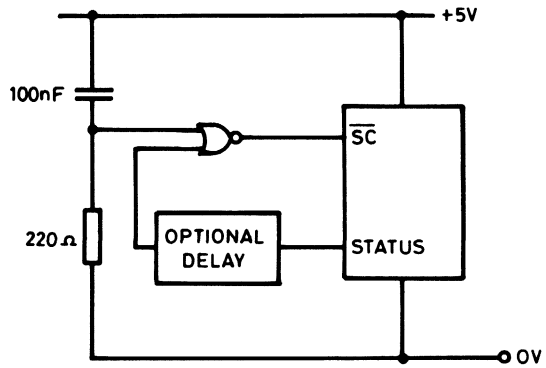


Fig. 6 Circuit for continuous conversion

PARALLEL DATA OUTPUTS

The ZN503/4 has true 3-state output buffers on-chip, hence eliminating the need for external buffers and latch circuitry.

The two byte select pins $\overline{BYTE}$ 1 and $\overline{BYTE}$ 2, control outputs DB9 to DB2, and outputs DB1 to DB0 respectively.

$\overline{BYTE}$ 1 and $\overline{BYTE}$ 2 will normally be held high during a conversion to keep the 3-state buffers in their high impedance state, and when data is ready, which will be signalled by a high going STATUS pulse, it can easily be read out by taking $\overline{BYTE}$ 1 and $\overline{BYTE}$ 2 low.

(A test circuit and timing diagram for the output enable/disable delays are given).

The STATUS output shown utilises a 5K internal pullup resistor for CMOS/TTL compatibility.

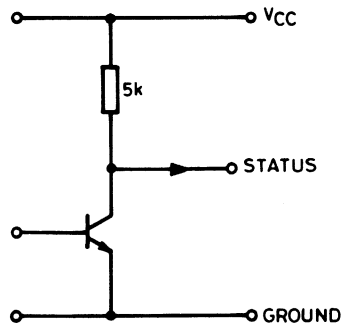


Fig. 7 Status output

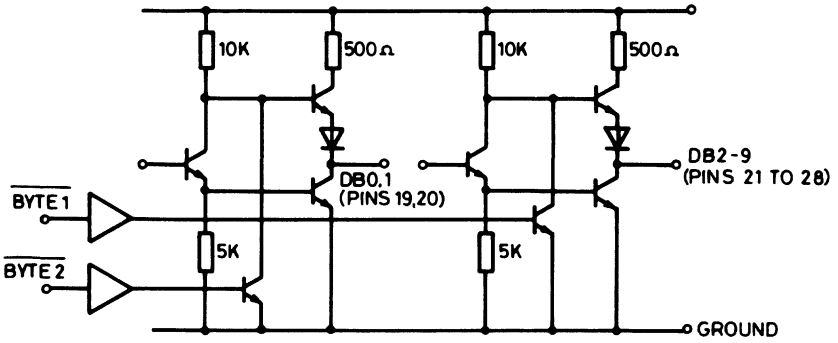
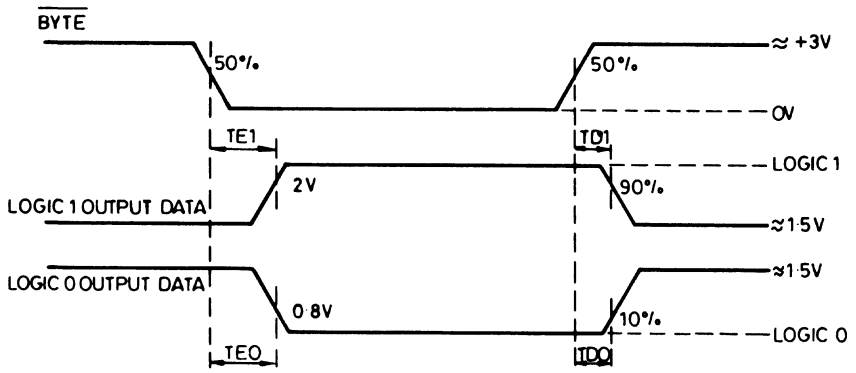


Fig. 8 Data outputs



TE = BYTE ENABLE DELAY TIME (CL = 50pF)
TD = BYTE DISABLE DELAY TIME (CL = 10pF)

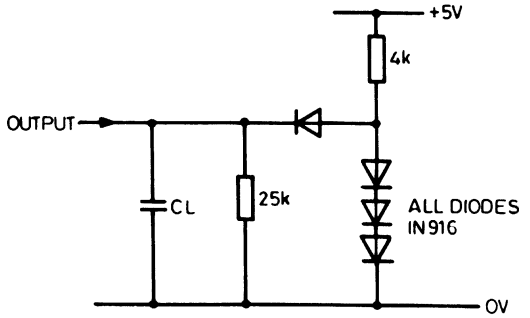


Fig. 9 Output enable/disable delays

DATA BUS CONNECTIONS

The ZN503/4 can be connected directly to an 8-bit microprocessor bus, where the two LSB's would normally be hardwired to the desired upper bits, usually the 2 MSB's. Hence the data would be transferred in two words with control of them, from $\overline{\text{BYTE}}$ 1 and $\overline{\text{BYTE}}$ 2.

For use with a 16-bit microprocessor, $\overline{\text{BYTE}}$ 1 and $\overline{\text{BYTE}}$ 2 would be tied together and all 10 bits would be enabled simultaneously. The 10-bit word could then be placed at either the higher or lower end of the 16-bit bus.

e.g.

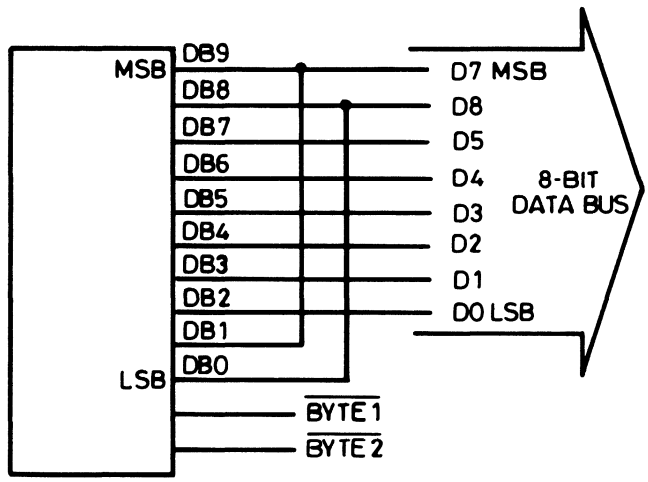


Fig. 10 8-bit data bus connections

$\overline{\text{BYTE}}$ 1

DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2
D7	D6	D5	D4	D3	D2	D1	D0

$\overline{\text{BYTE}}$ 2

DB1	DB0	X	X	X	X	X	X

DATA TRANSFERRED IN TWO WORDS

UNIPOLAR INPUT RANGES

V_{in} = 0 to +2.5V. R_{SET} (Pin9) connected to A_{in} (Pin10)

V_{in} = 0 to +5V. R_{SET} (Pin9) connected to A_{GND} (Pin7)

UNIPOLAR LOGIC CODING

Analogue input (Nominal code centre value)	Digital output code MSB LSB
FS - 1LSB	1111111111
FS - 2LSB	1111111110
¾.FS	1100000000
½.FS + LSB	1000000001
½.FS	1000000000
½.FS - 1LSB	0111111111
¼.FS	0100000000
1LSB	0000000001
0	0000000000

BIPOLAR INPUT RANGE

V_{in} = -2.5 to +2.5V. R_{SET} (Pin9) connected to $V_{REF\ OUT}$ (Pin6)

BIPOLAR LOGIC CODING

Analogue input (Nominal code centre value)	Digital output code MSB LSB
+(FS - 1LSB)	1111111111
+(FS - 2LSB)	1111111110
+(½.FS)	1100000000
+(1LSB)	1000000001
0	1000000000
-(1LSB)	0111111111
-(½.FS)	0100000000
-(FS - 1LSB)	0000000001
-FS	0000000000

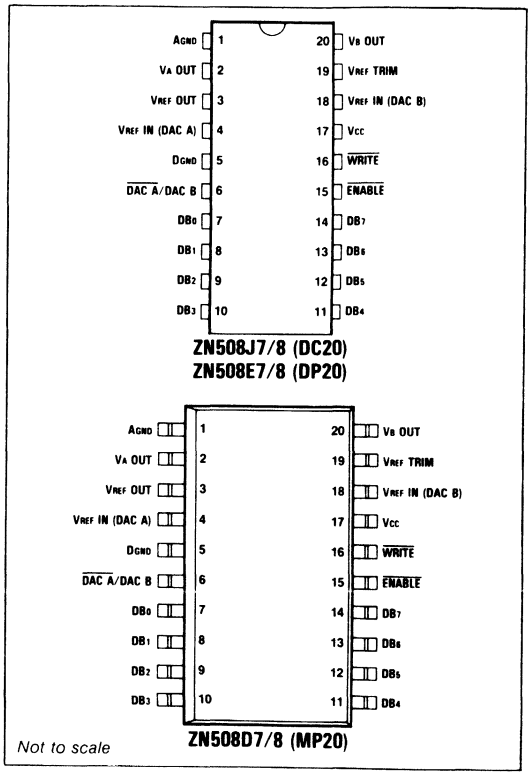
ZN508

DUAL 8-BIT MICROPROCESSOR COMPATIBLE D-A CONVERTER

The ZN508 is a monolithic dual 8-bit DAC designed to be easily interfaced to microprocessors. Integrated on-chip are two 8-bit DAC's, a 2.5V trimmable bandgap reference, separate V_{REF} inputs and data latches for each DAC. The on-chip reference not only can be used to drive the two DAC's but can be also used as a system reference. A consequence of the two DAC's being fabricated on the same chip is excellent, inherent, DAC to DAC matching.

FEATURES

- 800ns Voltge Settling Time
- 2.5V Trimmable Bandgap Reference
- Monotonic over Full Temperature Range
- Single +5V Supply
- Excellent DAC to DAC Matching
- Separate V_{REF} IN for each DAC
- Commerical and Military Temperature Ranges



Pin connections - top view

ORDERING INFORMATION

Device type	Linearity error (LSB)	Operating temperature	Package
ZN508E7	±1	-40°C to +85°C	DP20
ZN508E8	±½	-40°C to +85°C	DP20
ZN508D7	±1	-40°C to +85°C	MP20
ZN508D8	±½	-40°C to +85°C	MP20
ZN508J7	±1	-55°C to +125°C	DC20
ZN508J8	±½	-55°C to +125°C	DC20

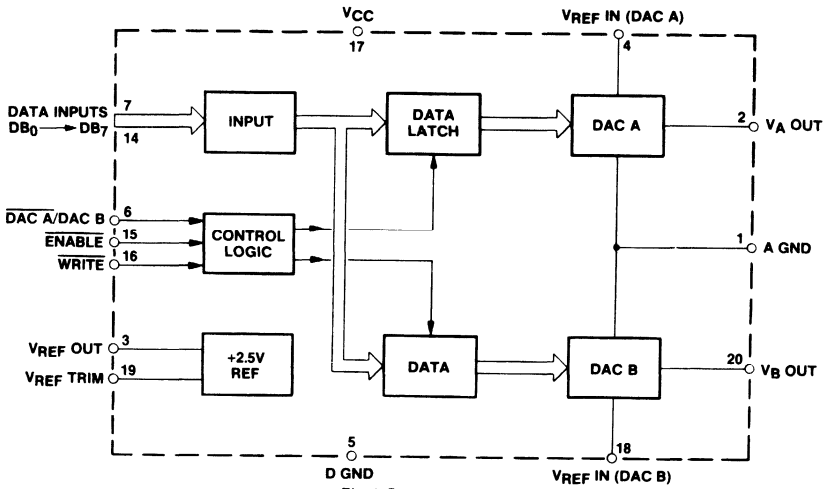


Fig.1 System diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	+7V	ZN508J	-55°C to 125°C
Max. voltage, logic and V_{REF} input	$+V_{CC}$	Storage temperature range	-55°C to 125°C
Operating temperture range		Analog ground to digital ground	±200mV
ZN508E and ZN508D	-40°C to +85°C		

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
ZN508-8					
Linearity error			±0.5	LSB	
Differential linearity error			±0.75	LSB	
ZN508-7					
Linearity error			±1.0	LSB	
Differential linearity error			±1.0	LSB	
All types					
Linearity error TC		±3		ppm/°C	
Differential non-linearity TC		±6		ppm/°C	
Offset voltage ZN508E		2	5	mV	All bits OFF
ZN508D		2	5	mV	All bits OFF
ZN508J		2	5	mV	All bits OFF
Offset voltage TC		±3		ppm/°C	
Full scale output	2.545	2.550	2.555	V	External reference V_{REF} IN = 2.560V, all bits ON
Full scale output TC		2		ppm/°C	
Analog output resistance		4		kΩ	
External reference voltage	0		3.0	V	
Settling time to 0.5 LSB		800		ns	1 LSB major transition (Note 1)
		1.25		µs	All bits ON to OFF or OFF to ON (Note 1)
Supply voltage (V_{CC})	4.5	5.0	5.5	V	
Supply current		36		mA	
Power consumption		180		mW	
DC supply rejection		-57		dB	ΔV_{CC} = 250µV p-p f ≤ 50kHz
Digital to analog glitch impulse				nV-s	00000000 11111111
Channel to channel isolation					
$V_{REF\ A}$ to Out B		-82		dB	f ≤ 50kHz
$V_{REF\ B}$ to Out A		-82		dB	f ≤ 50kHz
Internal voltage reference					
Output voltage		2.5		V	
Slope impedance		1		Ω	
V_{REF} OUT TC		50		ppm/°C	
Reference current	1		15	mA	
Logic					
(over specified operating temperature range)					
High level input voltage V_{IH}	2.0			V	
Low level input voltage V_{IL}			0.8	V	
High level input current I_{IH}			20	µA	V_{IN} = 2.4, V_{CC} = 5.5V
			320	µA	V_{IN} = 5.5, V_{CC} = 5.5V
Low level input current I_{IL}			-310	µA	V_{IN} = 0.4V, V_{CC} = 5.5V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Switching characteristics					
Chip select to write set up time t_{CS}	150			ns	
Chip select to write hold time, T_{CH}	10			ns	
DAC select to write set up time t_{AS}	150			ns	
DAC select to write hold time t_{AH}	10			ns	
Data valid to write set up time t_{DS}	100			ns	
Data valid to write hold time t_{DH}	50			ns	
Write pulse width t_{WR}	150			ns	

NOTE
1. R_L = 10 Megohms C_L = 10pF.

D-A CONVERTER

The converters are of the voltage switching type and use an R-2R ladder network as shown in Fig.2. Each 2R element is connected to 0V or V_{REF} IN by transistor voltage switches specially designed for low offset voltage (<1mV). A binary weighted voltage is produced at the output of the R-2R ladder.

Analog output $= \frac{n}{256} (V_{REF}\ IN - V_{OS}) + V_{OS}$

where n is the digital input to the D-A from the data latch.

V_{OS} is a small offset voltage produced by the D-A switch currents flowing through the package lead resistance. The value of V_{OS} is typically 1mV. This offset will normally be removed by the setting up procedure (see Operating Notes) and because the offset temperature coefficient is low ($\pm 6\mu V/°C$) the effect on accuracy is negligible.

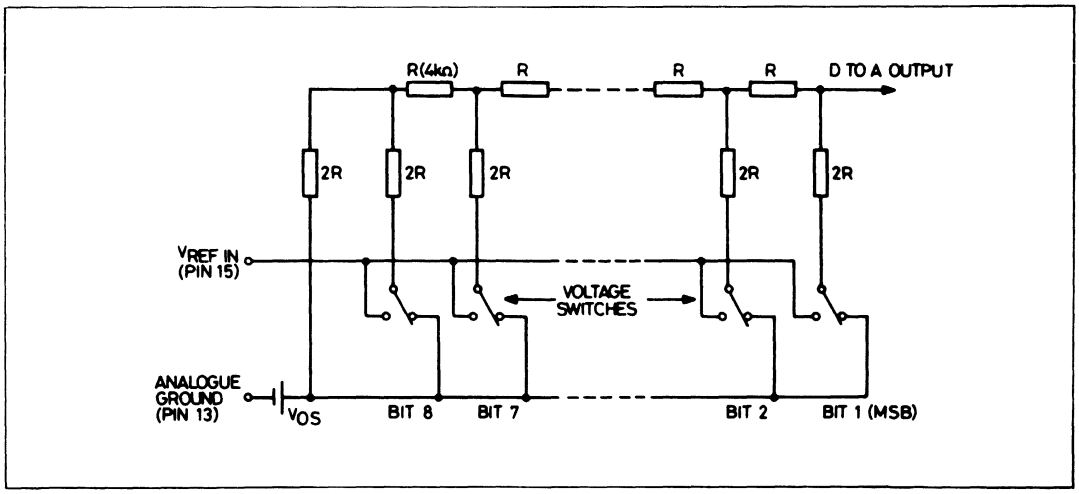


Fig.2 The R-2R ladder network

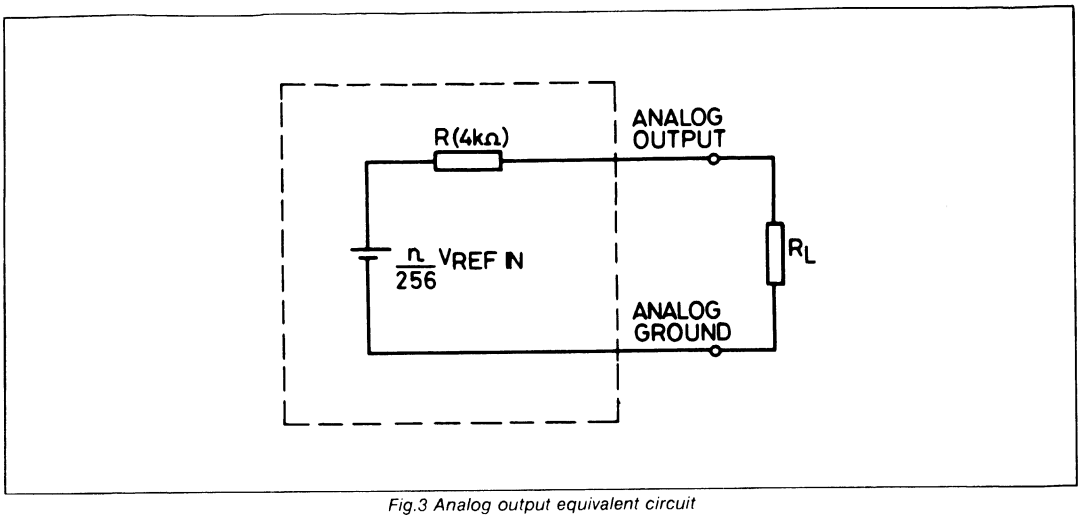


Fig.3 Analog output equivalent circuit

Fig.3 shows an equivalent circuit of the outputs (ignoring V_{OS}). The output resistance R has a temperature coefficient of +0.2% per °C.
The gain drift due to this is $\frac{0.2R}{R + R_L}$ % per °C

R_L should be chosen to be as large as possible to make the gain drift small. As an example if R_L = 400kΩ then the gain drift due to the TC of R for a 100°C change in ambient temperature will be less than 0.2%. Alternatively the ZN508 outputs can be buffered by amplifiers (see Operating Notes).

REFERENCE

1. Internal Reference

The internal reference is an active band gap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig.3). A resistor (R_{REF}), should be connected between +V_{CC} (pin 11) and pin 15. The recommended value of 1.5k will supply a nominal reference current of (5-2.5)/1500 = 1.7mA.

The reference voltage can be trimmed by ±5% with a 10k potentiometer (as shown in Fig.5).

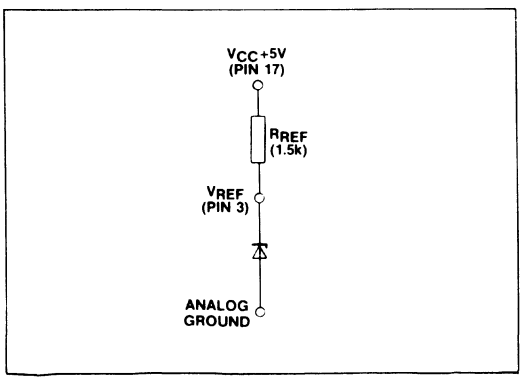


Fig.4 Internal voltage reference

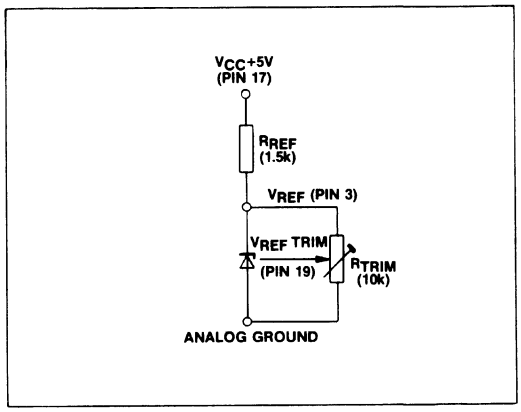


Fig.5 Trimming circuit for the voltage reference

2. External Reference

If required an external reference voltage may be connected to V_{REF} IN. The slope resistance of such a reference source should be less than $\frac{2.5\Omega}{n}$, where n is the number of converters supplied.

V_{REF} IN can be varied from 0 to +3V for ratiometric operation. The ZN508 is guaranteed monotonic for V_{REF} IN above 2V.

LOGIC

Input coding is binary for unipolar operation and offset binary for bipolar operation. Both DAC A and DAC B share an internal data bus and an 8-bit input port. The DAC to be loaded with new data is chosen by $\overline{\text{DAC A}}$/DAC B select pin; DAC A when the input is low and DAC B when the input is high. When $\overline{\text{ENABLE}}$ and $\overline{\text{WRITE}}$ are both low the DAC selected is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to the data presented to the input port. The data is then latched when either $\overline{\text{ENABLE}}$ or $\overline{\text{WRITE}}$ are taken high.

$\overline{\text{DAC A}}$/DAC B	$\overline{\text{CS}}$	$\overline{\text{WR}}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

Table 1 Logic truth table

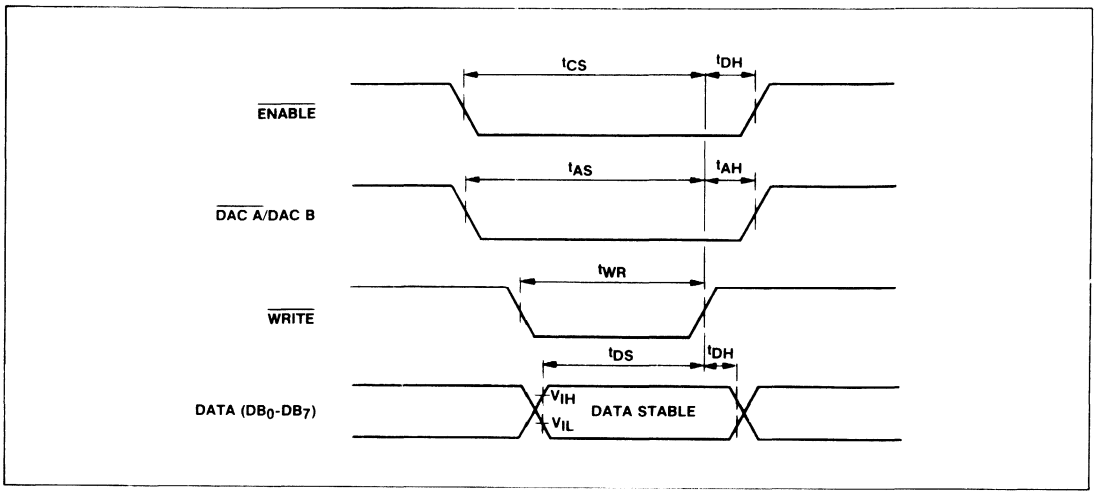


Fig.6 Logic timing diagram

OPERATING NOTES

In some applications the standard 0 to V_{REF} IN output voltage range and drive capability are not suitable, and other output ranges, both unipolar and bipolar are required.

To maintain flexibility two types of operational amplifier are illustrated; the industry standard 741 and a low cost pin-compatible alternative with a JFET input, the LF351. The LF351 features a high slew rate of 13V/μs, which gives a faster potential settling time than the 741. To keep drift to a minimum when using the 741, the external range setting resistors are calculated to match them to the 4kΩ ladder output impedance. This is not a consideration with the LF351, as the input offset current change with temperature is negligible for the impedances concerned. The resistor values for the LF351 were chosen to keep the output ringing to a minimum; a problem sometimes encountered with high slew rate op-amps. It is only the relative and not the absolute values of these resistors which set the range, and therefore can be changed as long as their ratios remain the same.

Unipolar Operation

The general scheme for unipolar operation is shown in Fig.6 and is suitable for amplifiers with input bias currents less than 1.5μA.

The resulting full scale range is given by

$$V_{OUT}\,FS = 1 + \frac{R1}{R2}\,(V_{REF}\,IN - 1\,LSB)$$

$$= G\,(V_{REF}\,IN) - 1\,LSB)$$

The impedance at the inverting input is R1/R2 and for low drift with temperature (741 only), this parallel combination should be equal to the ladder resistance (4kΩ).

The required nominal values of R1 and R2 are therefore given by R1 = 4GkΩ and R2 = 4G/(G-1)kΩ.

Using these relationships a table of nominal resistance values for R1 and R2 can be constructed for V_{REF} IN = 2.5V (Table 2). For gain setting R1 is adjusted about its nominal value. Practical circuit realisations for +5V and +10V output ranges are given in Figs. 8 and 9.

Output range	G	R1	R2
+5V	2	8kΩ	8kΩ
+10V	4	16kΩ	5.33kΩ

Table 2 Nominal values for R1 and R2

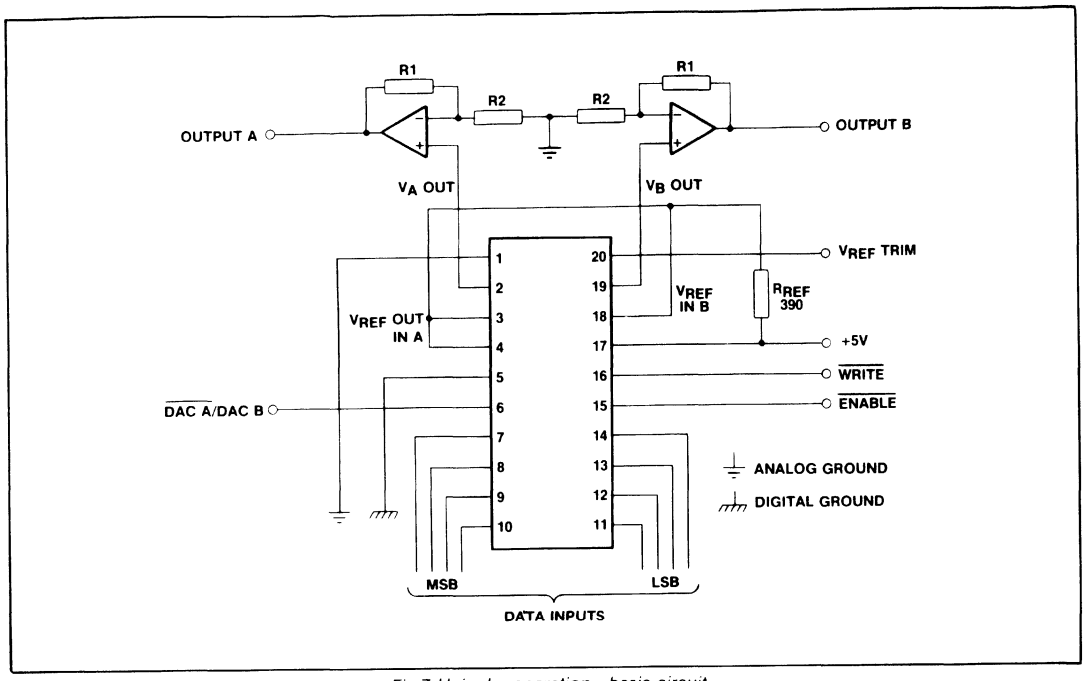


Fig.7 Unipolar operation - basic circuit

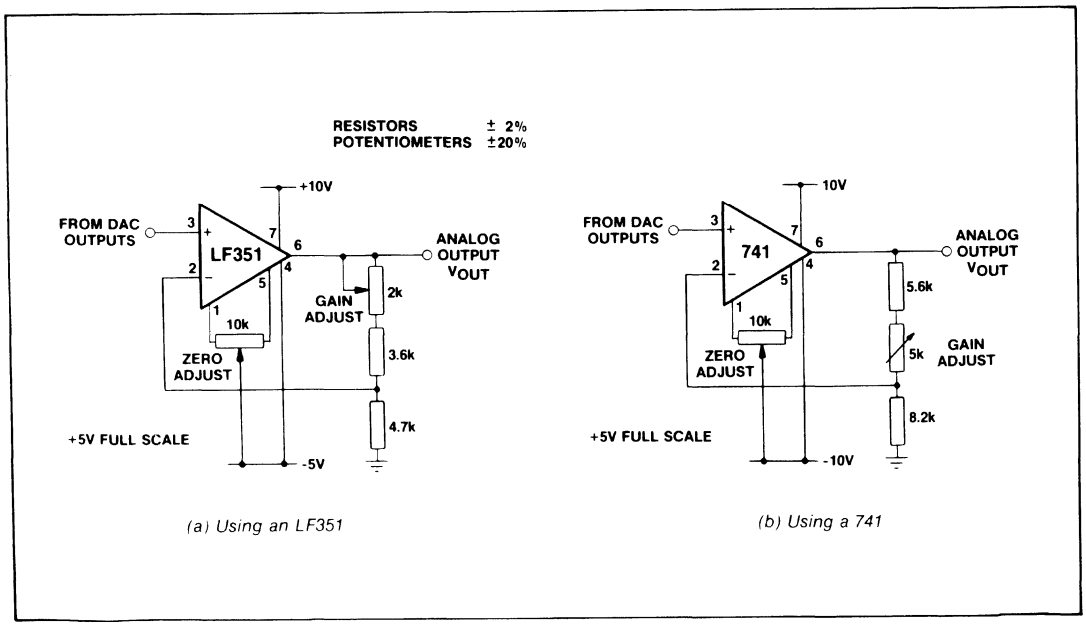
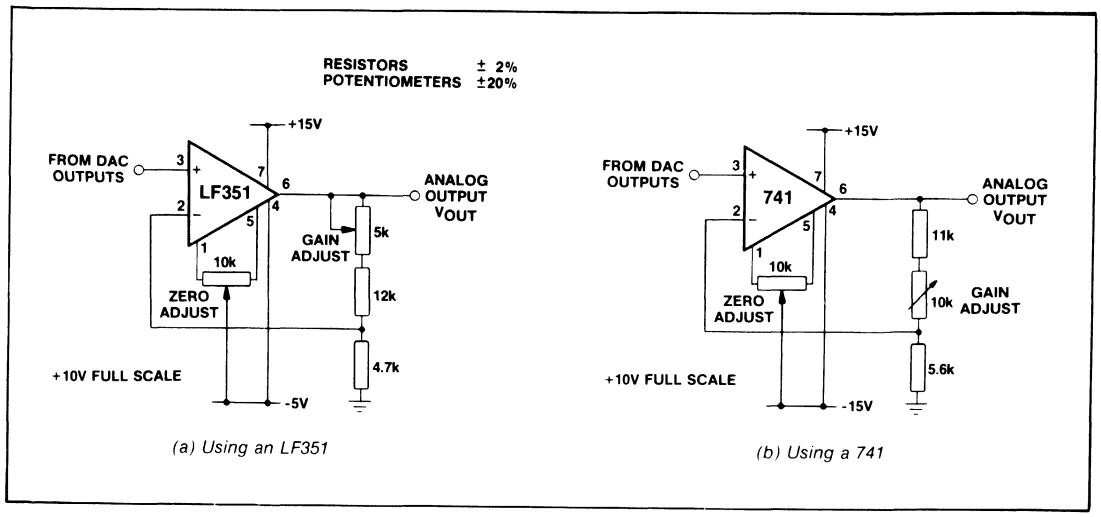


Fig.8 +5V full scale unipolar operation - component values



(a) Using an LF351 (b) Using a 741

Fig.9 +10V full scale unipolar operation - component values

Unipolar Adjustment Procedure

1. Set all bits to OFF (low) with $\overline{\text{ENABLE}}$ low and adjust zero until V_{OUT} = 0.0000V.

2. Set all bit ON (high) and adjust gain until V_{OUT} = FS - 1 LSB.

Output range, +FS	LSB	FS - 1 LSB
+5V	19.5mV	4.9805V
+10V	39.1mV	9.9609V

$1\ LSB = \frac{FS}{256}$

Table 3 Unipolar setting up points

Input code (Binary)	Analog output (nominal value)
11111111	FS - 1 LSB
11111110	FS - 2 LSB
11000000	¾ FS
10000001	½ FS + 1 LSB
10000000	½ FS
01111111	½ FS - 1 LSB
01000000	¼ FS
00000001	1 LSB
00000000	0

Table 4 Unipolar logic coding

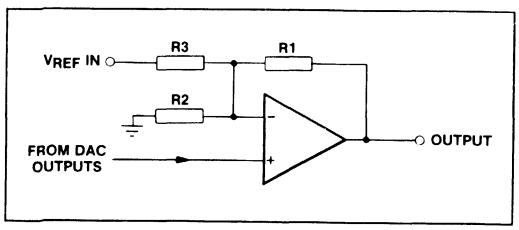


Fig.10 Bipolar operation

Bipolar Operation

For bipolar operation the output from the ZN508 is offset by half full scale by connecting a resistor R3 between V_{REF} IN and the inverting input of the buffer amplifier (Fig.10).

When the digital input to the ZN508 is zero the analog output is zero and the amplifier output should be - full scale. An input of all ones to the D-A will give a ZN508 output of V_{REF} IN - 1 LSB and an amplifier output of + full scale. When using the 741, the parallel combination of R1, R2 and R3 should match the 4kΩ ladder resistance.

The nominal values of R1, R2 and R3 which meet these conditions are given by

R1 = 8Gkω, R2 = 8G/(G-1)kω and R3 = 8kω,

where the resultant output range is ±G V_{REF} IN.

A binary output range of ± V_{REF} IN (which corresponds to the basic unipolar range 0 to V_{REF} IN) is obtained if R1 = R3 = 8kω and R2 = ∞.

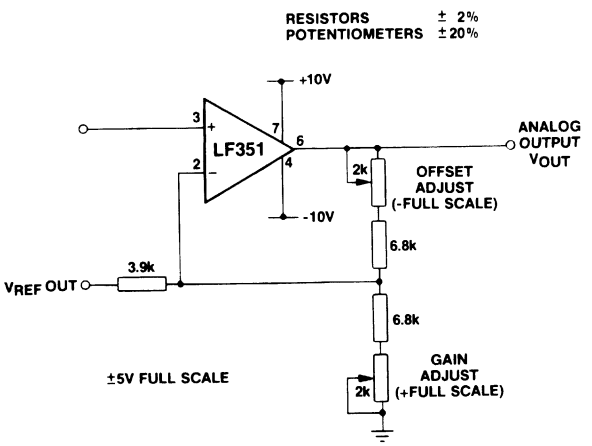
Assuming that V_{REF} IN = 2.5V the nominal values of resistors for ±5V and ±10V output ranges are given in Table 5.

Output range	G	R1	R2	R3
+5V	2	16kω	16kω	8kω
±10V	4	32kω	10.66kω	8kω

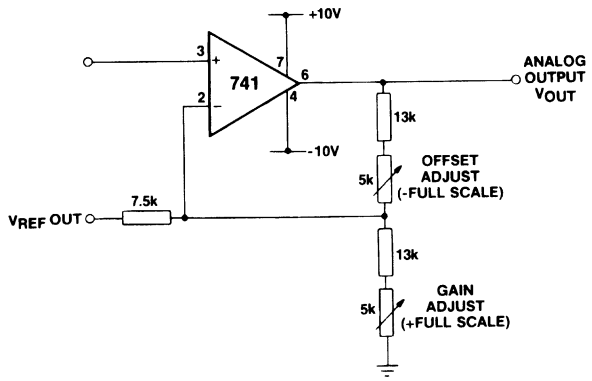
Table 5

Minus full scale (offset) is set by adjusting R1 about its nominal value relative to R3. Plus full scale (gain) is set by adjusting R2 relative to R1.

Practical circuit realisations are given in Figs. 11 and 12. Note that in the ±5V case (741 only), R3 has been chosen as 7.5kω (instead of 8.2kω) to give a more symmetrical range of adjustment using standard potentiometers.



(a) Using an LF351



(b) Using a 741

Fig. 11 ±5V full scale bipolar operation - component values

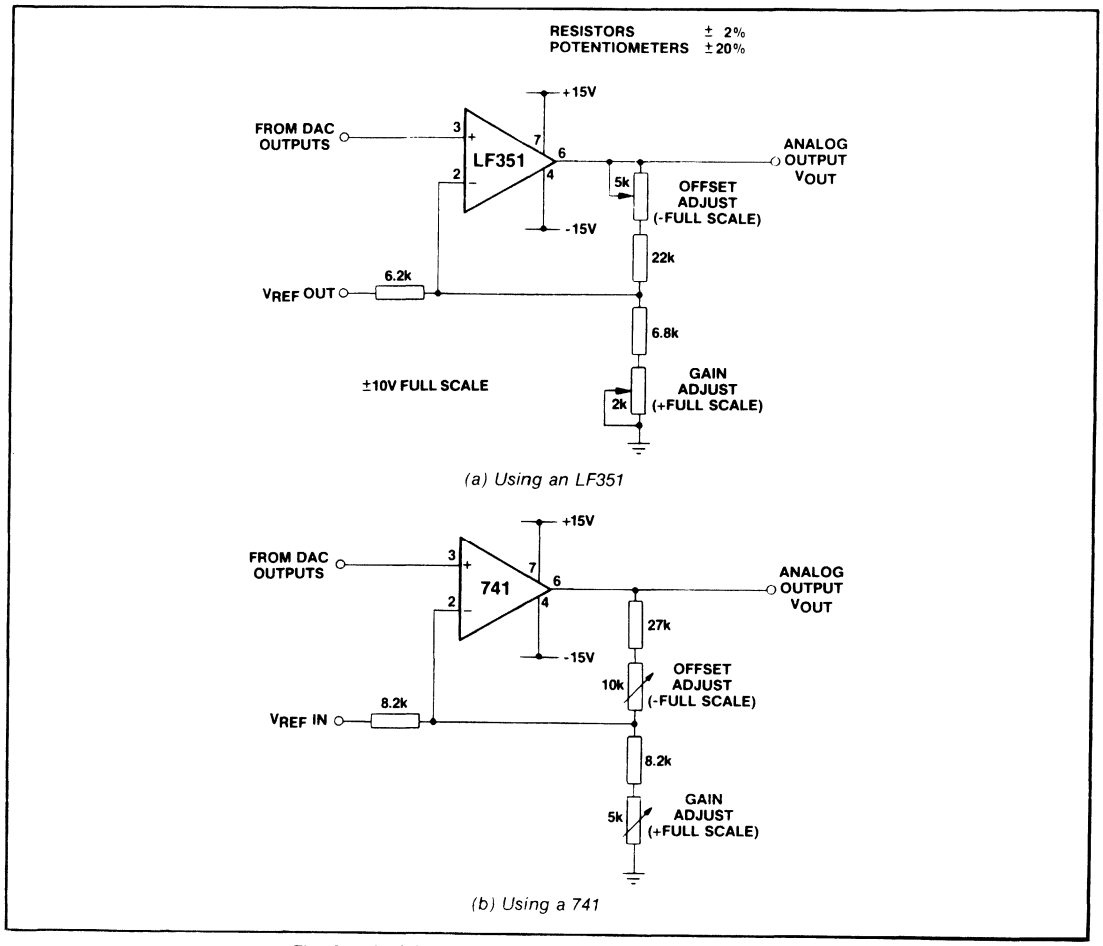


Fig.12 ±10V full scale bipolar operation - component values

Bipolar Adjustment Procedure

1. Set all bits to OFF (low) with $\overline{\text{ENABLE}}$ low and adjust offset until the amplifier output reads - full scale.

2. Set all bits ON (high) and adjust gain until the amplifier output reads + (full scale - 1 LSB).

Input range, ±FS	LSB	-FS	+(FS - 1 LSB)
±5V	39.1mV	-5.0000V	+4.9609V
±10V	78.1mV	-10.0000V	+9.9219V

$$1\ \text{LSB} = \frac{2\text{FS}}{256}$$

Table 6 Bipolar setting up points

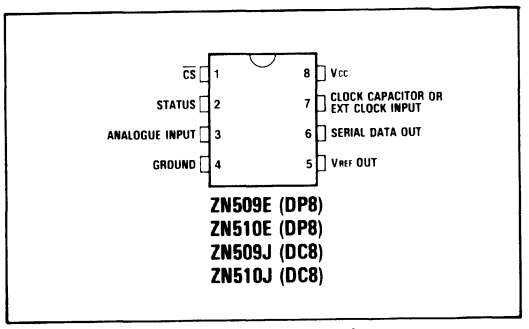
Input code (offset binary)	Analog output (nominal value)
11111111	+(FS - 1 LSB)
11111110	+(FS - 2 LSB)
11000000	+½ FS
10000001	+1 LSB
10000000	0
01111111	-1 LSB
01000000	-½ FS
00000001	-(FS - 1 LSB)
00000000	-FS

Table 7 Bipolar logic coding

ZN509/ZN510

8-BIT SERIAL A-D CONVERTER

The ZN509 and ZN510 are 8-bit serial output, successive approximation, A-D converters. Included on-chip is a clock generator which can be overdriven by an external clock, a 2.5V bandgap reference and 3-state output buffers. The devices operate from a single +5V supply and are economically packaged in an 8-pin DIL. Chip select determines the start of conversion, the conversion mode - either 'continuous' or 'single-shot' - and the 3-state control.



Pin connections - top view

FEATURES

- ½ or 1 LSB Linearity
- 8 microseconds Conversion Time
- Serial Data Output - Suitable for Remote Operation
- Easy Microprocessor Interfacing
- Equally suitable for 'Stand-Alone' Applications
- Operates from a Single +5V Supply
- On-Chip Bandgap Reference
- TTL and CMOS Compatible
- Commercial or Military Temperature Ranges

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+7.0V
Max. voltage, logic and V_{REF} inputs, A_{IN}	V_{CC}, -0.5V
Operating temperature range	
ZN509E, ZN510E	0°C to +70°C
ZN509J, ZN510J	-55°C to +125°C
Storage temperature range	-55°C to +125°C

ORDERING INFORMATION

Device type	Linearity error (LSB)	Operating temperature	Package
ZN509E	½	0°C to +70°C	DP8
ZN509J	½	-55°C to +125°C	DC8
ZN510E	1	0°C to +70°C	DP8
ZN510J	1	-55°C to +125°C	DC8

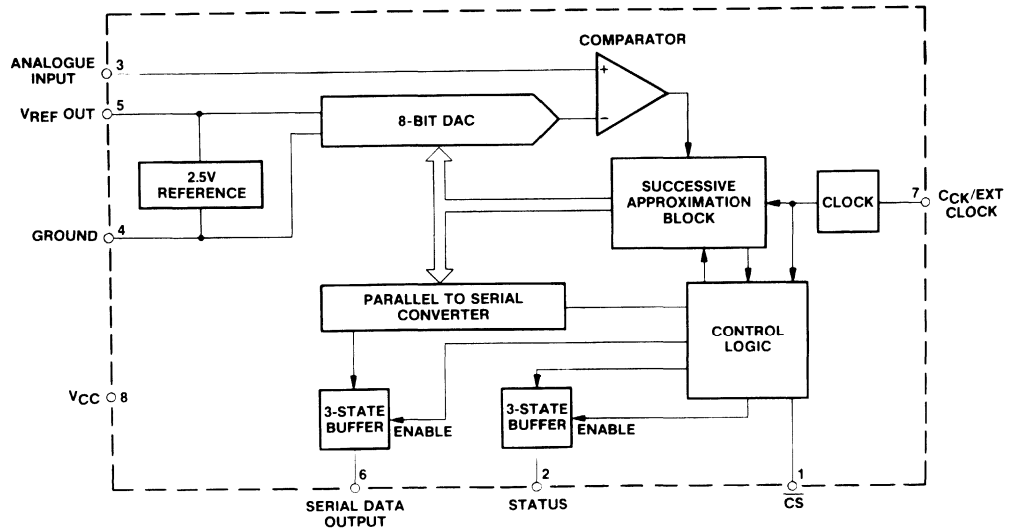


Fig.1 Block diagram of ZN509 and ZN510

ELECTRICAL CHARACTERISTICS (at V_{CC} = 5V, T_{amb} = 25°C and f_{CLK} = 1.0MHz unless otherwise specified).

Parameter	T_{amb} = +25°C			Over specified temp. range		Unit	Conditions
	Min.	Typ.	Max.	Min.	Max.		
ZN509							
Linearity error	–	–	±0.5	–	±0.5	LSB	
Differential linearity error	–	–	±0.75	–	±0.75	LSB	
ZN510							
Linearity error	–	–	±1	–	±1	LSB	
Differential linearity error	–	–	±1	–	±1	LSB	
ALL TYPES							
Zero transition	–	15	–	–	–	mV	ZN509/10E
(00000000→00000001)	–	15	–	–	–	mV	ZN509/10J
Full-scale transition	–	2.540	–	–	–	V	ZN509/10E
(11111110→11111111)	–	2.540	–	–	–	V	ZN509/10J
Linearity temperature coefficient			±3 typ.			ppm/°C	
Differential linearity temperature coefficient			±6typ.			ppm/°C	
Gain temperature coefficient			±10 typ.			ppm/°C	
Offset temperature coefficient			±7 typ.			ppm/°C	
Resolution	8	–	–	–	–	Bits	
Conversion time	8	–	–	–	–	μs	
Supply rejection	–	0.2	–	–	–	%/V	
Supply voltage	4.5	5.0	5.5	4.5	5.5	V	
Supply current	–	29	40	–	–	mA	
Power consumption	–	145	200	–	–	mW	
Ladder output impedance	–	3	–	–	–	kΩ	
COMPARATOR							
Analogue input current	–	230	–	–	–	μA	
Analogue input resistance	–	13	–	–	–	kΩ	
Analogue input voltage	−0.5	–	+3.5	−0.5	+3.5	V	

ELECTRICAL CHARACTERISTICS Cont.

Parameter	$T_{amb} = +25°C$			Over specified temp. range		Unit	Conditions
	Min.	Typ.	Max.	Min.	Max.		
INTERNAL VOLTAGE REFERENCE							
Output voltage	–	2.535	–	–	–	V	
Output voltage tolerance	–	–	±3	–	–	%	
Slope impedance	–	0.75	2	–	–	Ω	
Reference current	0.75	–	5.2	0.75	5.2	mA	
Output voltage temperature coefficient	–	70	–	–	–	ppm/°C	
CLOCK							
Maximum on-chip clock frequency	–	1.0	–	–	–	MHz	$C_{ck} = 220pF$
Clock frequency tempco	–	–0.125	–	–	–	%/°C	
Clock capacitor	220	–	–	–	–	pF	
Maximum external clock frequency	1.0	–	–	1.0	–	MHz	
Clock pulse width	250	–	–	–	–	ns	
High level I/P voltage V_{IH}	3.5	–	–	3.5	–	V	
Low level I/P voltage V_{IL}	–	–	0.8	–	0.8	V	
High level I/P current I_{IH}	–	850	–	–	–	μA	$V_{CC} = 5.5V$ $V_{IN} = 4V$
Low level I/P current I_{IL}	–	–880	–	–	–		$V_{CC} = 5.5V$ $V_{IN} = 0.8V$
Supply rejection	–	3.0	–	–	–	%/V	
LOGIC $\overline{CS}$ INPUT							
High level I/P voltage V_{IH}	2.4	–	–	2.4	–	V	
Low level I/P voltage V_{IL}	–	–	0.8	–	0.8	V	
High level I/P current I_{IH}	–	250	–	–	–	μA	$V_{CC} = +5.5V$ $V_{IN} = +5.5V$
High level I/P current I_{IH}	–	120	–	–	–	μA	$V_{CC} = +5.5V$ $V_{IN} = +2.4V$
Low level I/P current I_{IL}	–	–350	–	–	–	μA	$V_{CC} = +5.5V$ $V_{IN} = +0.4V$
DATA AND STATUS OUTPUTS							
High level output voltage V_{OH}	2.4	–	–	2.4	–	V	$I_{OH\ MAX}$
Low level output voltage V_{OL}	–	–	0.4	–	0.4	V	$I_{OL\ MAX}$
High level output current I_{OH}	–	–	–800	–	–	μA	
Low level output current I_{OL}	–	–	2	–	–	mA	
Three-state disable output leakage current			2		10	μA	

ELECTRICAL CHARACTERISTICS Cont.

Parameter	T_{amb} = +25°C			Over specified temp. range		Unit	Conditions
	Min.	Typ.	Max.	Min.	Max.		
CONTINUOUS CONVERSION							
Data output							
Delay times T_{EO}	–	100	125	–	150	ns	
T_{CD}	–	265	310	–	390	ns	
Status output							
Delay times T_{E1}	–	250	300	–	430	ns	
T_{SO}	–	165	210	–	260	ns	
T_{SI}	–	220	270	–	370	ns	
SINGLE SHOT OPERATION							
Data output							
Delay times T_{EO}	–	100	125	–	150	ns	
T_{DO}	–	200	260	–	310	ns	
T_{DI}	–	200	260	–	310	ns	
T_{CD}	–	265	310	–	390	ns	
Status output							
Delay times T_{E1}	–	250	300	–	430	ns	
T_{SO}	–	220	270	–	300	ns	
T_{SI}	–	230	280	–	320	ns	
T_{DSI}	–	250	300	–	360	ns	

GENERAL CIRCUIT OPERATION

The ZN509/10 uses the successive approximation technique to produce an 8-bit serial digital output. At the beginning of the conversion sequence the DAC input is set to the MSB. The resulting analogue output is compared with the unknown analogue input signal by means of the comparator. If the analogue input is larger the MSB is left in circuit, if not the MSB is removed. On the second clock pulse this sequence is repeated for the next most significant bit and so on until all 8-bits have been compared.

CONVERSION TIMING

The ZN509/10 will accept a low going chip select ($\overline{CS}$) pulse, which can be completely asynchronous with respect to the clock; this pulse enables the 3-state output buffers and starts the conversion. Valid serial data will be produced between one and two clock periods later depending on the relative timing of the clock and $\overline{CS}$ signals (see Fig. 3 & 4).

Upon receipt of a low going $\overline{CS}$ pulse the ZN509/10 is cleared i.e. the MSB and STATUS are set to one and all other bits reset to zero. The $\overline{CS}$ pulse can be as short as 150ns and if pulsed low during a conversion the device will be cleared and the conversion will restart. Holding the $\overline{CS}$ input low will not inhibit the operation of the device.

The STATUS produces two different types of output which is dependent upon whether the device is being operated in the single shot or continuous mode.

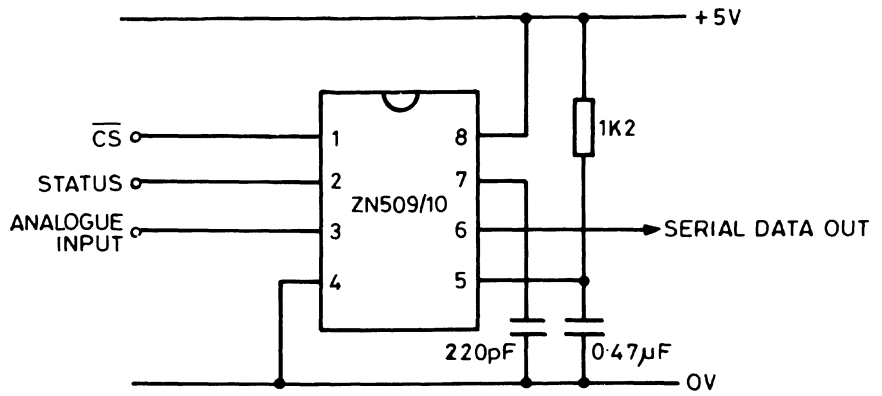


Fig. 2 Typical external connections

CONTINUOUS MODE OF OPERATION

The ZN509/10 can be made to cycle by simply tying the $\overline{CS}$ input low see Fig. 3 for timing diagram. It should be noted that after power up, valid data will only be available after the voltage reference has stabilised. This time is dependent upon the reference decoupling capacitor and load resistor, but is typically 2ms for a 1K6 resistor and a 0.47μF capacitor.

The synchronising status output goes low for one clock period every eight clock periods and coincides with the MSB data output.

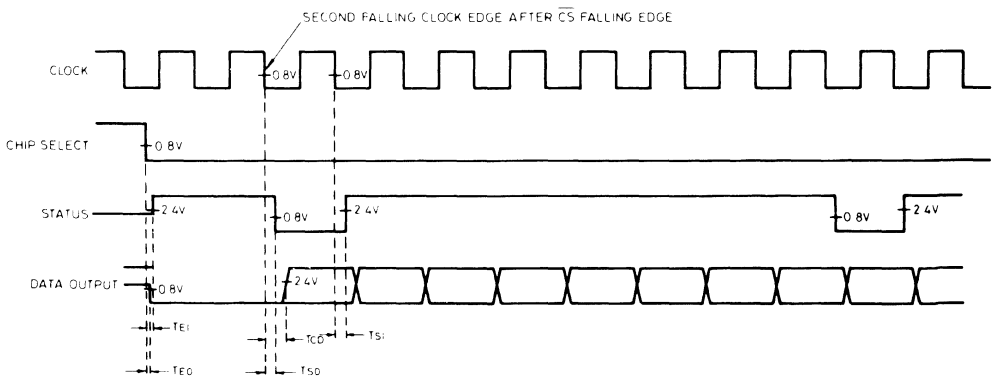


Fig. 3 Continuous (cycling) operation

SINGLE SHOT OPERATION

The ZN509/10 recognises that a single shot operation is to be performed if a $\overline{CS}$ pulse of greater than 150ns, but no longer than one clock period in length is applied. Once this pulse is applied, both the Status and Data outputs come out of 3-state, the Status going high and the data output low. Between one and two clock periods later valid data, MSB first, will appear on the data output (the status goes low to indicate when the valid data is available). When all 8 bits of data have appeared, the data output returns into a high impedance state, at which point the status goes high. One clock period later the Status output also returns to a high impedance state.

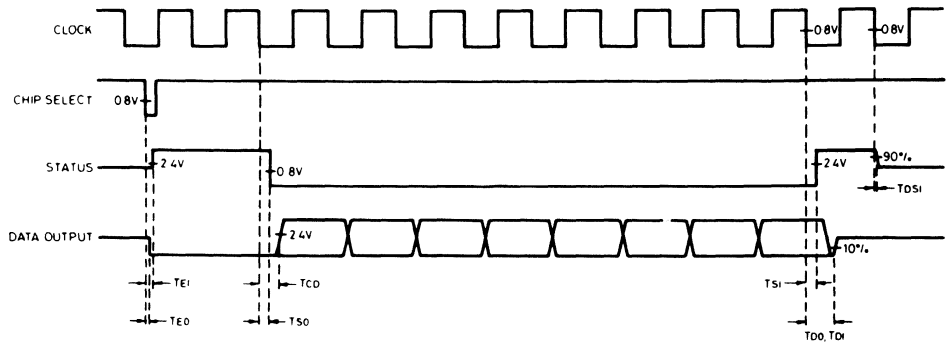


Fig. 4 Single shot operation

DIGITAL OUTPUTS

The digital outputs are provided with 3-state buffers to allow connection to a common data bus. An equivalent circuit is shown in Fig. 5. When disabled (see timing diagrams for the conditions under which this applies) both output transistors are turned off and the device presents a high impedance load to the bus. When enabled the outputs will assume the logic states present on the input to the buffer.

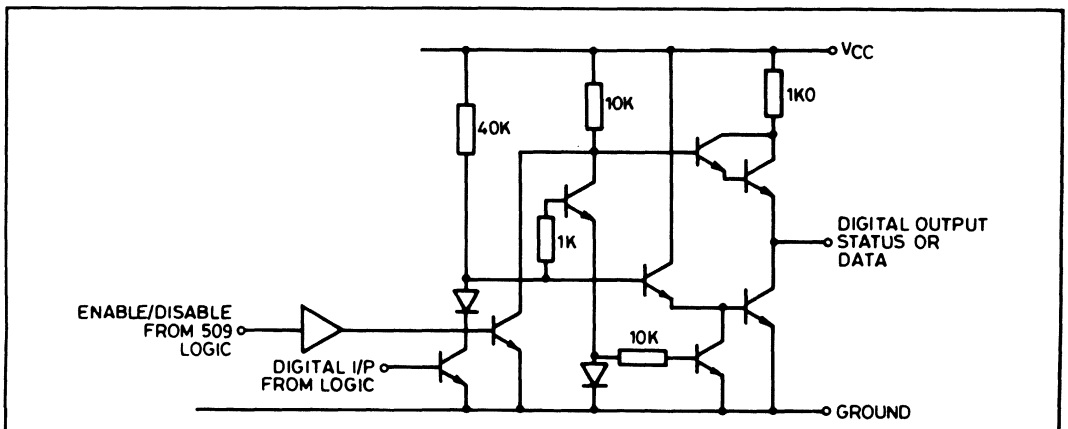


Fig. 5 Digital outputs

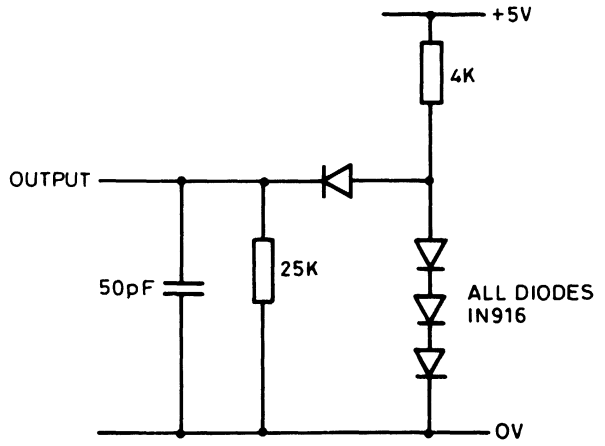


Fig. 6 Output load circuit

ON - CHIP CLOCK

The on-chip clock operates with only a single external capacitor connected between pin 7 and ground as shown in Fig. 7(a). A graph of typical oscillator frequency versus capacitance is given in Fig. 8a. The oscillator frequency may be trimmed by means of an external resistor in series with the capacitor, as shown in Fig. 7(b). A graph of typical oscillator frequency versus resistance and capacitance is given in Fig. 8b. The oscillator input may be overdriven with an external clock signal from a TTL or CMOS gate as shown in Fig. 7(c).

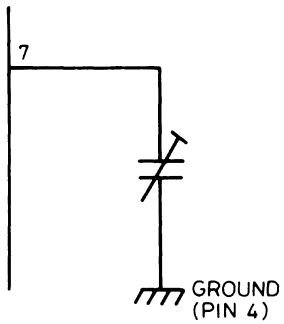


Fig. 7(a) Fixed/variable capacitor

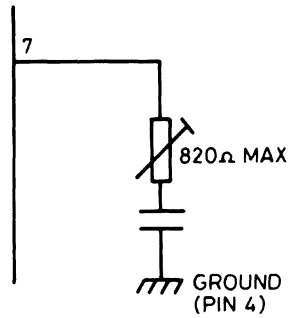


Fig. 7(b) Fixed capacitor and variable resistor

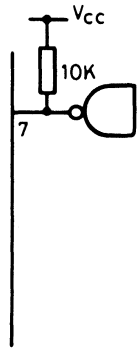


Fig. 7(c) External TTL or CMOS drive

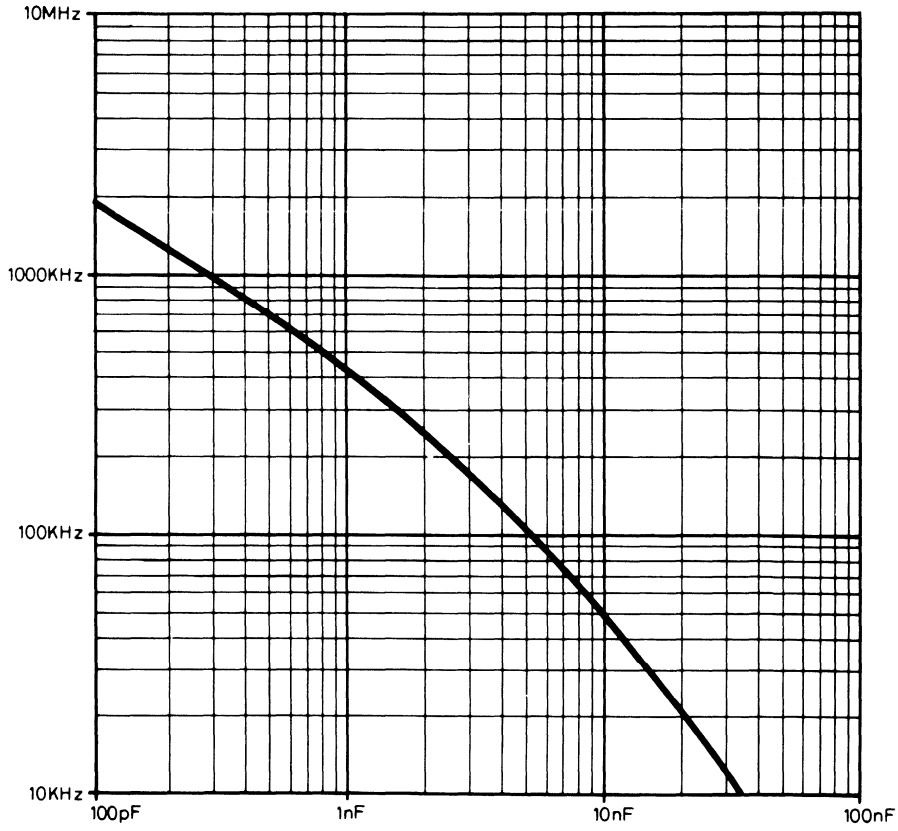


Fig. 8a Clock frequency v capacitance

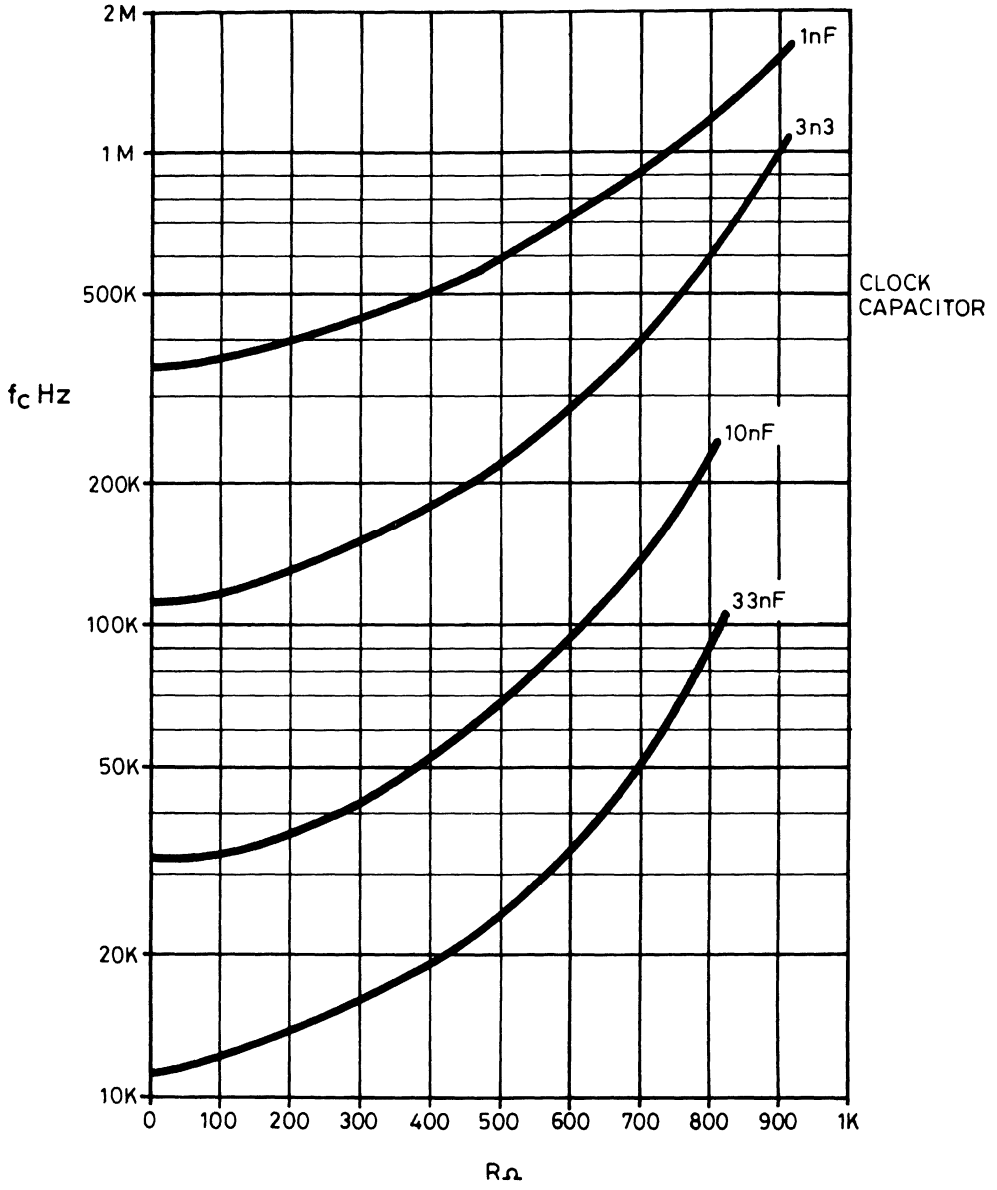


Fig. 8b Clock frequency v resistance and capacitance

ANALOGUE CIRCUITS

Reference

The internal reference is an active bandgap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig. 9). A resistor (R_{ref}) should be connected between V_{CC} and $V_{REF\ OUT}$, and a decoupling capacitor, C_{REF} (0.47μF), is required between $V_{REF\ OUT}$ and GND.

A suitable current to drive a ZN509/10 is nominally 2mA and will be supplied by an R_{REF} of 1K2 [(5-2.535)/1K2 $\simeq$ 2mA].

With $R_{REF} = 620\Omega$, the ZN509/10 reference may also be used as the reference voltage for other external circuits and can source or sink up to 1.5mA.

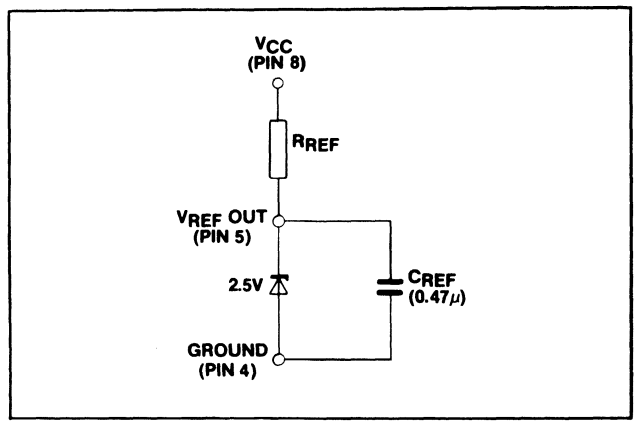


Fig. 9 Internal voltage reference

Analogue input

The equivalent analogue input is shown in Fig. 10.

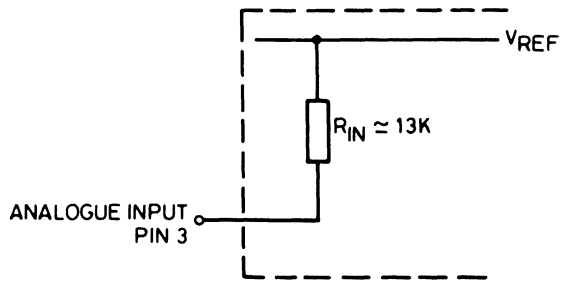


Fig. 10

D – A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 11. Each element is connected to either 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (1mV).

A binary weighted voltage is produced at the output of the R-2R ladder.

$$\text{D – A output} = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

Where n is the digital input to the D – A from the successive approximation register.

V_{OS} is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. This offset will normally be removed by the setting up procedure and since the offset temperature coefficient is low (7ppm/°C) the effect on accuracy will be negligible.

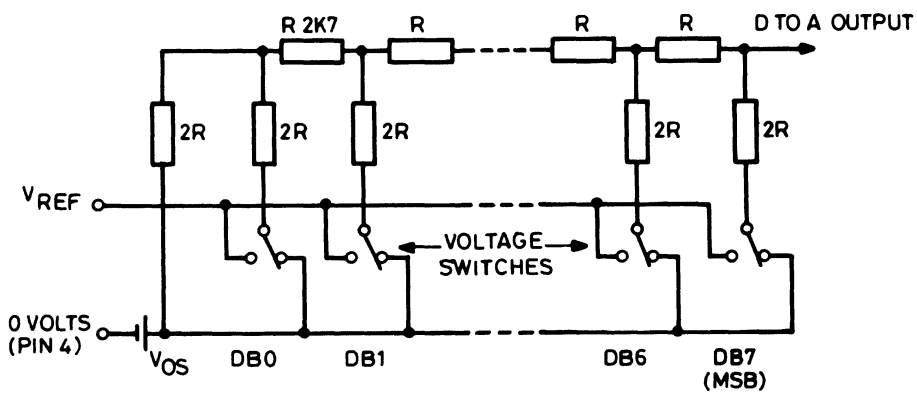


Fig. 11 R-2R ladder network

PLESSEY
Semiconductors

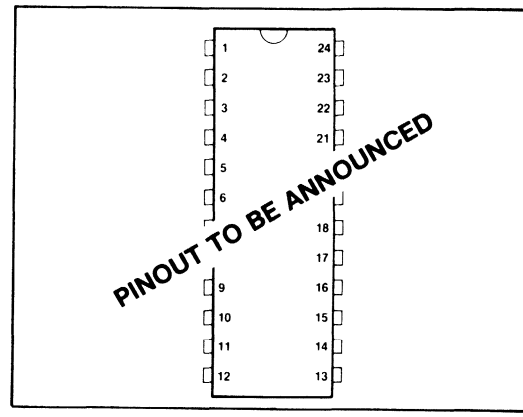
ADVANCED PRODUCT INFORMATION

ZN515

8-BIT VIDEO D-A CONVERTER

The ZN515 is a monolithic video digital-to-analog converter capable of accepting 8-bits of ECL compatible data at update rates as high as 100MHz, and converting this information to give 1 of 256 levels of grey scale. Output glitches are minimised by careful design of the switch decoding circuits and the provision of on-chip data latches.

The ZN515 incorporates complete composite video controls including sync, blanking, 10% bright and reference white and produces a composite video output to directly drive a doubly terminated 75Ω transmission line. The on-chip bandgap reference can be used externally to drive other converters in the system reducing component count and enhancing temperature tracking. This is particularly useful in high performance colour graphics where the reference of one ZN515 could be used to drive the other two ZN515 s.



Pin connections - top view

FEATURES

- 100MHz Update Rate
- Fast, 10ns Settling Time (to ±½ LSB)
- Low Glitch Energy
- ½ LSB Linearity Error
- Precision 1.25V Bandgap Reference
- Composite Sync, Blanking, Reference White and 10% Bright Controls
- ECL Compatible Inputs
- Single 5.2V Supply
- Generates Standard (RS330, RS343) 1V p-p Output across 37.5 Ohms
- 24 Pin DIL Package

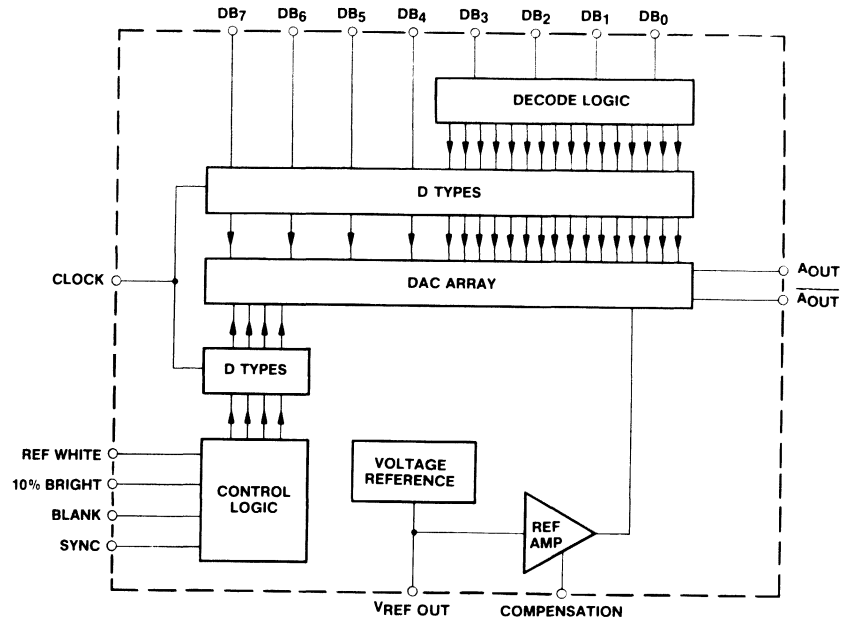


Fig.1 System diagram

PLESSEY
Semiconductors

ZN525D/E/J

8-BIT MULTIFUNCTION DATA CONVERTER

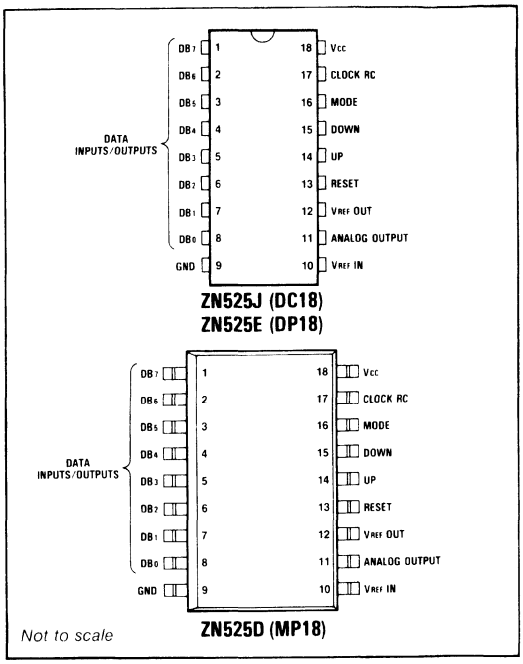
The ZN525 is a versatile, multifunction 8-bit data conversion system. A voltage-output DAC, 8-bit up/down counter, stable 2.5V bandgap reference and clock generator are contained on a single chip.

FEATURES

- Multimode Device Operates As:
  - DAC
  - ADC
  - Tracking ADC
  - Voltage to Frequency Converter
  - Ramp and Sawtooth Generator
  - Non-linear Waveform Generator
  - Voltage-Controlled Oscillator
  - Track-and-Hold Circuit
- 8-Bit Accuracy
- 800ns DAC Settling Time
- On-Chip Up/Down Counter
- On-Chip Clock
- On-Chip Voltage Reference
- Single +5V Supply
- Commercial or Military Temperature Range

ORDERING INFORMATION

Device type	Operating temperature	Package
ZN525D	0°C to +70°C	MP18
ZN525E	0°C to +70°C	DP18
ZN525J	-55°C to +125°C	DC18



Pin connections (top view)

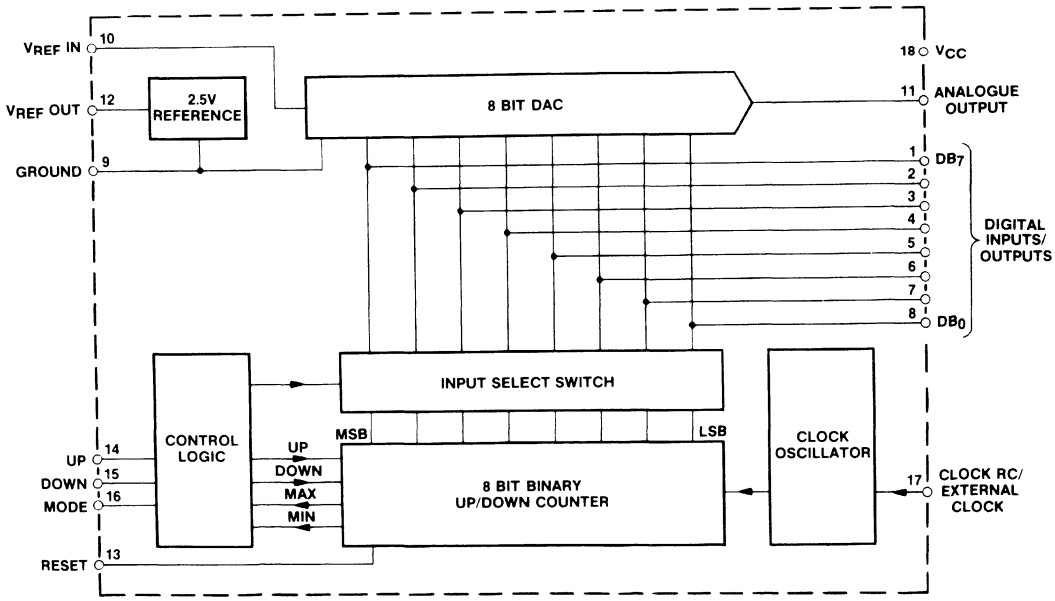


Fig.1 System diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = +5V, V_{REF} = 1.5V - 3.0V, T_{amb} = +25°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
D to A Converter					
Resolution	8	-	-	Bits	
Linearity error	-	±0.25	±0.5	LSB	T_{min}, T_{amb}, T_{max}
Differential linearity error	±0.25		±1	LSB	T_{min}, T_{amb}, T_{max}
Zero error	-	5.0	10.0	mV	ZN525D/E All bits OFF
	-	5.0	10.0	mV	ZN525J All bits OFF
Settling time to 0.5 LSB	-	500	-	ns	All bits OFF to ON
	-	800	-	ns	or vise versa
Full-scale output	2.545	2.550	2.555	V	All bits ON V_{REF} = 2.56V
Output resistance	-	4	-	kΩ	
Full-scale temperature coefficient	-	4	-	ppm/°C	Ext. V_{REF} = 2.56V
Reference voltage	0	-	3	V	
On-chip voltage reference					
Output voltage	2.4	2.59	2.7	V	R_{REF} = 390Ω
Slope resistance	-	2	4	Ω	C_{REF} = 220nF
Temperature coefficient of V_{REF}	-	50	-	ppm/°C	
Reference current	4	-	15	mA	
Counter (with external clock)					
High level threshold voltage V_{T+}	-	-	2.3	V	
Low level threshold voltage V_{T-}	1.7	-	-	V	
Maximum clock frequency	1	-	-	MHz	Note 1
On-chip clock					
Maximum frequency	500	-	-	kHz	
Clock frequency tempco	-	100	-	ppm/°C	
Clock resistor	3.3	-	100	kΩ	
Clock capacitor	100	-	-	pF	
High level threshold voltage V_{T+}	-	4.6	-	V	
Low level threshold voltage V_T	-	1.5	-	V	
Supply rejection	-	0.8	-	%/V	
Logic circuits					
Bit Inputs					
High level input voltage V_{IH}	2.0	-	-	V	
Low level input voltge V_{IL}	-	-	0.8	V	
High level input current I_{IH}	-	-	-180	μA	V_{IN} = 2.4V
Low level input current I_{IL}	-	-	-400	μA	V_{IN} = 0.4V
Bit Outputs					
High level output voltage V_{OH}	-	5.0	-		No load
Low level output voltage V_{OL}	-	0.1	-		No load
High level output voltage V_{OH}	2.4	-	-	V	I_{IH} = -40μA
Low level output voltage V_{OL}	-	-	0.4	V	I_{IL} = 2.5mA
Control inputs					
High level input voltage V_{IH}	2	-	-	V	
Low level input voltage V_{IL}	-	-	0.8	V	
High level input current I_{IH}	-	-	-25	μA	V_{IN} = 2.4V
Low level input current I_{IL}	-	-	-95	μA	V_{IN} = 0.4V
Reset pulse width	200	-	-	ns	
Power supply					
Supply voltage	4.5	5	5.5	V	
Supply current	-	39	47	mA	V_{CC} = 5.5V

NOTES 1 Speeds of up to 1.7MHz may be obtained by reducing the mark space ratio of the clock.

ABSOLUTE MAXIMUM RATINGS

Supply voltage	+7V
Max. voltage, logic and V_{REF} inputs	V_{CC}
Operating temperature range	
ZN525D/E (DP and MP)	0°C to +70°C
ZN525J (DC)	-55°C to +125°C
Storage temperature range	-55°C to +125°C

GENERAL CIRCUIT OPERATION

The ZN525 incorporates an 8-bit DAC based on a voltage switching R-2R ladder network. The reference voltage for this ladder may be derived from the on-chip precision bandgap reference, or an external reference voltage may be supplied.

The ZN525 also contains an 8-bit up/down counter and control logic. The DAC may receive its digital input data from the counter, the counter outputs being simultaneously available at an 8-bit I/O port. Alternatively the counter outputs may be inhibited and the I/O port used to feed data direct to the DAC inputs.

An on-chip oscillator is provided to drive the clock input of the up/down counter. The on-chip clock may be overridden by an external clock signal.

UP/DOWN COUNTER AND CONTROL LOGIC

The counter is a high-speed, synchronous up/down type, whose operation is determined by four control pins. The functions of the UP, DOWN and RESET inputs are fairly self explanatory, the MODE input determines the behaviour of the counter at zero and full-scale. When the MODE input is high the counter will reset to zero if it is clocked past full-scale in the UP direction and will reset to 255 if it is clocked past zero in the DOWN direction. When the MODE input is low the counter will stop on reaching full-scale or zero.

The normally invalid state of UP and DOWN inputs low simultaneously is also utilised in the ZN525. With the MODE input high and UP and DOWN inputs low the counter will cycle up and down continously, reversing at full-scale and zero. With all three control inputs low the counter outputs are disabled and the DAC inputs accessible from the I/O port.

A truth table for the control inputs is given in Table 1.

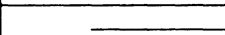
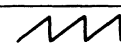
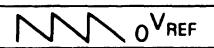
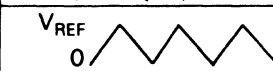
Reset	Mode	Down	Up	Digital function	Analogue waveform
1	1	1	1	Counter stopped.	
1	1	1	0	Count up continuously.	
1	1	0	1	Count down continuously.	
1	1	0	0	Count up, reverse at F.S., count down, reverse at zero.	
1	0	1	1	Counter stopped.	
1	0	1	0	Count up, stop at F.S.	
1	0	0	1	Count down, stop at zero.	
X	0	0	0	DAC mode, counter output disabled. Counter can still be reset by taking reset input low.	
0	X	X	X	Counter reset. Does not affect analogue output in DAC mode.	

Table 1

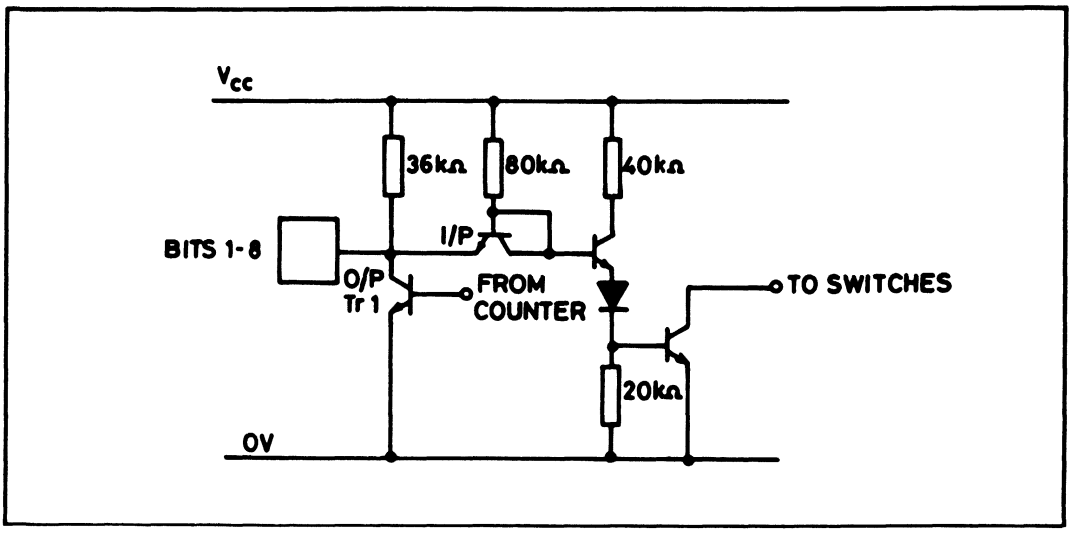


Fig.2 Bit inputs/outputs

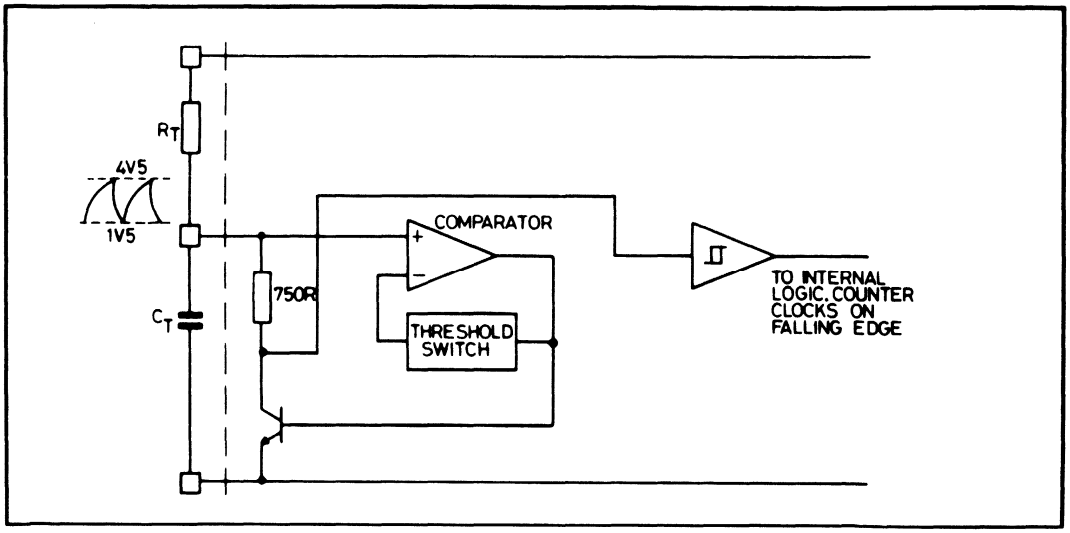


Fig.3

DATA PORT

One bit of the data port is shown in Fig.2. The input/output pin is the junction of the counter output buffer and the dAC input buffer.

Normally the DAC is driven from the counter and the counter data is also available at the port. However, when the counter outputs are disabled the output transistors are turned off and the DAC inputs may be accessed from the data port.

The data port can drive or be driven from B-series CMOS and all TTL families.

CLOCK CIRCUIT

The on-chip clock circuit of the ZN525 is shown in Fig.3. The frequency of the clock is given by

$$f_{CLK} \triangleq \frac{1}{2R_T C_C} \text{ (Hz, Ω, F)}$$

Typical graphs of oscillator frequency versus resistor and capacitor values are given in Fig.4.

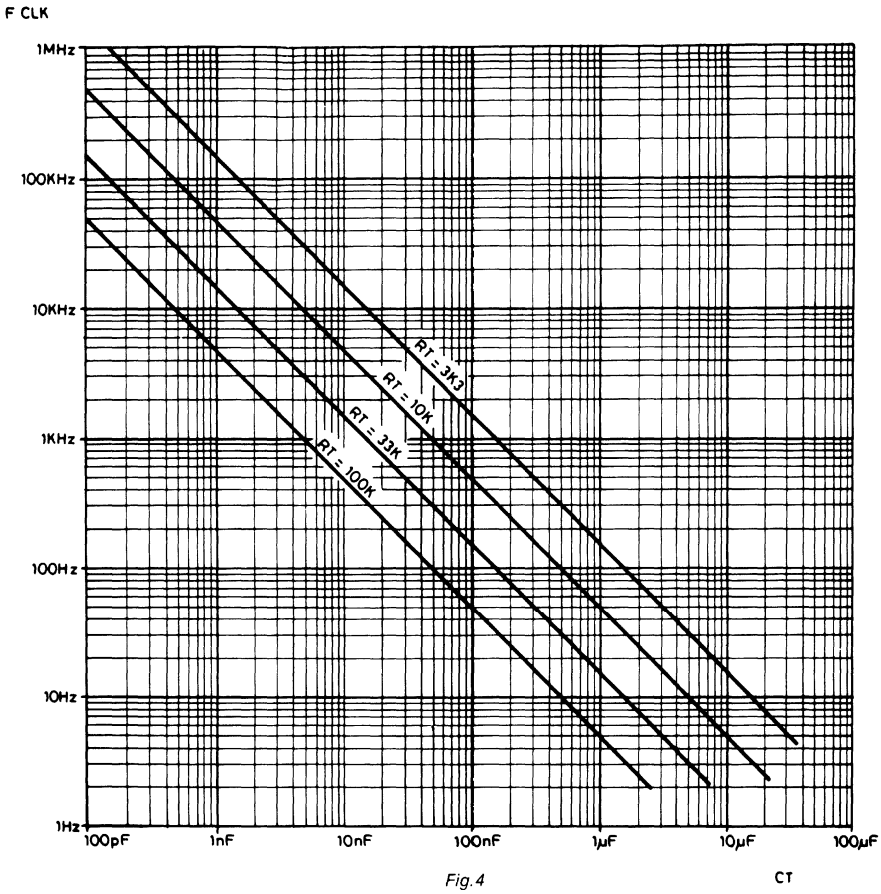


Fig.4

The external capacitor C_T is charged via the external resistor R_T to the upper threshold of the comparator (about +4.5V with V_{CC} = +5V). The comparator turns on the discharge transistor to discharge C_T and switches its threshold to the lower value of about 1.5V. When the voltage on C_T has fallen to this level the comparator turns off the discharge transistor and the cycle repeats.

The clock can be overdriven from either a TTL totem-pole output (Fig.5(a)), an open collector output (Fig.5(b)), or a CMOS gate (Fig.5(c)). In all three cases the V_{OH} of the driving gate must be attenuated to below 4.5V so that the internal discharge transistor is not turned on.

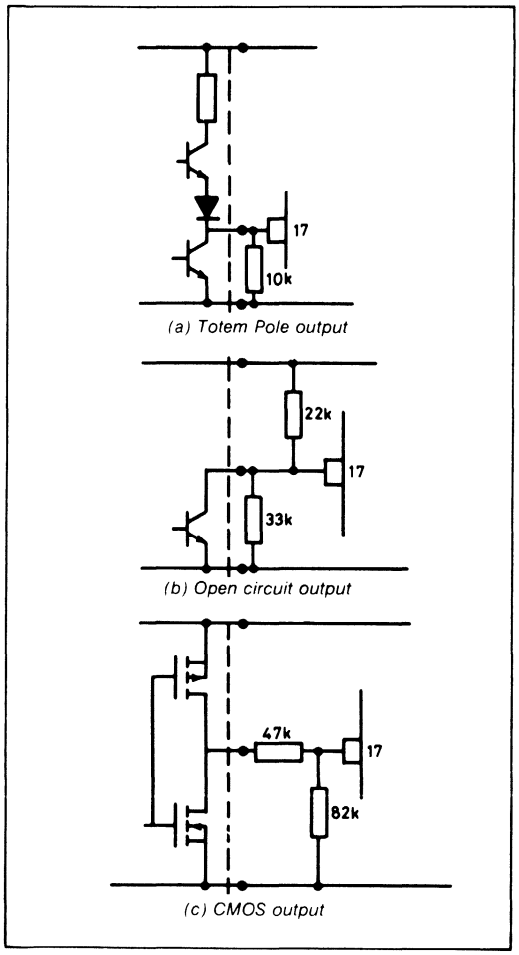


Fig.5 Overdriving the clock input

ANALOG CIRCUITS

D to A Converters

The DAC is of the voltage switching type and uses an R-2R ladder network as shown in Fig.6.

Each 2R element is connected to either 0V or V_{REF} IN by transistor voltage switches specially designed for low offset voltage (<1 millivolt). A binary weighted voltage is produced at the output of the R-2R ladder.

$$V_{OUT} = \frac{n}{256} (V_{REF}\ IN - V_{OS}) + V_{OS}$$

where n is the digital input from the counter or data port.

V_{OS} is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. The value of V_{OS} is typically 5mV for the device in any package. This offset will normally be removed by the setting up procedure and since the offset temperature coefficient is small the zero drift will be small. The DAC output range can be considered to be 0V to V_{REF} IN with an output resistance R (4kΩ).

REFERENCE

On-Chip Reference

The internal reference is an active bandgap circuit which is equivalent to a 2.5V zener diode with a very low slope impedance (Fig.7).

An external resistor (R_{REF}) should be connected between pins 12 and 18 to bias up the on-chip reference, whilst a stabilising/decoupling capacitor (C_{REF}) is required between pins 12 and 9.

To use the internal reference V_{REF} OUT (pin 12) is connected to V_{REF} IN (pin 10).

The recommended reference resistor of 390Ω will supply a nominal reference current of 6.4mA which is sufficient to drive the reference inputs of up to five ZN525s. Where several ZN525s are used in a system this useful feature can save up to four resistors and capacitors as well as reducing power consumption and giving excellent gain tracking.

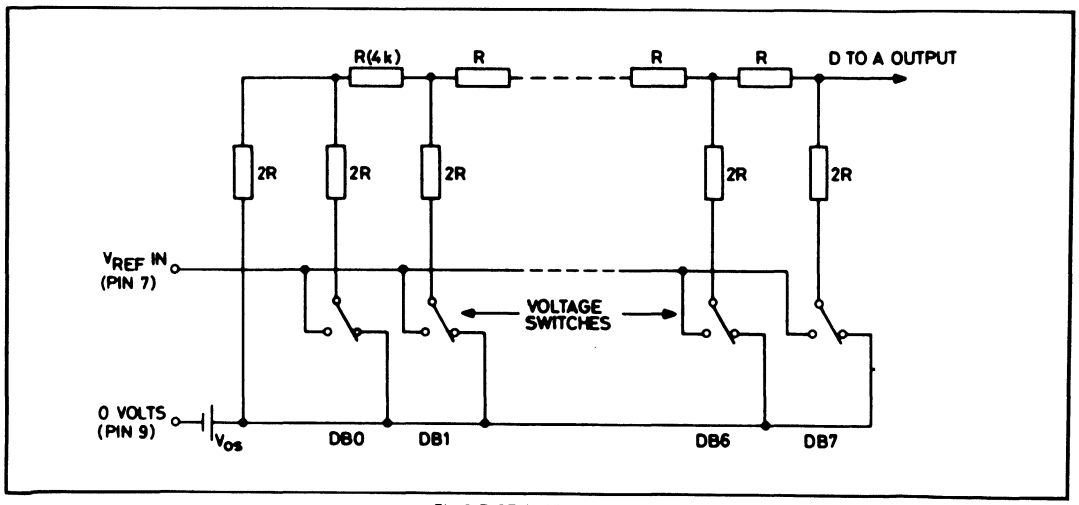


Fig.6 R-2R ladder network

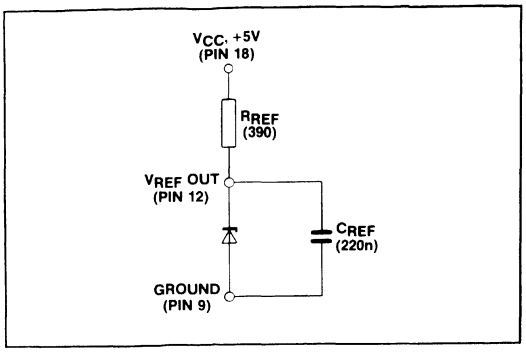


Fig.7 Internal voltage reference

APPLICATIONS

The applications of the ZN525 are too many and varied to detail in this data sheet. However a few basic configurations are illustrated. A feature of the device is that the UP/DOWN control lines can be changed totally asynchronously to the clock. The data presented to these UP/DOWN lines will be latched on the positive edge of clock and the counter will act upon this latched data on the following negative clock edge.

WAVEFORM GENERATOR

The circuit of a low frequency waveform generator is illustrated in Fig.8. This will produce stable, linear, sawtooth and triangle waveforms.

RAMP AND COMPARE A TO D CONVERTER

A simple ramp and compare A to D converter can be constructed using the ZN525 as shown in Fig.9.

The counter is set to count up from zero, producing a positive-going ramp at the analog output. When the ramp voltage exceeds the analog input the comparator output will go high, inhibiting the clock and stopping the counter. The converter can be reset and re-started by applying a low-going pulse to the reset input.

The basic analog input range is 0 - V_{REF}, but other ranges can be accommodated by adding an attenuator to the comparator unit. The comparator offset adjustment can be used for zero adjustment. Note that in this circuit the mode input is tied low to make the counter stop at full-scale. This prevents the counter cycling in the event of an overrange input.

TRACKING A TO D CONVERTER

The on-chip up-down counter allows the ZN525 to be configured very simply as a tracking A to D converter using an external comparator, as shown in Fig.10.

In this circuit two ZN424 op amps are used to make a window comparator. This has a deadband equal to one LSB of the DAC output (10mV), which is set by adjusting the offset of A1 until its threshold is 10mV above that of A2.

Whenever the analog voltage is above the threshold of A1 the counter will count up so that the DAC output increases to follow the analog voltage. Whenever the analog voltage is below the threshold of A2 the counter will count down to make the DAC follow the analog voltage. When the analog voltage is between the two thresholds the outputs of A1 and A2 will be high and the counter will be stopped.

The circuit here has an analog input range of ±10V. Other ranges may be accommodated by suitable choice of input resistors.

Note that in this circuit the mode input is tied low. This causes the counter to stop when full-scale or zero is reached, i.e. when the analog input exceeds plus or minus full-scale. Without this feature the counter would simply cycle continuously.

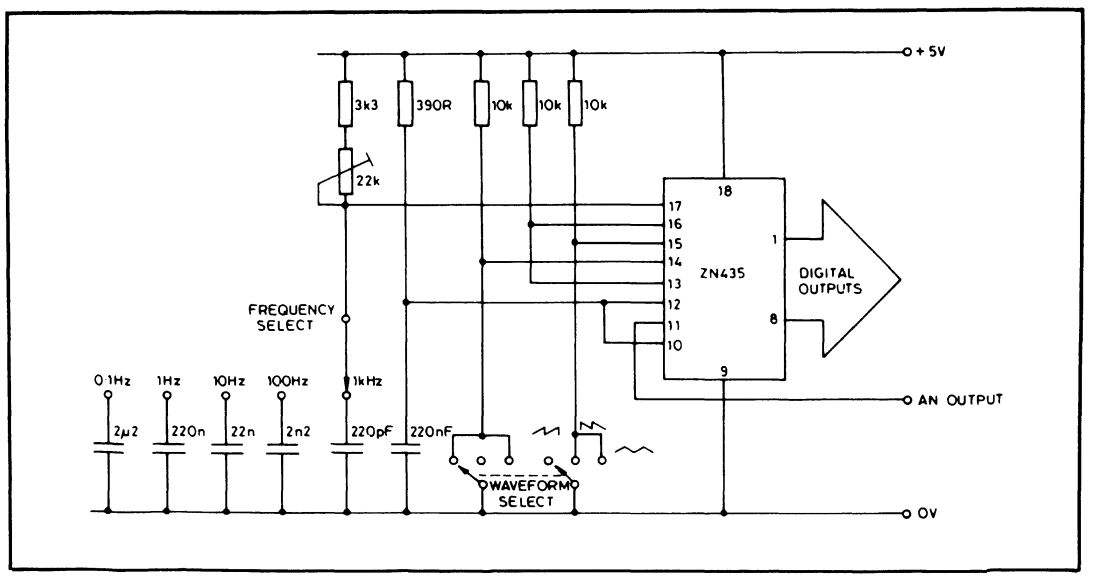


Fig.8 Waveform generator

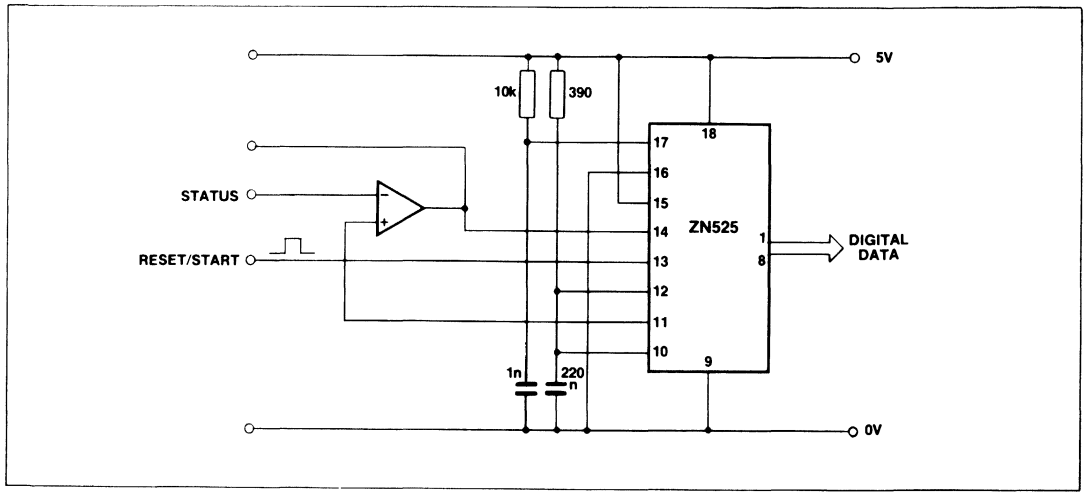


Fig.9 Ramp and compare ADC

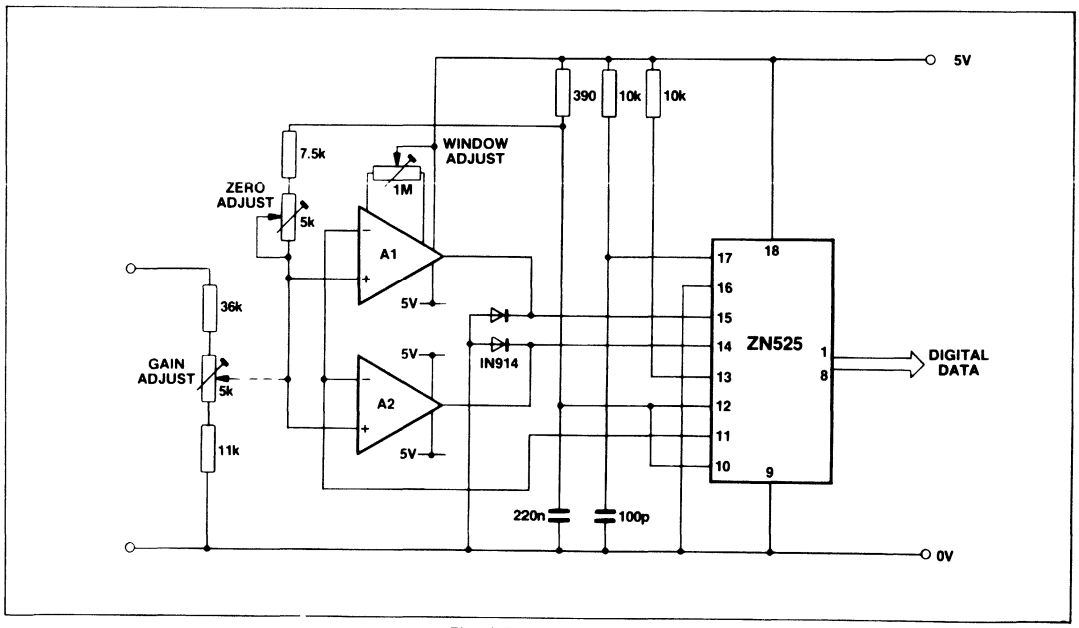


Fig.10 Tracking ADC

ZN527/ZN528

DUAL 8-BIT MICROPROCESSOR COMPATIBLE D-A CONVERTER

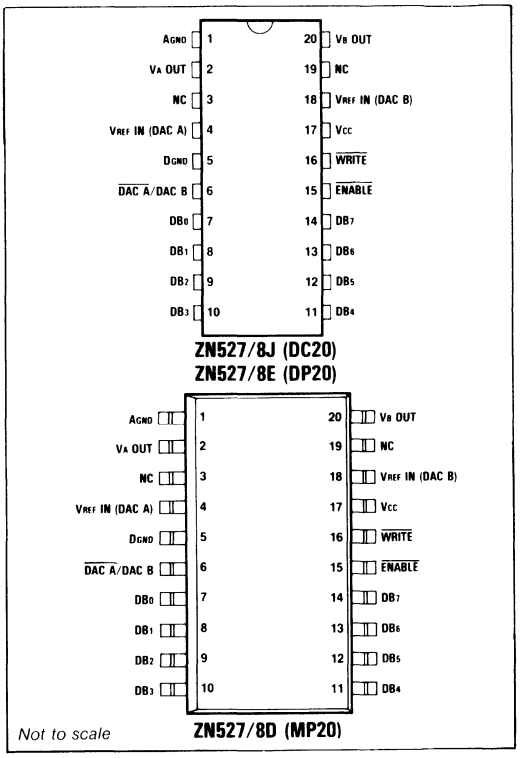
The ZN527 and ZN528 are monolithic dual 8-bit DACs designed to be easily interfaced to microprocessors. Integrated on-chip are two 8-bit DAC's, separate V_{REF} inputs and data latches for each DAC. A consequence of the two DAC's being fabricated on the same chip is excellent, inherent, DAC to DAC matching.

FEATURES

- 800ns Voltage Settling Time
- Monotonic over Full Temperature Range
- Single +5V Supply
- Excellent DAC to DAC Matching
- Separate V_{REF} IN for each DAC
- Commerical and Military Temperature Ranges

ORDERING INFORMATION

Device type	Linearity error (LSB)	Operating temperature	Package
ZN527E	±1	-40°C to +85°C	DP20
ZN528E	±½	-40°C to +85°C	DP20
ZN527D	±1	-40°C to +85°C	MP20
ZN528D	±½	-40°C to +85°C	MP20
ZN527J	±1	-55°C to +125°C	DC20
ZN528J	±½	-55°C to +125°C	DC20



Pin connections - top view

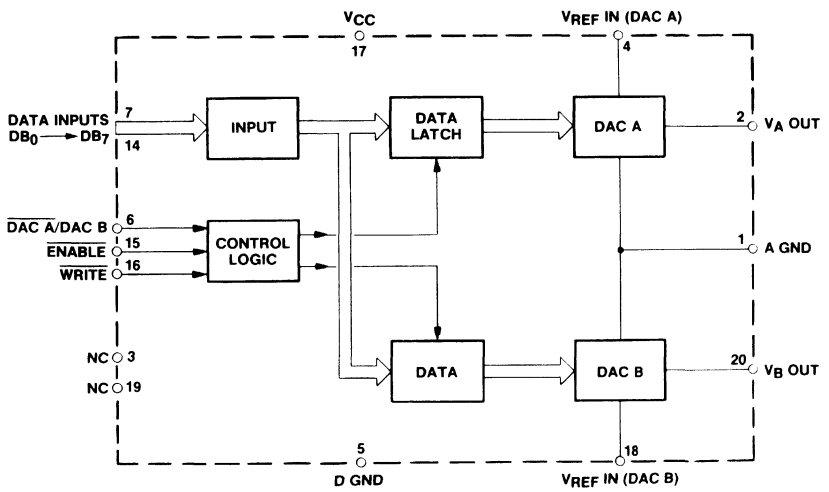


Fig.1 System diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC} +7V
Max. voltage, logic and V_{REF} input +V_{CC}
Operating temperture range
ZN527/8E and ZN527/8D -40°C to +85°C
ZN527/8J -55°C to 125°C
Storage temperature range -55°C to 125°C
Analog ground to digital ground ±200mV

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
ZN528					
Linearity error			±0.5	LSB	
Differential linearity error			±0.75	LSB	
ZN527					
Linearity error			±1.0	LSB	
Differential linearity error			±0.75	LSB	
All types					
Linearity error TC		±3		ppm/°C	
Differential non-linearity TC		±6		ppm/°C	
Offset voltage		2	5	mV	All bits OFF
Offset voltage TC		±3		ppm/°C	
Full scale output	2.545	2.550	2.555	V	External reference V_{REF} IN = 2.560V,
Full scale output TC		2		ppm/°C	all bits ON
Analog output resistance		4		kΩ	
External reference voltage	0		3.0	V	
Settling time to 0.5 LSB		800		ns	1 LSB major transition (Note 1)
		1.25		μs	All bits ON to OFF or OFF to ON (Note 1)
Operating temperature range:					
ZN508E and ZN508D	-40		85	°C	
ZN508J	-55		125	°C	
Supply voltage (V_{CC})	4.5	5.0	5.5	V	
Supply current		36		mA	
Power consumption		180		mW	
DC supply rejection		-57		dB	ΔV_{CC} = 250μV p-p f ≤ 50kHz
Digital to analog glitch impulse				nV-s	00000000 11111111
Channel to channel isolation					
$V_{REF\ A}$ to Out B		-82		dB	f ≤ 50kHz
$V_{REF\ B}$ to Out A		-82		dB	f ≤ 50kHz
Internal voltage reference					
Output voltage		2.5		V	
Slope impedance		1		Ω	
V_{REF} OUT TC		50		ppm/°C	
Reference current	1		15	mA	
Logic					
(over specified operating temperature range)					
High level input voltage V_{IH}	2.0			V	
Low level input voltage V_{IL}			0.8	V	
High level input current I_{IH}			20	μA	V_{IN} = 2.4, V_{CC} = 5.5V
			320	μA	V_{IN} = 5.5, V_{CC} = 5.5V
Low level input current I_{IL}			-310	μA	V_{IN} = 0.4V, V_{CC} = 5.5V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Switching characteristics					
Chip select to write set up time t_{CS}	150			ns	
Chip select to write hold time, T_{CH}	10			ns	
DAC select to write set up time t_{AS}	150			ns	
DAC select to write hold time t_{AH}	10			ns	
Data valid to write set up time t_{DS}	100			ns	
Data valid to write hold time t_{DH}	50			ns	
Write pulse width t_{WR}	150			ns	

NOTE
1. R_L = 10 Megohms C_L = 10pF.

D-A CONVERTER

The converters are of the voltage switching type and use an R-2R ladder network as shown in Fig.2. Each 2R element is connected to 0V or V_{REF} IN by transistor voltage switches specially designed for low offset voltage (<1mV). A binary weighted voltage is produced at the output of the R-2R ladder.

$$\text{Analog output} = \frac{n}{256}(V_{REF}\text{ IN} - V_{OS}) + V_{OS}$$

where n is the digital input to the D-A from the data latch.

V_{OS} is a small offset voltage produced by the D-A switch currents flowing through the package lead resistance. The value of V_{OS} is typically 1mV. This offset will normally be removed by the setting up procedure (see Operating Notes) and because the offset temperature coefficient is low ($\pm 6\mu V/°C$) the effect on accuracy is negligible.

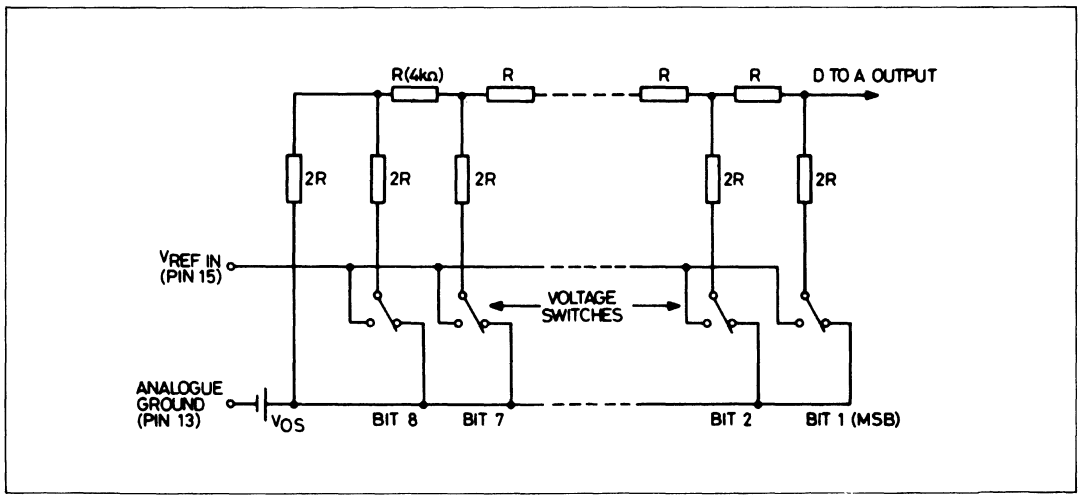


Fig.2 The R-2R ladder network

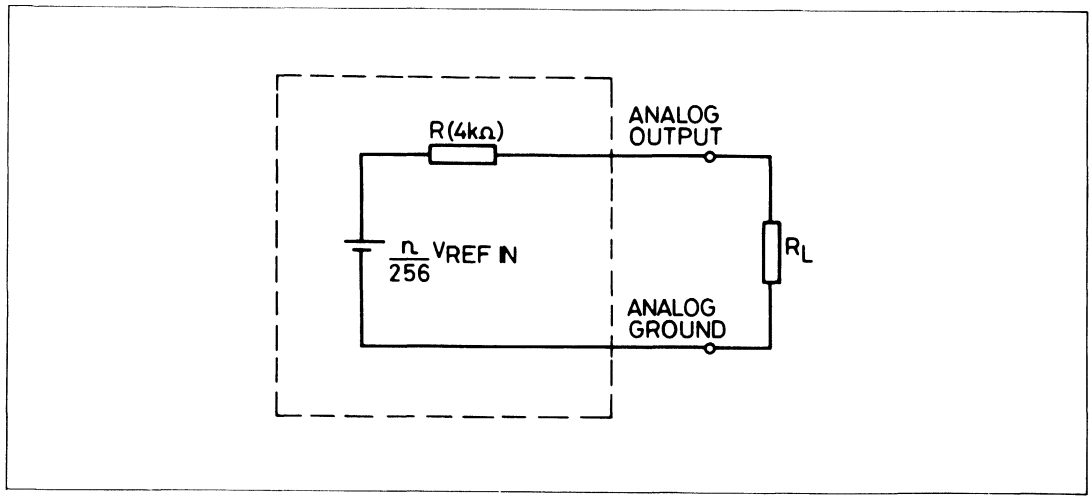


Fig.3 Analog output equivalent circuit

Fig.3 shows an equivalent circuit of the outputs (ignoring V_{OS}). The output resistance R has a temperature coefficient of +0.2% per °C.
The gain drift due to this is $\frac{0.2R}{R + R_L}$ % per °C

R_L should be chosen to be as large as possible to make the gain drift small. As an example if $R_L = 400k\Omega$ then the gain drift due to the TC of R for a 100°C change in ambient temperature will be less than 0.2%. Alternatively the ZN527/8 outputs can be buffered by amplifiers (see Operating Notes).

REFERENCE

External Reference

Should an external reference voltage be connected to V_{REF} IN, the slope resistance of such a reference source should be less than $\frac{2.5\Omega}{n}$, where n is the number of converters supplied.

V_{REF} IN can be varied from 0 to +3V for ratiometric operation. The ZN527/8 is guaranteed monotonic for V_{REF} IN above 2V.

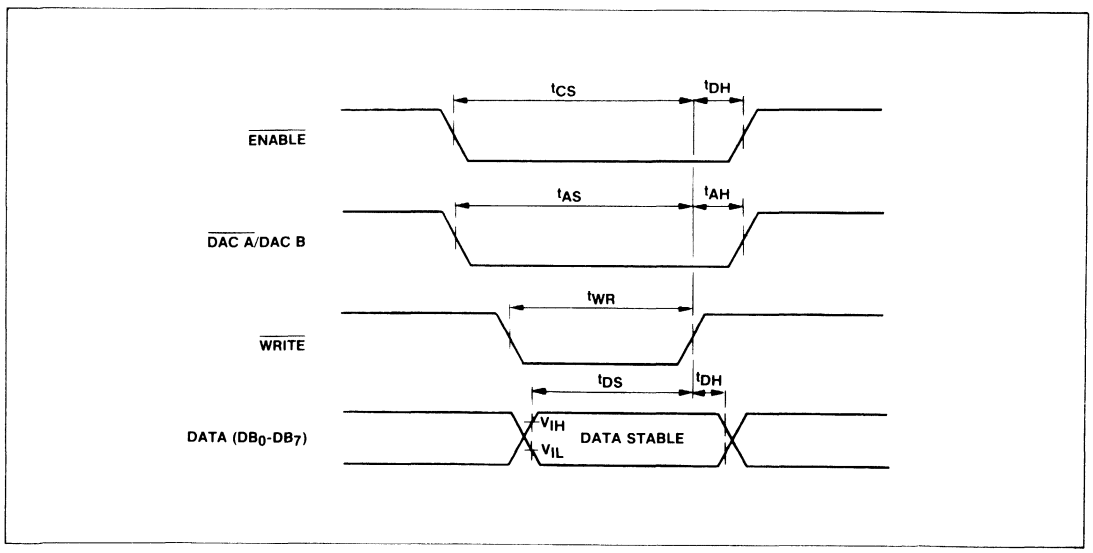


Fig.4 Logic timing diagram

LOGIC

Input coding is binary for unipolar operation and offset binary for bipolar operation. Both DAC A and DAC B share an internal data bus and an 8-bit input port. The DAC to be loaded with new data is chosen by $\overline{\text{DAC A}}$/DAC B select pin; DAC A when the input is low and DAC B when the input is high. When $\overline{\text{ENABLE}}$ and $\overline{\text{WRITE}}$ are both low the DAC selected is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to the data presented to the input port. The data is then latched when either $\overline{\text{ENABLE}}$ or $\overline{\text{WRITE}}$ are taken high.

$\overline{\text{DAC A}}$/DAC B	$\overline{\text{CS}}$	$\overline{\text{WR}}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

Table 1 Logic truth table

OPERATING NOTES

In some applications the standard 0 to V_{REF} IN output voltage range and drive capability are not suitable, and other output ranges, both unipolar and bipolar are required.

To maintain flexibility two types of operational amplifier are illustrated; the industry standard 741 and a low cost pin-compatible alternative with a JFET input, the LF351. The LF351 features a high slew rate of 13V/μs, which gives a faster potential settling time than the 741. To keep drift to a minimum when using the 741, the external range setting resistors are calculated to match them to the 4kΩ ladder output impedance. This is not a consideration with the LF351, as the input offset current change with temperature is negligible for the impedances concerned. The resistor values for the LF351 were chosen to keep the output ringing to a minimum; a problem sometimes encountered with high slew rate op-amps. It is only the relative and not the absolute values of these resistors which set the range, and therefore can be changed as long as their ratios remain the same.

Unipolar Operation

The general scheme for unipolar operation is shown in Fig.4 and is suitable for amplifiers with input bias currents less than 1.5μA.

The resulting full scale range is given by

$$V_{OUT}\,FS = \left(1 + \frac{R1}{R2}\right)(V_{REF}\,IN - 1\,LSB)$$

$$= G\,(V_{REF}\,IN) - 1\,LSB)$$

The impedance at the inverting input is R1/R2 and for low drift with temperature (741 only), this parallel combination should be equal to the ladder resistance (4kΩ).

The required nominal values of R1 and R2 are therefore given by R1 = 4GkΩ and R2 = 4G/(G–1)kΩ.

Using these relationships a table of nominal resistance values for R1 and R2 can be constructed for V_{REF} IN = 2.5V (Table 2). For gain setting R1 is adjusted about its nominal value. Practical circuit realisations for +5V and +10V output ranges are given in Figs. 6 and 7.

Output range	G	R1	R2
+5V	2	8kΩ	8kΩ
+10V	4	16kΩ	5.33kΩ

Table 2 Nominal values for R1 and R2

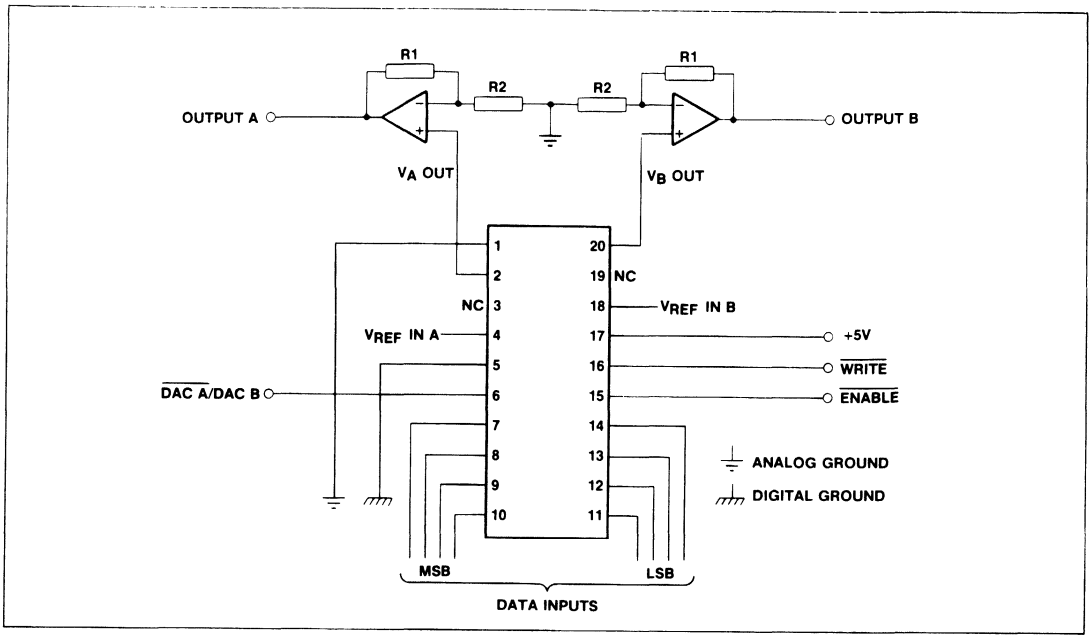


Fig.5 Unipolar operation - basic circuit

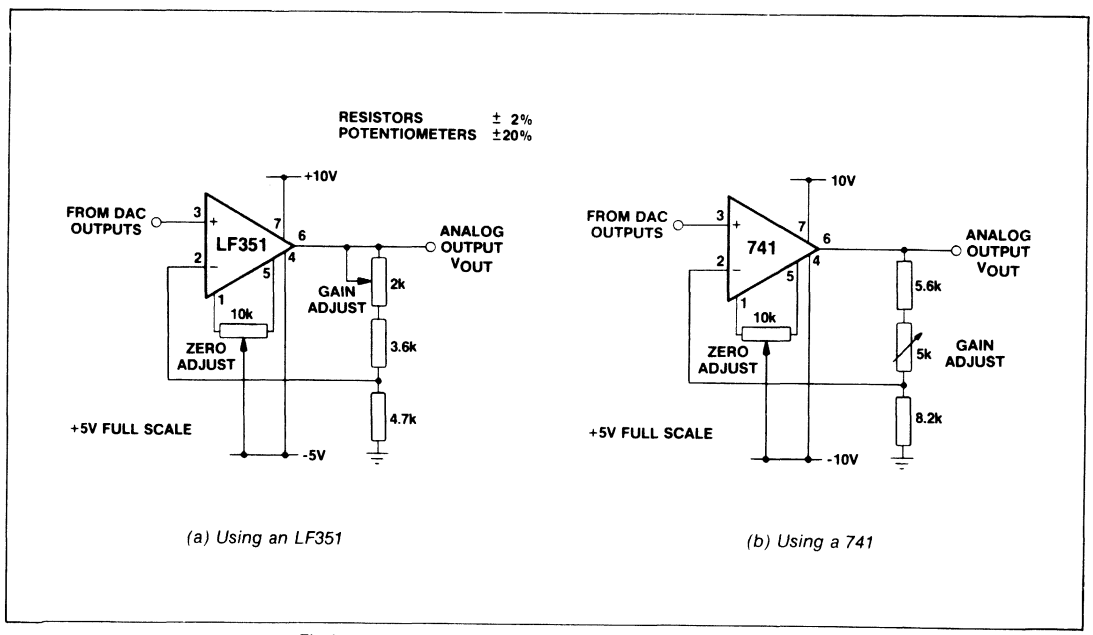
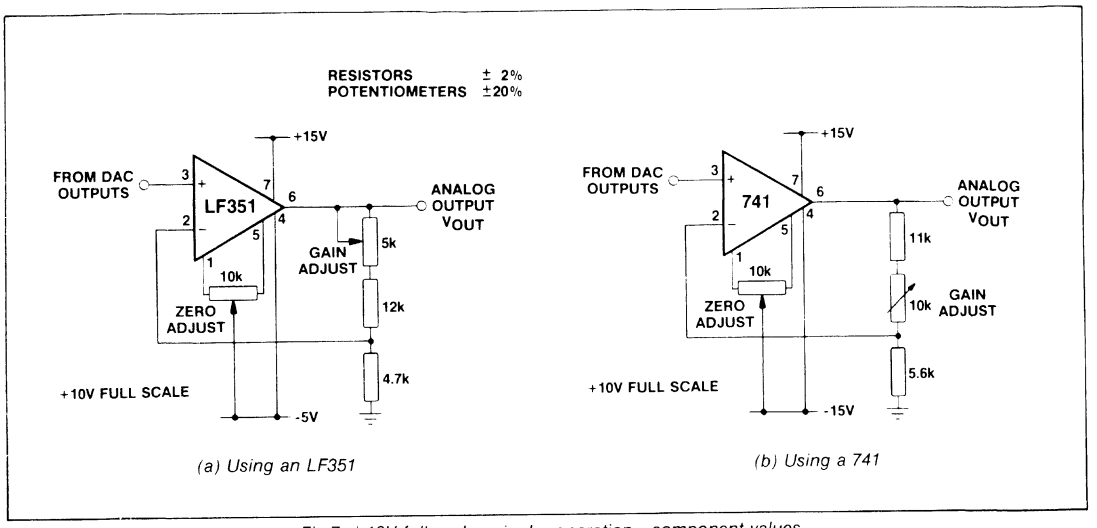


Fig.6 +5V full scale unipolar operation - component values



(a) Using an LF351 (b) Using a 741

Fig.7 +10V full scale unipolar operation - component values

Unipolar Adjustment Procedure

1. Set all bits to OFF (low) with $\overline{\text{ENABLE}}$ low and adjust zero until V_{OUT} = 0.0000V.

2. Set all bit ON (high) and adjust gain until V_{OUT} = FS - 1 LSB.

Output range, +FS	LSB	FS - 1 LSB
+5V	19.5mV	4.9805V
+10V	39.1mV	9.9609V

$$1\ LSB = \frac{FS}{256}$$

Table 3 Unipolar setting up points

Input code (Binary)	Analog output (nominal value)
11111111	FS - 1 LSB
11111110	FS - 2 LSB
11000000	¾ FS
10000001	½ FS + 1 LSB
10000000	½ FS
01111111	½ FS - 1 LSB
01000000	¼ FS
00000001	1 LSB
00000000	0

Table 4 Unipolar logic coding

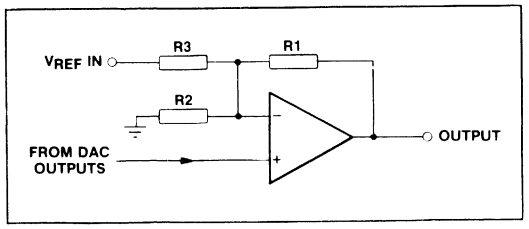


Fig.8 Bipolar operation

Bipolar Operation

For bipolar operation the output from the ZN527/8 is offset by half full scale by connecting a resistor R3 between V_{REF} IN and the inverting input of the buffer amplifier (Fig.8).

When the digital input to the ZN527/8 is zero the analog output is zero and the amplifier output should be - full scale. An input of all ones to the D-A will give a ZN527/8 output of V_{REF} IN - 1 LSB and an amplifier output of + full scale. When using the 741, the parallel combination of R1, R2 and R3 should match the 4kΩ ladder resistance.

The nominal values of R1, R2 and R3 which meet these conditions are given by

R1 = 8GkΩ, R2 = 8G/(G-1)kΩ and R3 = 8kΩ,

where the resultant output range is ±G V_{REF} IN.

A binary output range of ±V_{REF} IN (which corresponds to the basic unipolar range 0 to V_{REF} IN) is obtained if R1 = R3 = 8kΩ and R2 = ∞.

Assuming that V_{REF} IN = 2.5V the nominal values of resistors for ±5V and ±10V output ranges are given in Table 5.

Output range	G	R1	R2	R3
+5V	2	16kΩ	16kΩ	8kΩ
±10V	4	32kΩ	10.66kΩ	8kΩ

Table 5

Minus full scale (offset) is set by adjusting R1 about its nominal value relative to R3. Plus full scale (gain) is set by adjusting R2 relative to R1.

Practical circuit realisations are given in Figs. 9 and 10. Note that in the ±5V case (741 only), R3 has been chosen as 7.5kΩ (instead of 8.2kΩ) to give a more symmetrical range of adjustment using standard potentiometers.

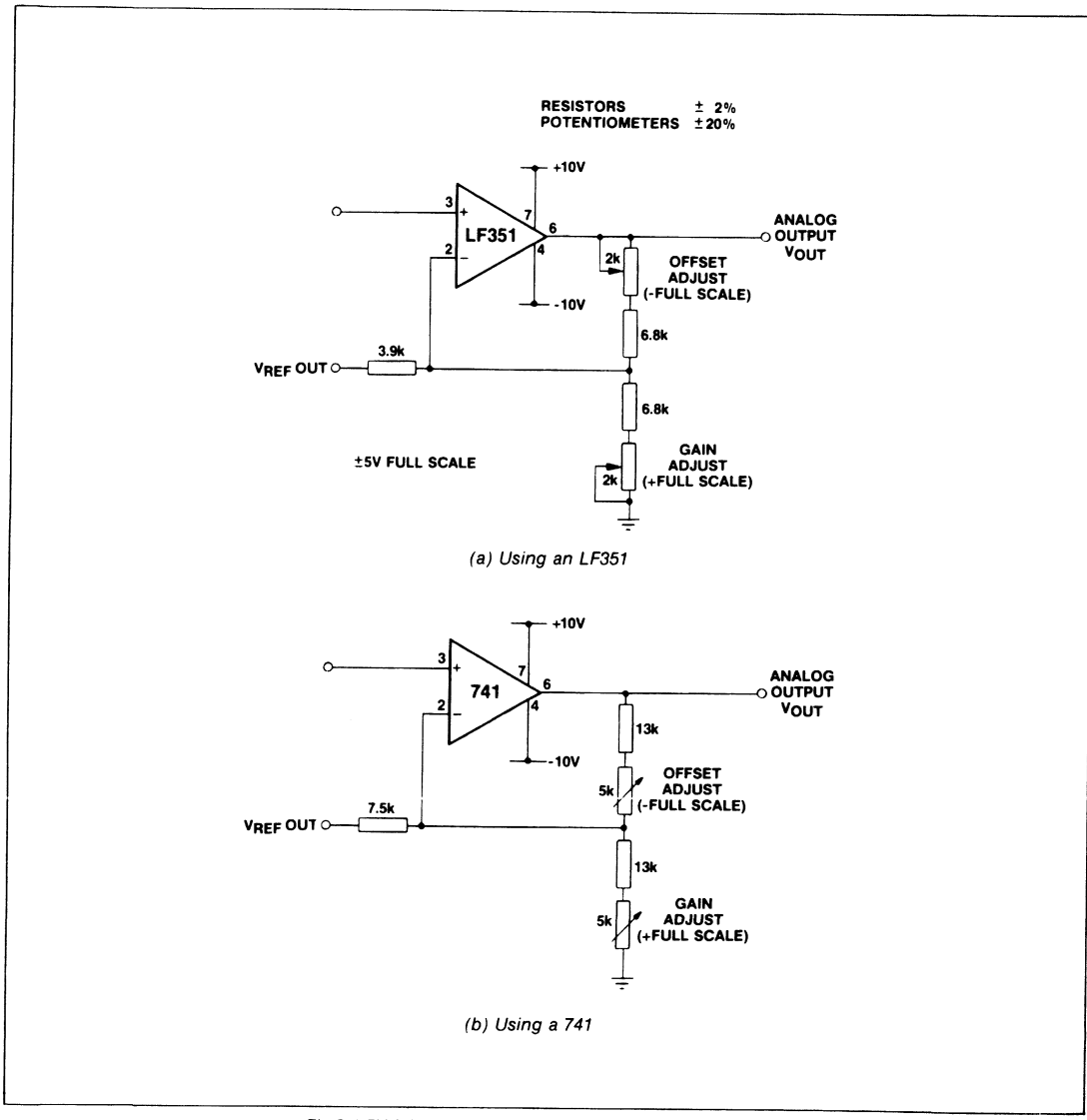


Fig.9 ±5V full scale bipolar operation - component values

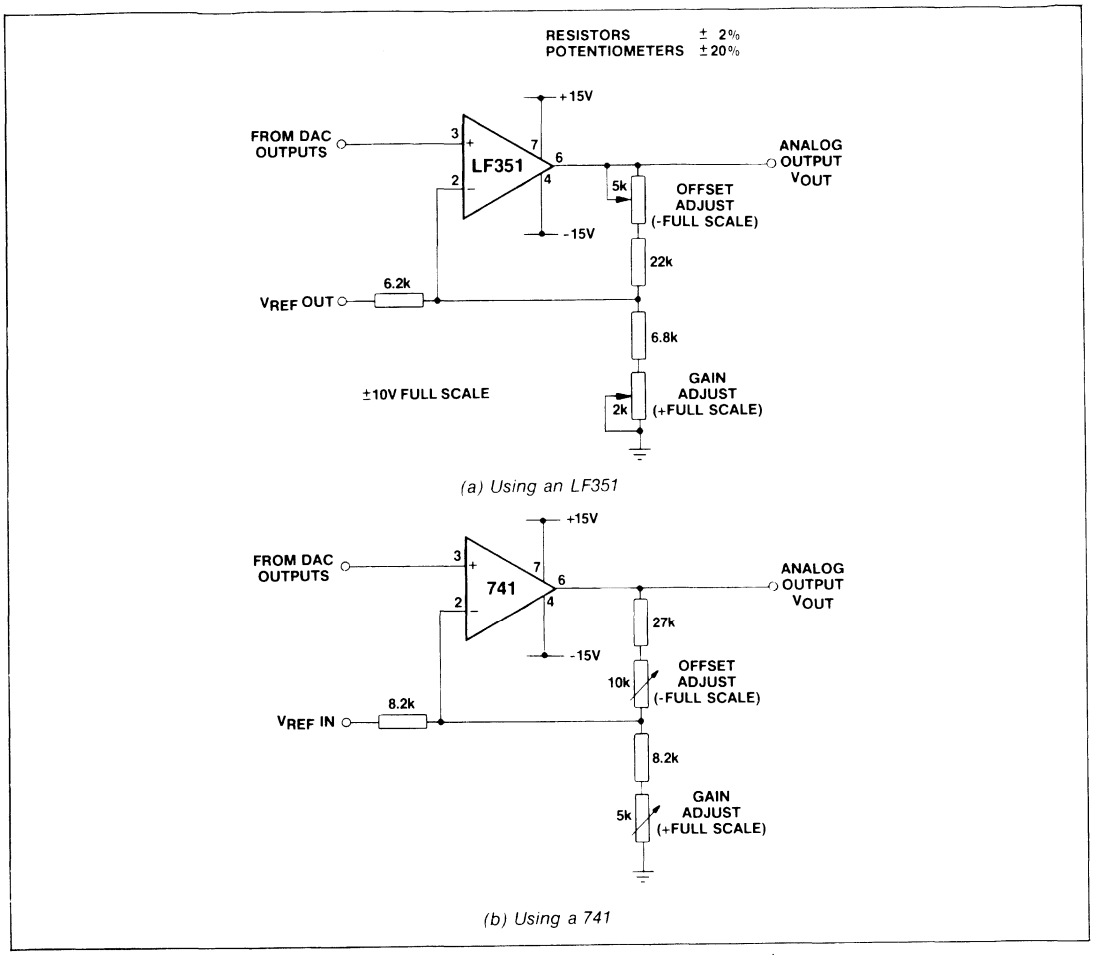


Fig.10 ±10V full scale bipolar operation - component values

Bipolar Adjustment Procedure

1. Set all bits to OFF (low) with ENABLE low and adjust offset until the amplifier output reads - full scale.

2. Set all bits ON (high) and adjust gain until the amplifier output reads + (full scale - 1 LSB).

Input range, ±FS	LSB	-FS	+(FS - 1 LSB)
±5V	39.1mV	-5.0000V	+4.9609V
±10V	78.1mV	-10.0000V	+9.9219V

$1\ LSB = \frac{2FS}{256}$

Table 6 Bipolar setting up points

Input code (offset binary)	Analog output (nominal value)
11111111	+(FS - 1 LSB)
11111110	+(FS - 2 LSB)
11000000	+½ FS
10000001	+1 LSB
10000000	0
01111111	-1 LSB
01000000	-½ FS
00000001	-(FS - 1 LSB)
00000000	-FS

Table 7 Bipolar logic coding

PLESSEY
Semiconductors

ADVANCED PRODUCT INFORMATION

ZN538/ZN539

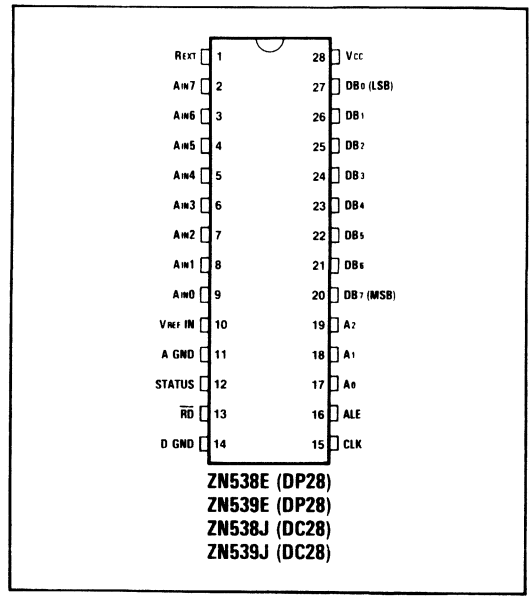
MICROPROCESSOR-COMPATIBLE 8-BIT, 8 CHANNEL DATA ACQUISITION SYSTEM

The ZN538 and ZN539 are 8-bit, 8-channel data acquisition systems designed to easily interface to most popular microprocessors. Each consists of an 8-bit successive approximation A-D converter, an 8 channel multiplexer, 8 x 8 bit RAM, clock prescaler, control logic and double buffered latches with 3-state outputs.

Using the successive approximation technique, the result of each channel conversion is loaded into the correct location of the 8 x 8 bit RAM. The address bus (A_2–A_0) is used to select the channel data to be read with the double buffered output latches allowing data to be read at any time irrespective of the conversion status.

FEATURES

- Choice of Linearity: ±0.5 LSB (ZN538) or ±1 LSB (ZN539)
- 16 microseconds Conversion Time
- 8 Analog Inputs
- On-Chip 8 x 8 RAM
- Continuous Conversion Operation
- Versatile Microprocessor Interfacing with Double Buffered Output Latch
- Microprocessor, TTL and CMOS Compatible
- Accepts Microprocessor Clocks up to 4MHz
- ROM Type Operation
- Commercial or Military Temperature Ranges



ZN538E (DP28)
ZN539E (DP28)
ZN538J (DC28)
ZN539J (DC28)

Pin connections - top view

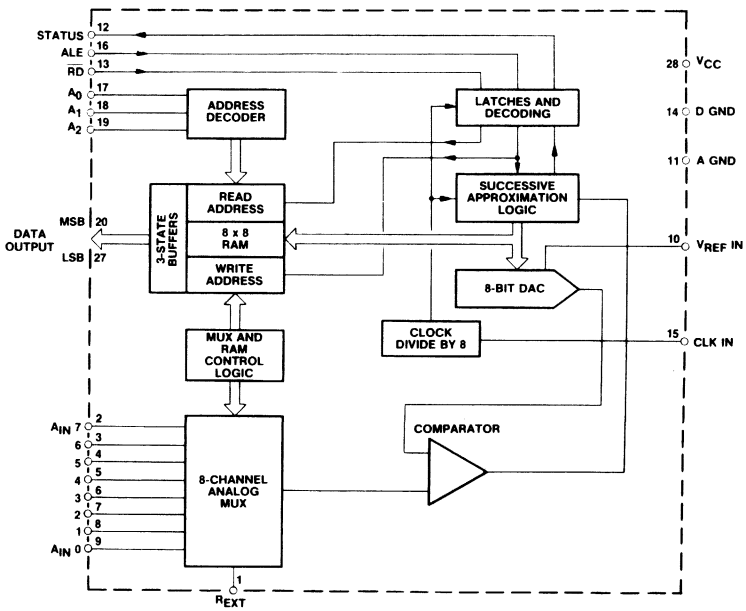


Fig.1 System diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = 5V, T_{amb} = +25°C, f_{CLK} = 500kHz

Characteristic	Value					Units	Conditions
	T_{amb} = +25°C			Over specified temp. range			
	Min.	Typ.	Max.	Min.	Max.		
ZN538							
Linearity error	-	-	±0.5	-	±0.5	LSB	
Differential linearity error	-	-	±0.75	-	±0.75	LSB	
ZN539							
Linearity error	-	-	±1	-	±1	LSB	
Differential linearity error	-	-	±1	-	±1	LSB	
All types							
Zero transition	-	10	-	-	-	mV	Plastic DP28 } Ext. Ref. = 2.56V
(00000000 00000001)	-	10	-	-	-	mV	Ceramic DG28 } Ext. Ref. = 2.56V
Full-scale transition	-	2.550	-	-	-	V	Plastic DP28 } Ext. Ref. = 2.56V
(11111110 11111111)	-	2.550	-	-	-	V	Ceramic DG28 } Ext. Ref. = 2.56V
Linearity temperature coefficient		±3 typ.				ppm/°C	} Ext. Ref. = 2.50V
Differential linearity temperature coefficient		±6 typ.				ppm/°C	} Ext. Ref. = 2.50V
Gain temperature coefficient		±10 typ.				ppm/°C	} Ext. Ref. = 2.50V
Offset temperature coefficient		±7 typ.				ppm/°C	} Ext. Ref. = 2.50V
Resolution	8	-	-	-	-	Bits	
Conversion time	16	-	-	-	-	µs	per channel
Supply rejection	-	0.2	-	-	-	%/V	
Supply voltage	4.5	5.0	5.5	4.5	5.5	V	
Supply current	-	42	-	-	-	mA	} Outputs in high impedance state
Power consumption	-	210	-	-	-	mW	} Outputs in high impedance state
Reference input range	1.5	-	3.0	-	-	V	
Ladder output impedance	-	2.7	-	-	-	kΩ	
Multiplexed inputs							
Input current	-	10	-	-	-	nA	V_{IN} = +3V, R_{EXT} = 1.8kΩ
Input resistance	-	10	-	-	-	MΩ	
Tail current	-	1.1	-	-	-	mA	R_{EXT} = 1.8kΩ, V_{EE} = -5V
Negative supply	-3	-5	-30	-3	-30	V	
Input voltage, V_{IN}	-0.5	-	+3.5	-0.5	+3.5	V	
External voltage reference							
Output voltage	1.5	-	3.0	-	-	V	
Slope impedance	-	0.75	-	-	-	Ω	
ZN538 current drain from V_{REF} IN	-	-	1.0	-	-	mA	Note 1
Output voltage temperature coefficient	-	50	-	-	-	ppm/°C	
External clock							
Clock frequency	-	-	4.0	-	4.0	MHz	
High level input voltage V_{IH}	2.0	-	-	2.0	-	V	
Low level input voltage V_{IL}	-	-	0.8	-	0.8	V	
High level input current I_{IH}	-	200	-	-	-	µA	V_{CC} = 5.5V, V_{IN} = 4V
Low level input current I_{IL}	-	-160	-	-	-	µA	V_{CC} = 5.5V, V_{IN} = 0.8V

Characteristic	Value					Units	Conditions
	T_{amb} = +25°C			Over specified temp. range			
	Min.	Typ.	Max.	Min.	Max.		
Logic ALE RD, A_2, A_1, A_0 inputs							
High level input voltage V_{IH}	2.0	-	-	2.0	-	V	
Low level input voltage V_{IL}	-	-	0.8	-	0.8	V	
High level input current I_{IH}	-	220	-	-	-	μA	V_{CC} = +5.5V V_{IN} = +5.5V
High level input current I_{IH}	-	35	-	-	-	μA	V_{CC} = +5.5V V_{IN} = +2.4V
Low level input current I_{IL}	-	-200	-	-	-	μA	V_{CC} = +5.5V V_{IN} = +0.4V
Data outputs							
High level output voltage V_{OH}	2.4	-	-	2.4	-	V	I_{OH} max.
Low level output voltage V_{OL}	-	-	0.4	-	0.4	V	I_{OL} max.
High level output current I_{OH}	-	-	-800	-	-	μA	
Low level output current I_{OL}	-	-	2.0	-	-	mA	
Enable/disable delay times							
TE1	90	-	220	-	-	ns	
TE0	60	-	120	-	-	ns	
TD1	80	-	160	-	-	ns	See Fig.9
TD0	60	-	110	-	-	ns	
ALE pulse width	150	-	-	-	-	ns	
Read pulse width	220	-	-	-	-	ns	
RD high to STATUS high	-	240	400	-	-	ns	
Address inputs stable prior to RD going low	10	-	-	-	-	ns	
Address inputs stable after RD going high	0	-	-	-	-	ns	

NOTES
1. When bipolar operation is employed, the external component connections will present an additional load to the reference. See section on bipolar operation.

ORDERING INFORMATION

Device type	Linearity error (LSB)	Operating temperature	Package
ZN538E	±0.5	0°C to +70°C	DP28
ZN538J	±0.5	-55°C to +125°C	DC28
ZN539E	±1.0	0°C to +70°C	DP28
ZN539J	±1.0	-55°C to +125°C	DC28

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	+7V
Max. voltage, logic and V_{REF} inputs	V_{CC}
Operating temperature range	0°C to 70°C (DP)
	-55°C to +125°C (DG)
Storage temperature range	-55°C to +125°C

GENERAL CIRCUIT DESCRIPTION

The ZN538/9 accepts eight analog inputs. Each input channel can be converted into an eight bit binary word using the successive approximation technique with the result of the conversion being loaded into the correct location of the 8 x 8 bit RAM. The STATUS output goes high to indicate the beginning of the conversion and the DAC input is set to the MSB. The multiplexer selects one input channel at a time on which a conversion is to be performed. The output of the DAC is compared to the unknown analog signal by means of the comparator. If the analog input is larger, the MSB is left in the circuit and if not the MSB is removed. On the second clock pulse this sequence is repeated for the next most significant bit and so on until all eight bits have been compared. On the 8th negative clock edge the STATUS goes low indicating that the conversion is complete and the RAM is updated.

The STATUS signal may be used to provide an interrupt signal when a particular channel receives updated data. To achieve this it is necessary to identify which channel is currently under conversion. The STATUS output provides an identifying signal by staying low for an additional 7 clock periods over normal 8 clock periods when channel 7 is active (see Fig.2).

Data can be read from the chip by placing the correct channel address on pins A_0, A_1 A_2. The Input address is latched when ALE goes low, when ALE goes high address input latch is transparent, and $\overline{RD}$ is taken low. The negative edge of the $\overline{RD}$ pulse powers up the required channel's RAM location and enables the 3-state outputs. The RAM is kept in a low power standby mode when not being accessed. Double buffered latches on-chip allow the outputs to be enabled at any time, irrespective of the conversion status and valid data will always be presented to the data bus, this data will be the result of the most recent conversion on that channel, therefore the $\overline{RD}$ signal can be completely asynchronous with respect to the STATUS.

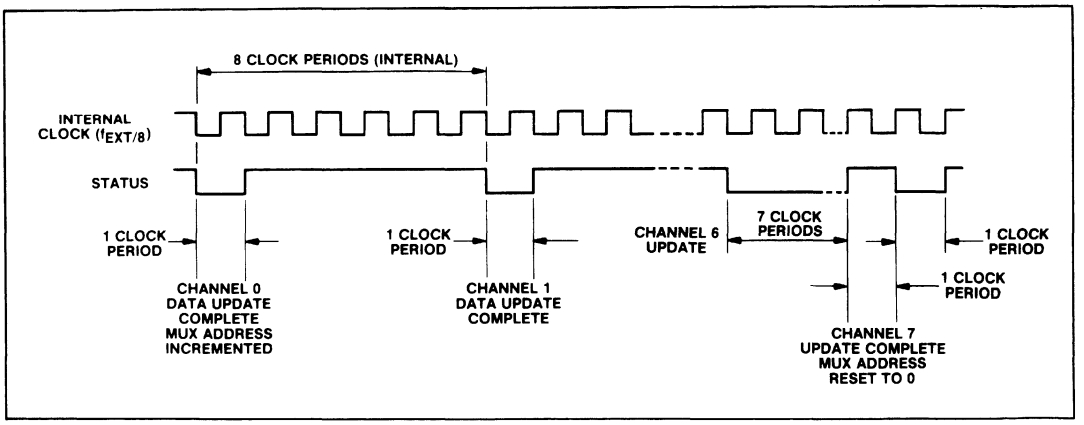


Fig.2 Status timing diagram

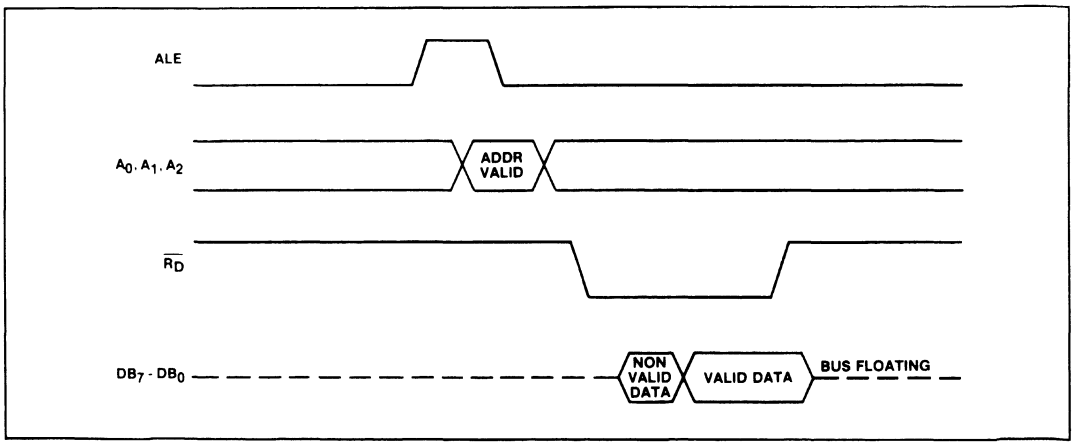


Fig.3 Read access timing diagram

ZN540/ZN541

8-BIT ANALOG I/O PORT

The ZN540 is a complete analog I/O system contained on one chip. It includes, a high speed successive approximation ADC with 5μs conversion time and double buffered latch outputs (this allows data to be read out irrespective of the state of the ADC); two DACs with double latch inputs and a maximum of 1.25μs settling time; an on-chip (2.5V) temperature compensated bandgap reference. Separate reference input connection for the ADC and a common reference connection for the DACs allows flexible connection to the on-chip reference or to an external reference source or sources.

The main data interface is a fast 8-bit bi-directional data bus and eight control lines, which allow for complete and flexible management of the system.

A programmable clock prescaler allows input clock speeds of up to 12.8MHz to be used to drive the ADC.

The device is packaged in 28-pin DIL (DP28) and a 28-pin Plastic Leaded Chip Carrier (HP28).

FEATURES

- 5 microseconds ADC
- Two 1.25 microseconds DACs
- On-Chip Bandgap Reference
- On-Chip Clock Prescaler
- Double Buffered ADC Output
- Fast Microprocessor Interface
- TTL and CMOS compatible
- Single Supply Operation
- Temperature Range -40°C to +85°C

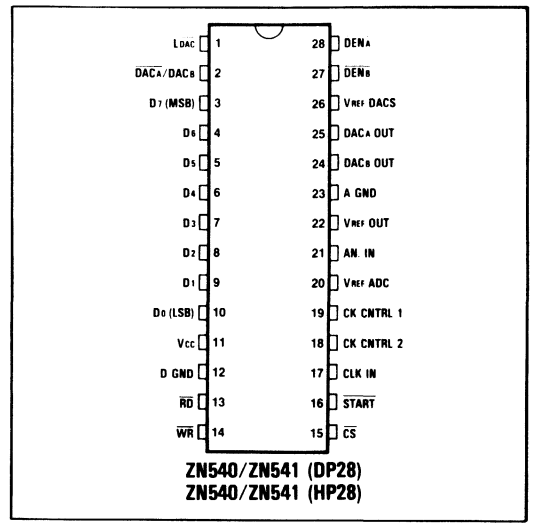


Fig.1 Pin connections (top view)

ORDERING INFORMATION

Device type	Linearity error (LSB)	Operating temperature	Package
ZN540	±0.5	-40°C to +85°C	DP28,HP28
ZN541	±1.0	-40°C to +85°C	DP28,HP28

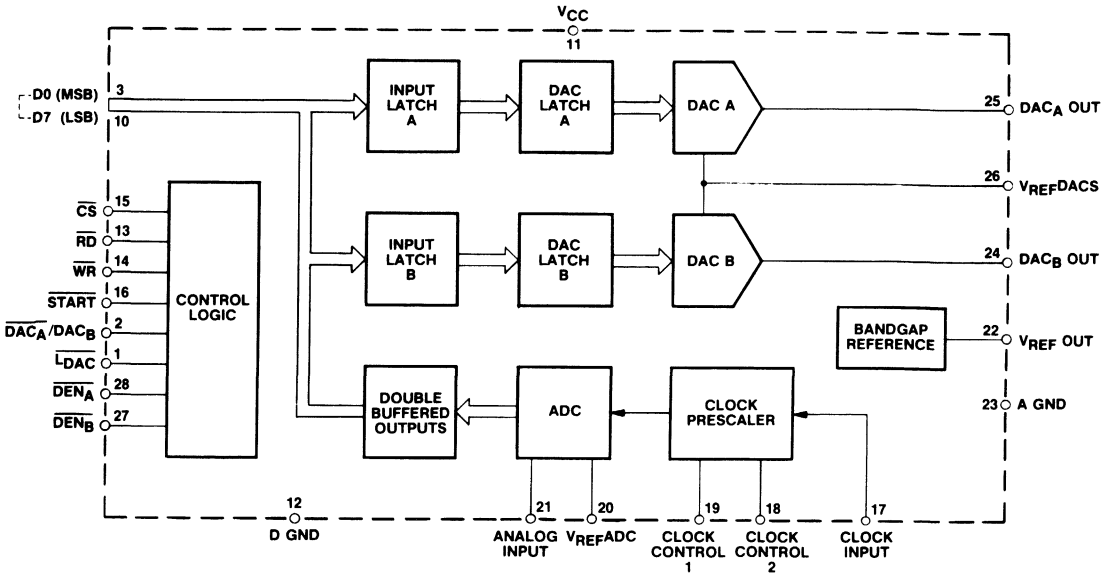


Fig.2 Block diagram of ZN540 and ZN541

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	+7V
Maximum voltage, logic inputs	V_{CC}
Operating temperature range	-40°C to +85°C
Storage temperature range	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = +5V, T_{amb} = +25°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
ADC					
ZN540					
Linearity error			±½	LSB	Clock input to ADC (after prescaling) = 1.6MHz
Differential linearity error			±¾	LSB	
ZN541					
Linearity error			±1	LSB	
Differential linearity error			±1	LSB	
Zero transition		10		mV	
Full scale transition	2.55		V		
Resolution	8			Bits	
DACs					
Linearity error			±½	LSB	
Differential linearity error			±¾	LSB	
Settling time, to ±½ LSB			800	ns	1 LSB major transition
			1.25	μs	All input data high to all input data low
Reference					
Output voltage		2.56		V	
Slope impedance			2.5	Ω	
O/P voltage T.C.		70		ppm/°C	
Reference current	2		5.2	mA	Driving both DACs and ADC (worst case)
Logic					
High level input voltage	2			V	
Low level input voltage			0.8	V	
High level output voltage	2.4			V	
Low level output voltage			0.4	V	
Maximum clock input			12.8	MHz	Prescaler ratio set to ÷8
Whole system					
Reference input range	1.5		3	V	
Supply voltage		5		V	
Supply current		95		mA	
Power consumption		475		mW	

LOGIC INTERFACE

The following Tables 1 through 5 show the control input requirements for the various system functions.

DAC

$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	$\overline{DAC_A}/DAC_B$	FUNCTION
1	0	0	0	Load I/P Latch A
1	0	0	1	Load I/P Latch B

Table 1 Loading input latches with data

$\overline{L_{DAC}}$	$\overline{DEN_A}$	$\overline{DEN_B}$	FUNCTION
0	0	1	Transfer Latch A to DAC_A
0	1	0	Transfer Latch B to DAC_B
0	0	0	TFR latch A to DAC_A and TFR Latch B to DAC_B

Table 2 Transferring data from input latches to DAC latches

ADC

$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	FUNCTION
0	1	0	Read ADC Data from Buffered Latches (Independent of state of current conversion)

Table 3 Reading ADC data

$\overline{START}$	FUNCTION
1	No conversion started
PULSED Low	Single A-D conversion then stop
HELD Low	Continuous A-D conversions

Table 4 Starting ADC conversion

CLK CNTRL 1	CLK CNTRL 2	CLOCK DIVISION RATIO
0	0	÷8
1	0	÷4
0	1	÷2
1	1	÷1

Table 5 Clock prescaler

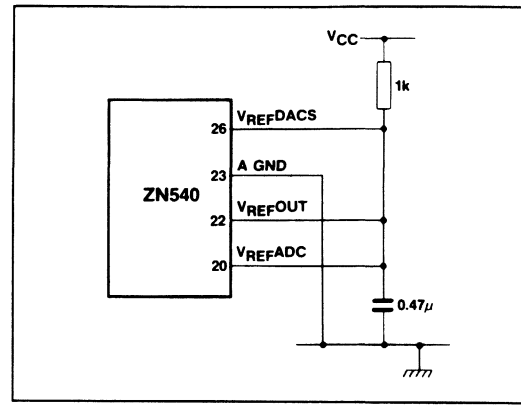


Fig.3 External components required for on-chip reference operation

ZN558

8-BIT LATCHED INPUT MONOLITHIC D-A CONVERTER

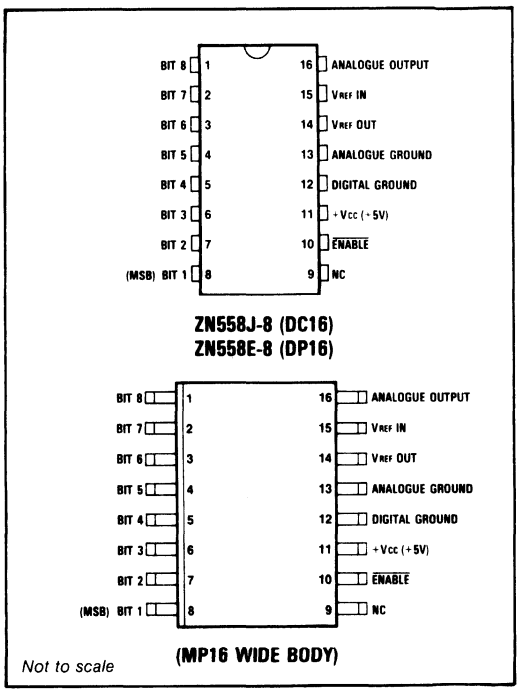
The ZN558 is a monolithic 8-bit D-A converter with input latches to facilitate updating from a data bus. The latch is transparent when enable is LOW and the data is held when enable is taken HIGH. The ZN558 also contains a 2.5V reference the use of which is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.

FEATURES

- Contains DAC with Data Latch and On-Chip Reference
- Guaranteed Monotonic over the Full Operating Temperature Range
- Single +5V Supply
- Microprocessor Compatible
- TTL and 5V CMOS Compatible
- 800ns Settling Time
- Complementary to ZN447 A-D Series
- Commercial and Military Temperature Ranges
- Available in Miniature Plastic Surface Mount Package (MP16)

ORDERING INFORMATION

Device type	Operating temperature	Package
ZN558D	0°C to +70°C	MP16
ZN558E-8	0°C to +70°C	DP16
ZN558J-8	-55°C to +125°C	DC16



Pin connections - top view

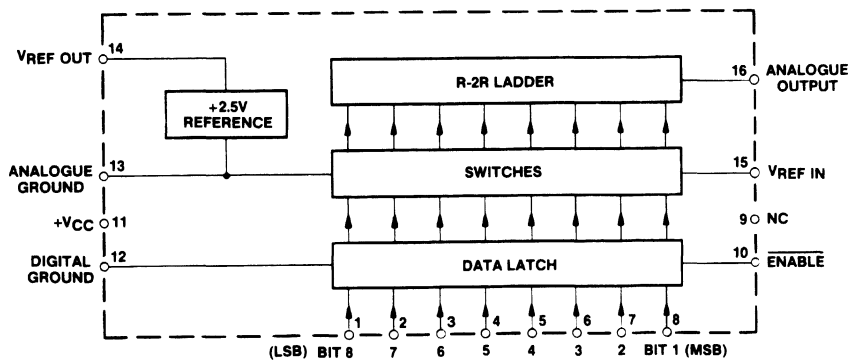


Fig.1 System diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	+7.0V
Max. voltage, logic and V_{REF} input	$+V_{CC}$
Operating temperature range	0°C to +70°C (ZN558E-8, ZN558D) -55°C to +125°C (ZN558J-8)
Storage temperature range	-55°C to +125°C
Analogue ground to digital ground	±200mV

ELECTRICAL CHARACTERISTICS (V_{CC} = +5V, T_{amb} = 25°C unless otherwise specified).

Parameter	Min.	Typ.	Max.	Units	Conditions
Internal voltage reference					
Output voltage	2.475	2.550	2.625	V	R_{REF} = 390Ω, C_{REF} = 1μF
Slope resistance		0.5	2	Ω	
$V_{REF\ OUT}$ T.C.		50		ppm/°C	
Reference current	4		15	mA	Note 1
D-A converter					
Linearity error			±0.5	LSB	2.0V ≤ $V_{REF\ IN}$ ≤ 3.0V
Differential non-linearity		±0.5		LSB	
Linearity error T.C.		±3		ppm/°C	
Differential non-linearity T.C.		±6		ppm/°C	
Offset voltage		2	5	mV	All bits OFF
Offset voltage		±6		μV/°C	
Full scale output	2.545	2.550	2.555		External reference $V_{REF\ IN}$ = 2.560V, all bits ON
Full scale output T.C.		2		ppm/°C	
Analogue output resistance		4		kΩ	
External reference voltage	0		3.0	V	
Settling time to 0.5 LSB		800		ns	1 LSB major transition (note 2)
		1.25		μs	All bits ON to OFF or OFF to ON (note 2)
Operating temperature range:					
ZN558E-8/D	0		70	C	
ZN558J-8	-55		125	C	
Supply voltage (V_{CC})	4.5	5.0	5.5	V	

Note 1 See REFERENCE, page 1-88.

Note 2 R_L = 10MΩ, C_L = 10pF.

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	Min.	Typ.	Max.	Units	Conditions
Supply current		20	30	mA	Note 3
Power consumption		100		mW	
Logic (over specified operating temperature range)					
High level input voltage	2.0			V	
Low level input voltage			0.8	V	
High level input current			60	μA	$V_{IN} = 5.5V$, $V_{CC} = Max.$
			20	μA	$V_{IN} = 2.4V$, $V_{CC} = Max.$
Low level input current			−5	μA	$V_{IN} = 0.4V$, $V_{CC} = Max.$
Input clamp diode voltage		−1.5		V	$I_{IN} = -8mA$
Enable pulse width	100			ns	
Data set-up time	150			ns	Note 4
Data hold time	10			ns	Note 5

Note 3 All inputs HIGH ($V_{IH} = 3.5V$).
Note 4 Set up time before $\overline{\text{enable}}$ goes high.
Note 5 Hold time after $\overline{\text{enable}}$ goes high.

D-A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 2. Each 2R element is connected to 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (<1mV). A binary weighted voltage is produced at the output of the R-2R ladder.

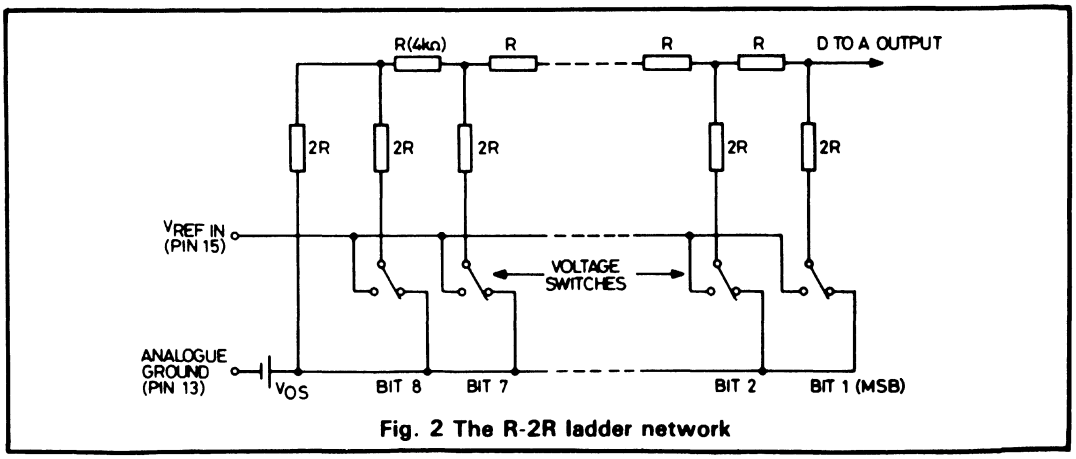


Fig. 2 The R-2R ladder network

$$\text{Analogue output} = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input to the D-A from the data latch.

V_{OS} is a small offset voltage produced by the D-A switch currents flowing through the package lead resistance. The value of V_{OS} is typically 1mV. This offset will normally be removed by the setting up procedure (see APPLICATIONS section) and because the offset temperature coefficient is low ($\pm 6\mu V/°C$) the effect on accuracy is negligible.

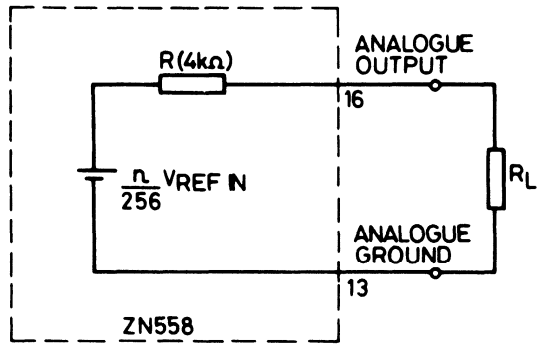


Fig. 3 Analogue output equivalent circuit

Fig. 3 shows an equivalent circuit of the output (ignoring V_{OS}). The output resistance R has a temperature coefficient of +0.2% per °C.

The gain drift due to this is $\frac{0.2R}{R+R_L}$ % per °C

R_L should be chosen to be as large as possible to make the gain drift small. As an example if R_L = 400kΩ then the gain drift due to the T.C. of R for a 100°C change in ambient temperature will be less than 0.2%. Alternatively the ZN558 can be buffered by an amplifier (see Operating Notes).

REFERENCE

(a) Internal reference

The internal reference is an active band gap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig. 4). A resistor (R_{REF}), should be connected between $+V_{CC}$ (pin 11) and pin 14. The recommended value of 390Ω will supply a nominal reference current of (5.0-2.5)/0.39 = 6.4mA. A stabilising/decoupling capacitor $C_{REF} = 1\mu F$ is required between pins 14 and 13 for internal reference option, $V_{REF\ OUT}$ (pin 14) being connected to $V_{REF\ IN}$ (pin 15).

Up to five ZN558's may be driven from one internal reference (there is no need to reduce R_{REF}). This useful feature saves power and gives excellent gain tracking between the converters.

(b) External reference

If required an external reference voltage may be connected to $V_{REF\ IN}$. The slope resistance of such a reference source should be less than $\frac{2.5\Omega}{n}$, where n is the number of converters supplied.

$V_{REF\ IN}$ can be varied from 0 to +3V for ratiometric operation. The ZN558 is guaranteed monotonic for $V_{REF\ IN}$ above 2V.

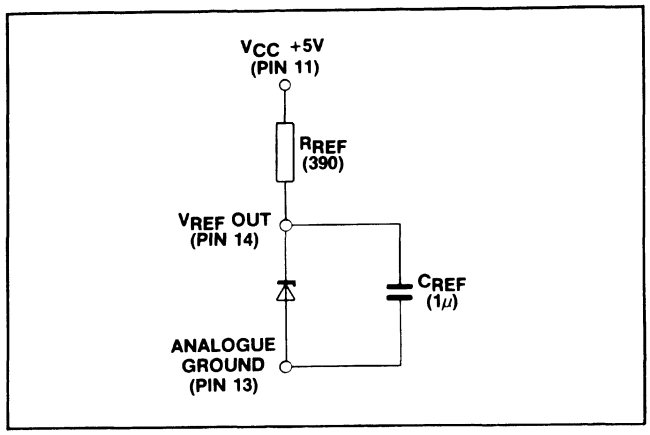


Fig.4 Internal voltage reference

LOGIC

Input coding is binary for unipolar operation and offset binary for bipolar operation. When the enable input is low the data inputs drive the D-A directly. When enable goes high the input data word is held in the data latch.

The equivalent circuit for the data and clock inputs is shown in Fig.5.

The ZN558 is provided with seperate analogue and digital ground connections. The circuit will operate correctly with as much as ±200mV between the two grounds.

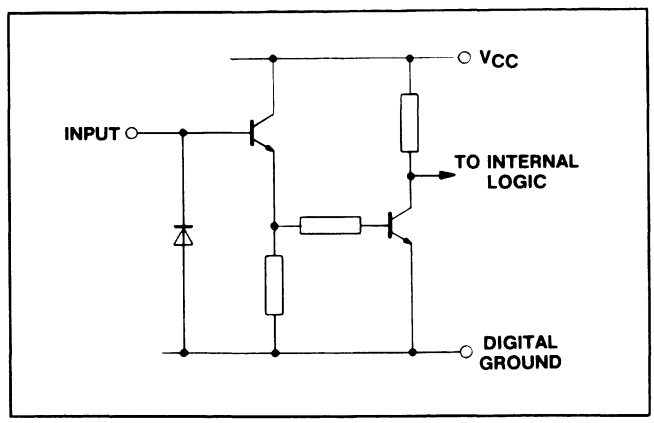


Fig. 5 Equivalent circuit of all inputs

OPERATING NOTES

(1) Unipolar D-A converter

The nominal output range of the ZN558 is 0 to $V_{REF\ IN}$ through a 4kΩ resistance. Other output ranges can readily be obtained by using an external amplifier.

The general scheme (Fig. 6) is suitable for amplifiers with input bias currents less than 1.5μA.

The resulting full scale range is given by

$$V_{OUT}\ FS = \left(1 + \frac{R1}{R2}\right) V_{REF\ IN} = G.V_{REF\ IN}$$

The impedance at the inverting input is R1//R2 and for low drift with temperature this parallel combination should be equal to the ladder resistance (4kΩ). The required nominal values of R1 and R2 are given by $R1 = 4GkΩ$ and $R_2 = 4G/(G-1)kΩ$.

Using these relationships a table of nominal resistance values for R_1 and R_2 can be constructed for $V_{REF\ IN} = 2.5V$.

Output range	G	R_1	R_2
+5V	2	8kΩ	8kΩ
+10V	4	16kΩ	5.33kΩ

For gain setting R_1 is adjusted about its nominal value. Practical circuit realisations (including amplifier stabilising components) for +5 and +10V output ranges are given in Fig. 7. Settling time for a major transistion is 1.5μs typical.

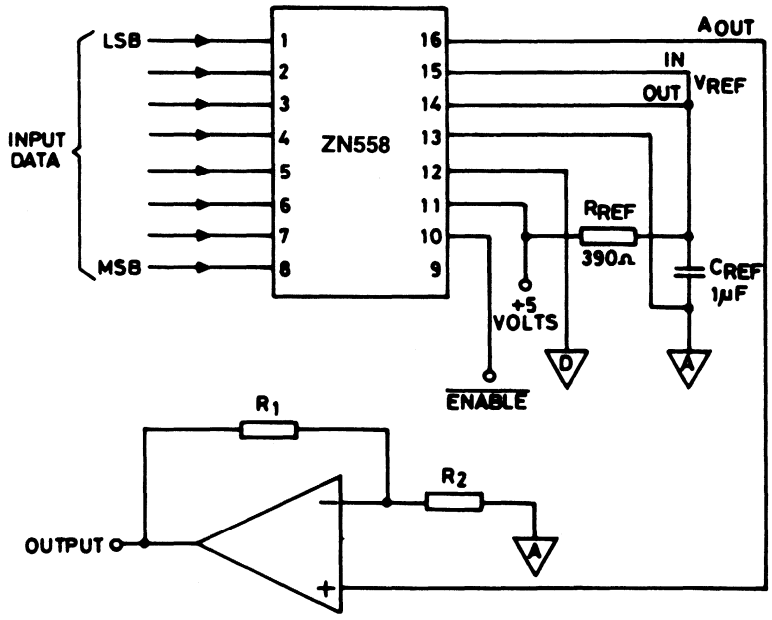
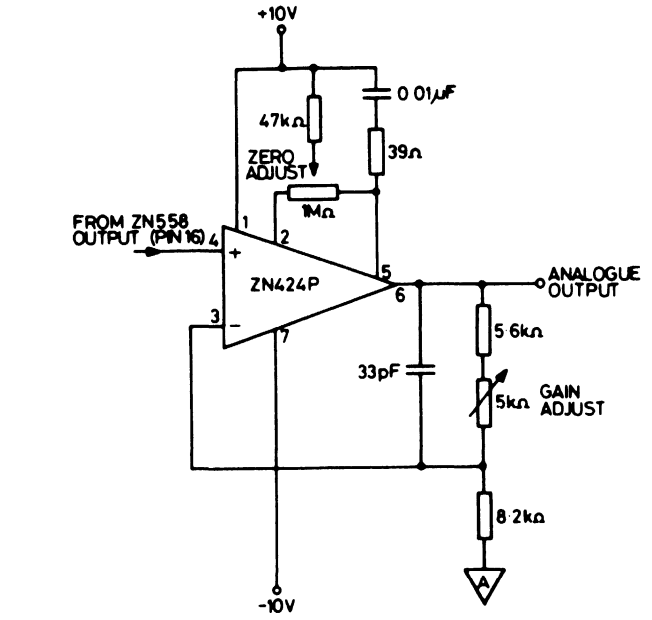


Fig. 6 Unipolar operation - basic circuit



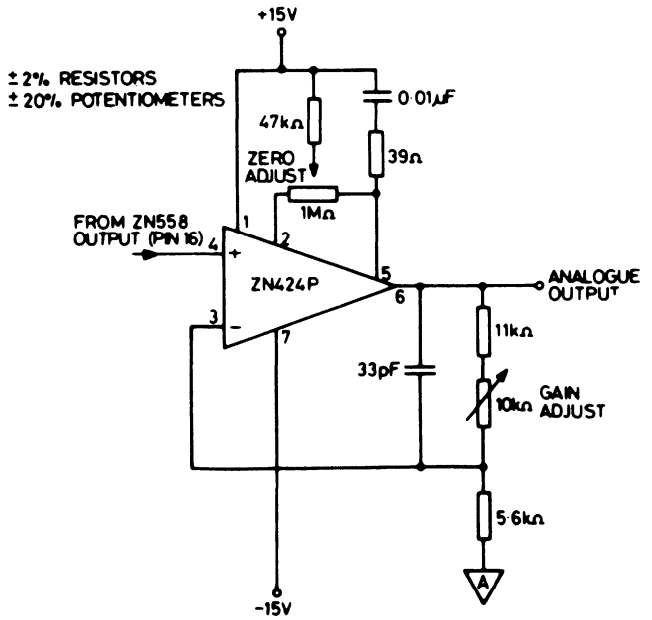


Fig. 7 Unipolar operation - component values

UNIPOLAR ADJUSTMENT PROCEDURE

(i) Set all bits to OFF (low) with $\overline{\text{enable}}$ low and adjust zero until $V_{OUT} = 0.0000V$.
(ii) Set all bits ON (high) and adjust gain until $V_{OUT} = FS - 1LSB$.

UNIPOLAR SETTING UP POINTS

Output range, +FS	LSB	FS - 1LSB
+5V	19.5mV	4.9805V
+10V	39.1mV	9.9609V

$$1LSB = \frac{FS}{256}$$

UNIPOLAR LOGIC CODING

Input code (Binary)	Analogue output (Nominal value)
11111111	FS - 1LSB
11111110	FS - 2LSB
11000000	¾ FS
10000001	½FS + 1LSB
10000000	½FS
01111111	½FS - 1LSB
01000000	¼FS
00000001	1LSB
00000000	0

(2) Bipolar D-A converter

For bipolar operation the output from the ZN558 is offset by half full scale by connecting a resistor R_3 between $V_{REF\ IN}$ and the inverting input of the buffer amplifier (Fig. 8).

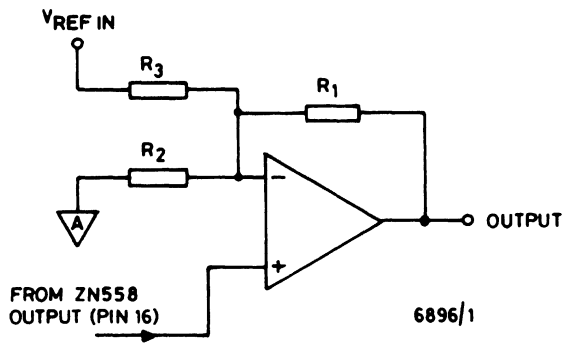


Fig. 8 Bipolar operation - basic circuit

When the digital input to the ZN558 is zero the analogue output is zero and the amplifier output should be − full scale. An input of all ones to the D-A will give a ZN558 output of $V_{REF\ IN}$ and the amplifier output required is + full scale. Also, to match the ladder resistance the parallel combination of R_1, R_2 and R_3 should be 4kΩ.

The nominal values of R_1, R_2 and R_3 which meet these conditions are given by

$R_1 = 8Gk\Omega$, $R_2 = 8G/(G-1)k\Omega$ and $R_3 = 8k\Omega$

where the resultant output range is $\pm G\ V_{REF\ IN}$.

A bipolar output range of $\pm V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $V_{REF\ IN}$) is obtained if $R_1 = R_3 = 8k\Omega$ and $R_2 = \infty$.

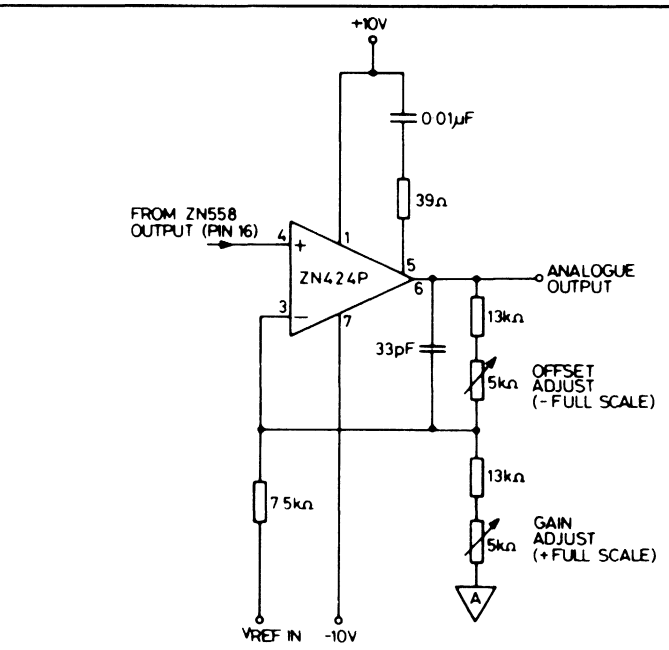
Assuming that $V_{REF\ IN} = 2.5V$ the nominal values of resistors for ± 5 and ± 10V output ranges are given in the following table:

Output range	G	R_1	R_2	R_3
± 5V	2	16kΩ	16kΩ	8kΩ
± 10V	4	32kΩ	10.66kΩ	8kΩ

Minus full scale (offset) is set by adjusting R_1 about its nominal value relative to R_3. Plus full scale (gain) is set by adjusting R_2 relative to R_1.

Practical circuit realisations are given in Fig. 9.

Note that in the ± 5V case R_3 has been chosen as 7.5kΩ (instead of 8.2kΩ) to get a more symmetrical range of adjustment using standard potentiometers. Settling time for a major transition is 1.5μs typical.



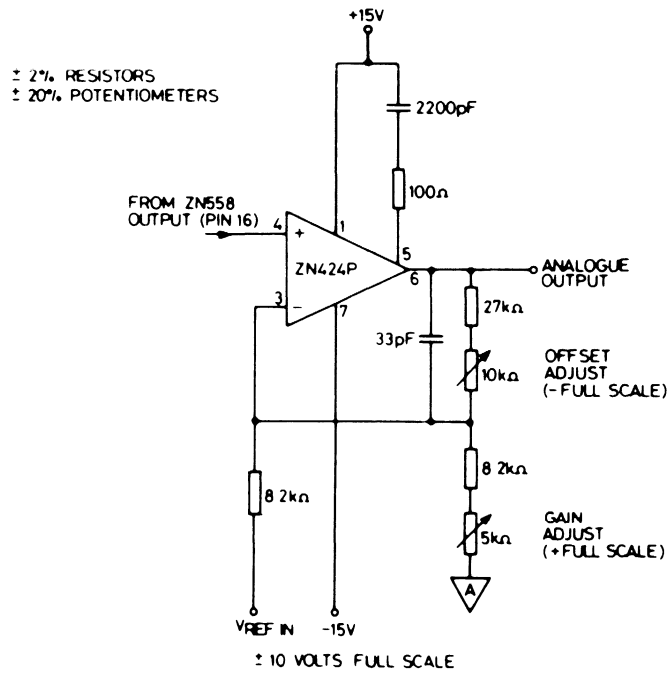


Fig. 9 Bipolar operation - component values

Bipolar Adjustment Procedure

(1) Set all bits to OFF (low) with $\overline{\text{enable}}$ low and adjust offset until the amplifier output reads −full scale.

(2) Set all bits ON (high) and adjust gain until the amplifier output reads +(full scale - 1LSB).

BIPOLAR SETTING UP POINTS

Input range, ±FS	LSB	−FS	+(FS - 1LSB)
±5V	39.1mV	−5.0000V	+4.9609V
±10V	78.1mV	−10.0000V	+9.9219V

$$1LSB = \frac{2FS}{256}$$

BIPOLAR LOGIC CODING

Input code (Offset binary)	Analogue output (Nominal value)
11111111	+(FS - 1LSB)
11111110	+(FS - 2LSB)
11000000	+½FS
10000001	+1LSB
10000000	0
01111111	−1LSB
01000000	−½FS
00000001	−(FS - 1LSB)
00000000	−FS

PLESSEY
Semiconductors

ZN559

LOW COST 8-BIT LATCHED INPUT MONOLITHIC D-A CONVERTER

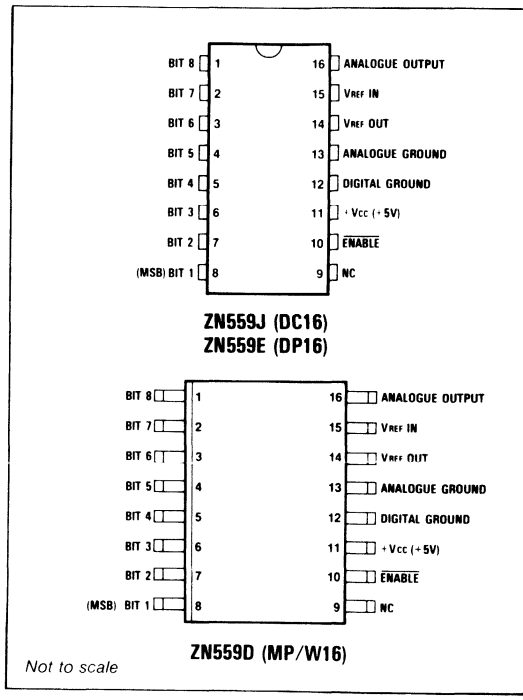
The ZN559 is a low cost 8-bit D-A converter with input latches to facilitate updating from a data bus. The latch is transparent when enable is LOW and the data is held when enable is taken HIGH. The device has a precision 2.5V voltage reference, the use of which is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.

FEATURES

- Low Cost DAC with Data Latch and On-Chip Reference
- Guaranteed Monotonic over the Full Operating Temperature Range
- Complementary to the ZN449 ADC
- 800ns Settling Time
- Single +5V Supply
- Microprocessor, TTL and 5V CMOS Compatible
- Commerical and Military Temperature Ranges

ORDERING INFORMATION

Device type	Operating temperature	Package
ZN559D	0°C to +70°C	MP16
ZN559E-8	0°C to +70°C	DP16
ZN559J-8	-55°C to +125°C	DC16



Pin connections - top view

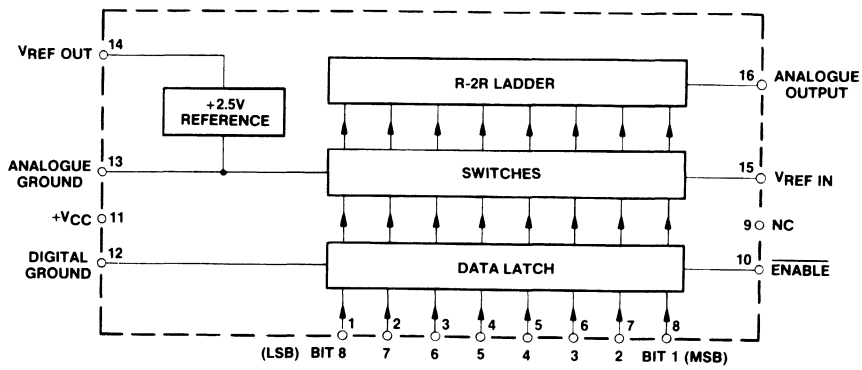


Fig.1 System diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	+7.0V
Max. voltage, logic and V_{REF} input	$+V_{CC}$
Operating temperature range	0 to +70°C (ZN559E & ZN559D)
	−55 to +125°C (ZN559J)
Storage temperature range	−55 to +125°C
Analogue ground to digital ground	±200mV

ELECTRICAL CHARACTERISTICS (V_{CC} = +5V, T_{amb} = 25°C unless otherwise specified).

Parameter	Min.	Typ.	Max.	Units	Conditions
Internal voltage reference					
Output voltage	2.475	2.550	2.625	V	R_{REF} = 390Ω, C_{REF} = 1μF
Slope resistance		0.5	2	Ω	
$V_{REF\ OUT}$ T.C.		50		ppm/°C	
Reference current	4		15	mA	Note 1
D-A converter					
Linearity error			±1.0	LSB	2.0V ≤ $V_{REF\ IN}$ ≤ 3.0V
Differential non-linearity		±0.5	±0.75	LSB	
Linearity error T.C.		±3		ppm/°C	
Differential non-linearity T.C.		±6		ppm/°C	
Offset voltage ZN559E		3	6	mV	All bits OFF
ZN559D		3	6	mV	All bits OFF
ZN559J		3	6	mV	All bits OFF
Offset voltage T.C.		±6		μV/°C	
Full scale output	2.540	2.550	2.560	V	External reference $V_{REF\ IN}$ = 2.560V, all bits ON
Full scale output T.C.		2		ppm/°C	
Analogue output resistance		4		kΩ	
External reference voltage	0		3.0	V	
Settling time to 0.5 LSB		800		ns	1 LSB major transition (note 2)
		1.25		μs	All bits ON to OFF or OFF to ON (note 2)
Operating temperature range:					
ZN559E & ZN559D	0		70	C	
ZN559J	−55		125	C	
Supply voltage (V_{CC})	4.5	5.0	5.5	V	

Note 1 See REFERENCE

Note 2 R_L = 10MΩ, C_L = 10pF.

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	Min.	Typ.	Max.	Units	Conditions
Supply current		20	30	mA	Note 3
Power consumption		100		mW	
Logic (over specified operating temperature range)					
High level input voltage V_{IH}	2.0			V	
Low level input voltage V_{IL}			0.8	V	
High level input current I_{IH}			60	μA	$V_{IN}=5.5V$, $V_{CC}=$ Max.
			20	μA	$V_{IN}=2.4V$, $V_{CC}=$ Max.
Low level input current I_{IL}			−5	μA	$V_{IN}=0.4V$, $V_{CC}=$ Max.
Input clamp diode voltage		−1.5		V	$I_{IN}=-8mA$
Enable pulse width	100			ns	
Data set-up time	150			ns	Note 4
Data hold time	10			ns	Note 5

Note 3 All inputs HIGH ($V_{IH}=3.5V$).
Note 4 Set up time before $\overline{\text{enable}}$ goes high.
Note 5 Hold time after $\overline{\text{enable}}$ goes high.

D-A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 2. Each 2R element is connected to 0V or $V_{REF\,IN}$ by transistor voltage switches specially designed for low offset voltage (< 1mV). A binary weighted voltage is produced at the output of the R-2R ladder.

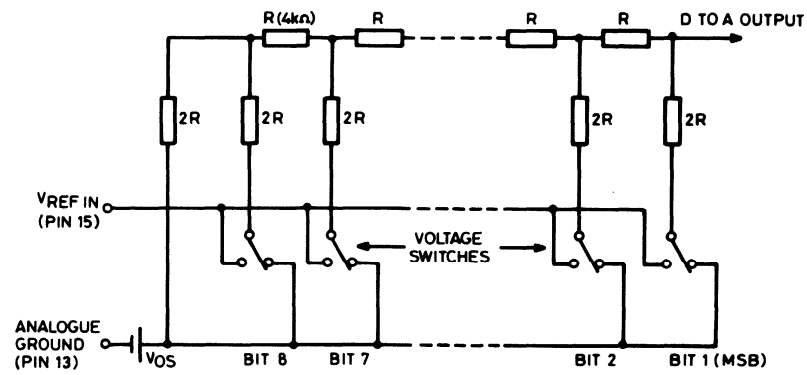


Fig. 2 The R-2R ladder network

Analogue output = $\frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$

where n is the digital input to the D-A from the data latch.

V_{OS} is a small offset voltage produced by the D-A switch currents flowing through the package lead resistance. The value of V_{OS} is typically 1mV. This offset will normally be removed by the setting up procedure (see APPLICATIONS section) and because the offset temperature coefficient is low ($\pm 6\mu V/°C$) the effect on accuracy is negligible.

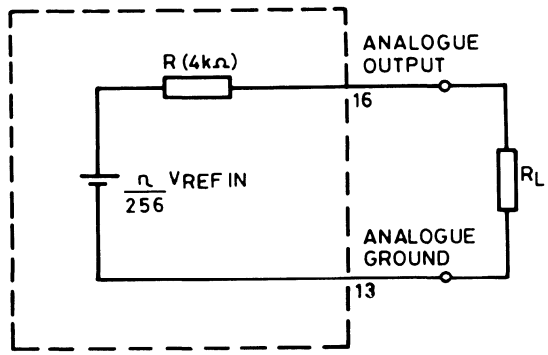


Fig. 3 Analogue output equivalent circuit

Fig. 3 shows an equivalent circuit of the output (ignoring V_{OS}). The output resistance R has a temperature coefficient of +0.2% per °C.

The gain drift due to this is $\frac{0.2R}{R+R_L}$ % per °C

R_L should be chosen to be as large as possible to make the gain drift small. As an example if $R_L = 400k\Omega$ then the gain drift due to the T.C. of R for a 100°C change in ambient temperature will be less than 0.2%. Alternatively the ZN559 can be buffered by an amplifier (see APPLICATIONS section).

REFERENCE

(a) Internal reference

The internal reference is an active band gap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig. 4). A resistor (R_{REF}), should be connected between $+V_{CC}$ (pin 11) and pin 14. The recommended value of 390Ω will supply a nominal reference current of (5.0-2.5)/0.39 = 6.4mA. A stabilising/decoupling capacitor $C_{REF} = 1\mu F$ is required between pins 14 and 13 for internal reference option, $V_{REF\ OUT}$ (pin 14) being connected to $V_{REF\ IN}$ (pin 15).

Up to five ZN559's may be driven from one internal reference (there is no need to reduce R_{REF}). This useful feature saves power and gives excellent gain tracking between the converters.

(b) External reference

If required an external reference voltage may be connected to $V_{REF\ IN}$. The slope resistance of such a reference source should be less than $\frac{2.5\Omega}{n}$, where n is the number of converters supplied.

$V_{REF\ IN}$ can be varied from 0 to +3V for ratiometric operation. The ZN559 is guaranteed monotonic for $V_{REF\ IN}$ above 2V.

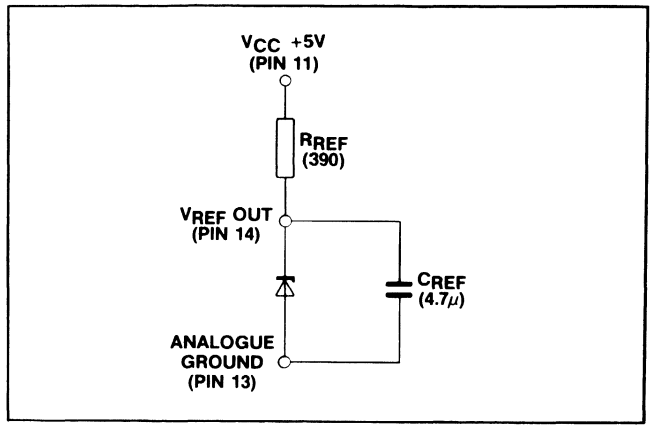


Fig. 4 Internal voltage reference

LOGIC

Input coding is binary for unipolar operation and offset binary for bipolar operation. When the enable input is low the data inputs drive the D-A directly. When enable goes high the input data word is held in the data latch.

The equivalent circuit for the data and clock inputs is shown in Fig.5.

The ZN559 is provided with seperate analogue and digital ground connections. The circuit will operate correctly with as much as ±200mV between the two grounds.

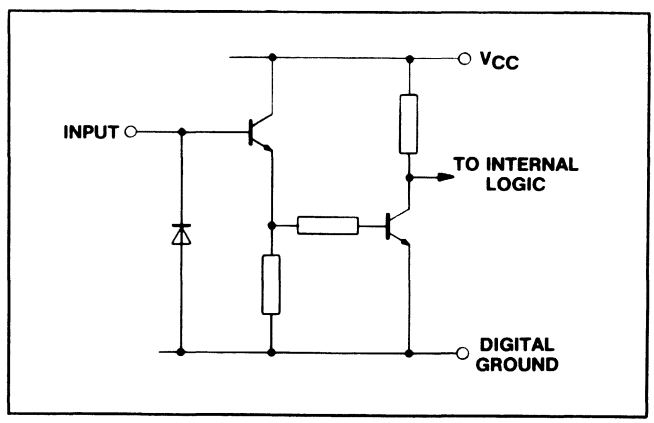


Fig. 5 Equivalent circuit of all inputs

APPLICATIONS

In some applications the standard 0 to $V_{REF\ IN}$ output voltage range and drive capability are not suitable, and other output ranges, both unipolar and bipolar are required.

To maintain flexibility two types of operational amplifier are illustrated; the industry standard 741 and a low cost pin-compatible alternative with a JFET input, the LF351. The LF351 features a high slew rate of 13V/μs, which gives a faster potential settling time than the 741. To keep drift to a minimum when using the 741, the external range setting resistors are calculated to match them to the 4KΩ ladder output impedance. This is not a consideration with the LF351, as the input offset current change with temperature is negligible for the impedances concerned. The resistor values for the LF351 were chosen to keep the output ringing to a minimum; a problem sometimes encountered with high slew rate op-amps. It is only the relative and not the absolute values of these resistors which set the range, and therefore can be changed as long as their ratios remain the same.

1) Unipolar operation

The general scheme for unipolar operation is shown in Fig. 6 and is suitable for amplifiers with input bias currents less than 1.5μA.

The resulting full scale range is given by

$$V_{OUT}\ FS = \left|1 + \frac{R1}{R2}\right| (V_{REF\ IN} - 1LSB)$$
$$= G\ (V_{REF\ IN} - 1LSB)$$

The impedance at the inverting input is R1//R2 and for low drift with temperature (741 only), this parallel combination should be equal to the ladder resistance (4kΩ).

The required nominal values of R1 and R2 are therefore given by $R1 = 4GkΩ$ and $R_2 = 4G/(G-1)kΩ$.

Using these relationships a table of nominal resistance values for R_1 and R_2 can be constructed for $V_{REF\ IN} = 2.5V$.

Output range	G	R_1	R_2
+ 5V	2	8kΩ	8kΩ
+ 10V	4	16kΩ	5.33kΩ

For gain setting R_1 is adjusted about its nominal value. Practical circuit realisations for + 5 and + 10V output ranges are given in Figs. 7 & 8

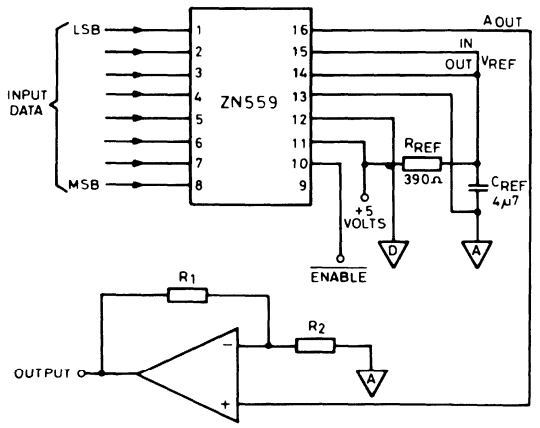
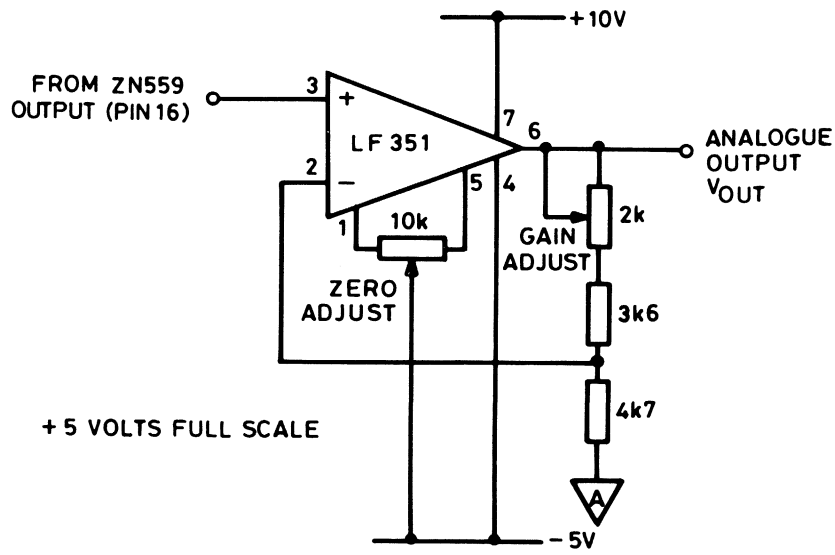
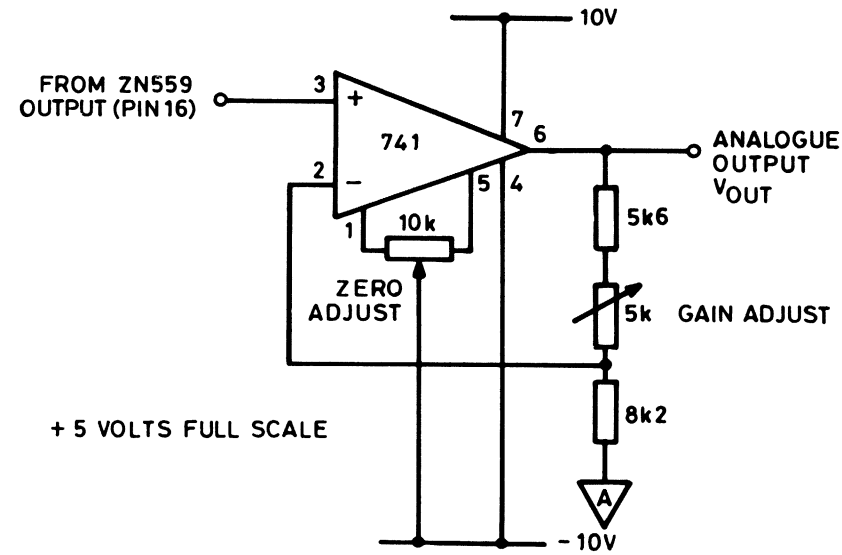


Fig. 6 Unipolar operation - basic circuit

RESISTORS ± 2%
POTENTIOMETERS ± 20%



a) Using an LF351



b) Using a 741

Fig. 7 + 5V full scale unipolar operation - component values

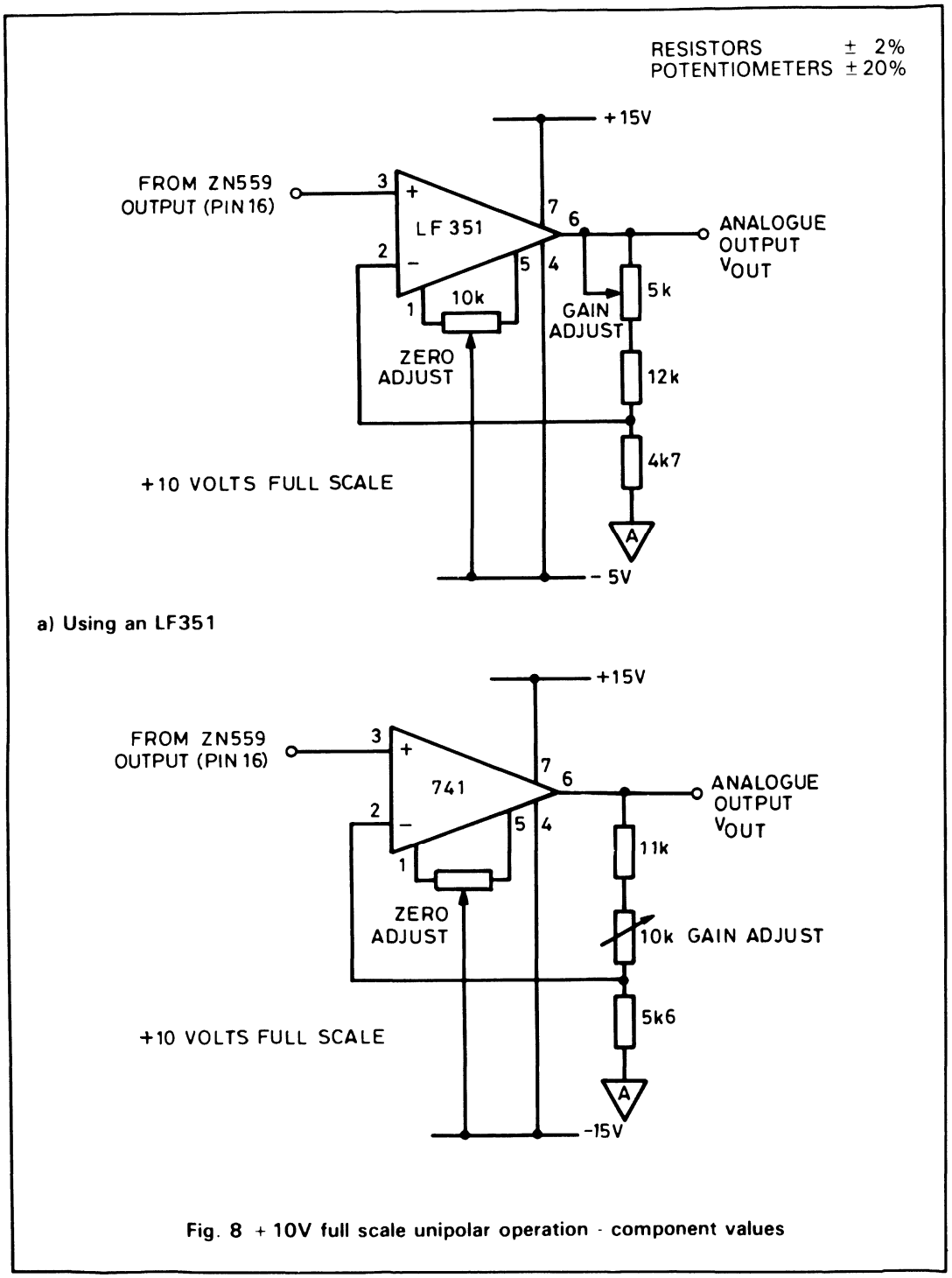


Fig. 8 + 10V full scale unipolar operation - component values

UNIPOLAR ADJUSTMENT PROCEDURE

(i) Set all bits to OFF (low) with $\overline{\text{enable}}$ low and adjust zero until $V_{OUT} = 0.0000V$.

(ii) Set all bits ON (high) and adjust gain until $V_{OUT} = FS - 1LSB$.

UNIPOLAR SETTING UP POINTS

Output range, +FS	LSB	FS - 1LSB
+5V	19.5mV	4.9805V
+10V	39.1mV	9.9609V

$$1LSB = \frac{FS}{256}$$

UNIPOLAR LOGIC CODING

Input code (Binary)	Analogue output (Nominal value)
11111111	FS - 1LSB
11111110	FS - 2LSB
11000000	¾ FS
10000001	½FS + 1LSB
10000000	½FS
01111111	½FS - 1LSB
01000000	¼FS
00000001	1LSB
00000000	0

(2) Bipolar operation

For bipolar operation the output from the ZN559 is offset by half full scale by connecting a resistor R_3 between $V_{REF\ IN}$ and the inverting input of the buffer amplifier (Fig. 9).

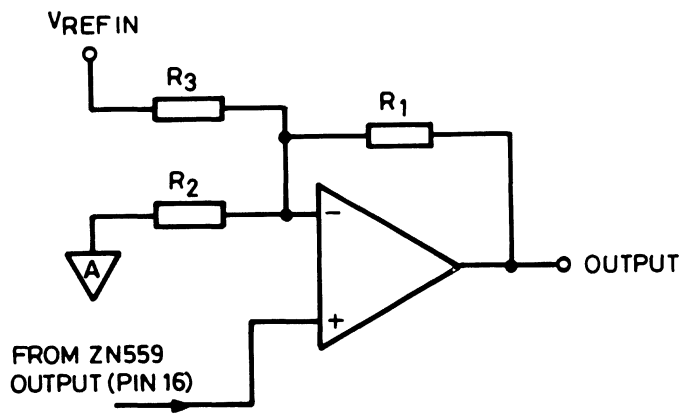


Fig. 9 Bipolar operation - basic circuit

When the digital input to the ZN559 is zero the analogue output is zero and the amplifier output should be – full scale. An input of all ones to the D-A will give a ZN559 output of $V_{REF\ IN}$ – 1LSB and an amplifier output of + full scale. When using the 741, the parallel combintion of R_1, R_2, and R_3 should match the 4kΩ ladder resistance.

The nominal values of R_1, R_2 and R_3 which meet these conditions are given by

$R_1 = 8Gk\Omega$, $R_2 = 8G/(G-1)k\Omega$ and $R_3 = 8k\Omega$

where the resultant output range is $\pm G\ V_{REF\ IN}$.

A bipolar output range of $\pm V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $V_{REF\ IN}$) is obtained if $R_1 = R_3 = 8k\Omega$ and $R_2 = \infty$.

Assuming that $V_{REF\ IN} = 2.5V$ the nominal values of resistors for ± 5 and ± 10V output ranges are given in the following table:

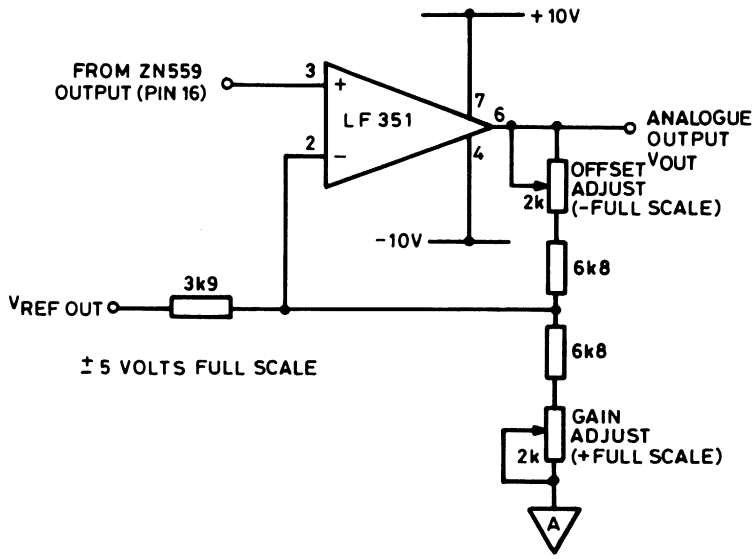
Output range	G	R_1	R_2	R_3
± 5V	2	16kΩ	16kΩ	8kΩ
± 10V	4	32kΩ	10.66kΩ	8kΩ

Minus full scale (offset) is set by adjusting R_1 about its nominal value relative to R_3. Plus full scale (gain) is set by adjusting R_2 relative to R_1.

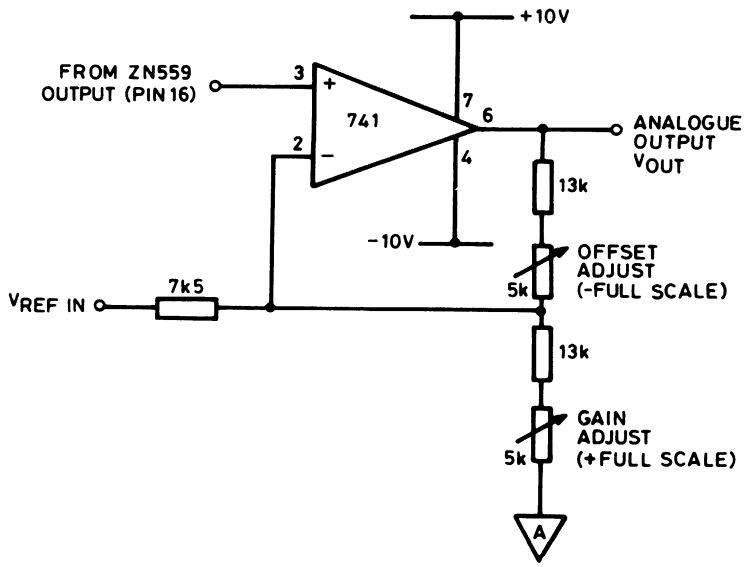
Practical circuit realisations are given in Figs. 10 & 11.

Note that in the ± 5V case (741 only), R_3 has been chosen as 7.5kΩ (instead of 8.2kΩ) to give a more symmetrical range of adjustment using standard potentiometers.

RESISTORS ± 2%
POTENTIOMETERS ± 20%



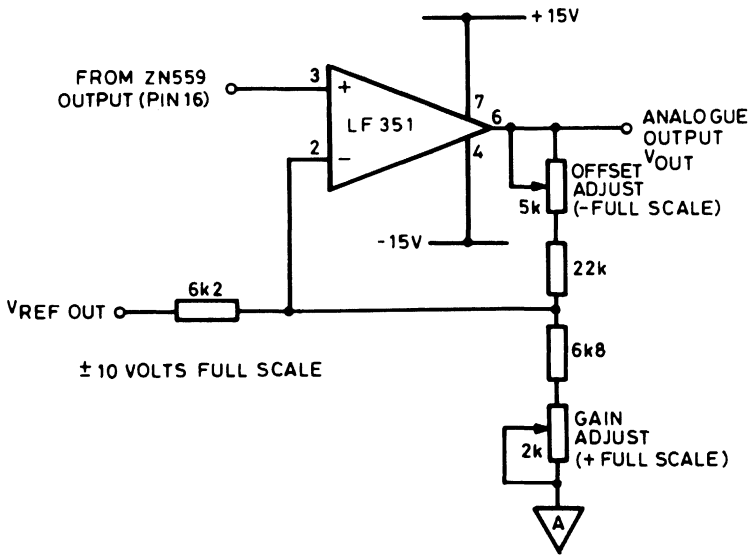
a) Using an LF351



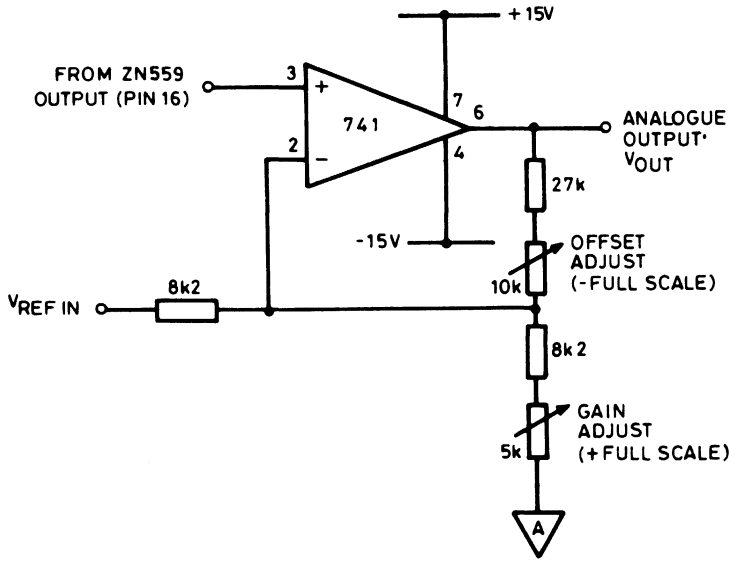
b) Using a 741

Fig. 10 ±5V full scale bipolar operation - component values

RESISTORS ± 2%
POTENTIOMETERS ± 20%



a) Using an LF351



b) Using a 741

Fig. 11 ± 10V full scale bipolar operation - component values

Bipolar Adjustment Procedure

(i) Set all bits to OFF (low) with $\overline{\text{enable}}$ low and adjust offset until the amplifier output reads −full scale.

(ii) Set all bits ON (high) and adjust gain until the amplifier output reads +(full scale - 1LSB).

BIPOLAR SETTING UP POINTS

Input range, ±FS	LSB	−FS	+(FS - 1LSB)
±5V	39.1mV	−5.0000V	+4.9609V
±10V	78.1mV	−10.0000V	+9.9219V

$$1LSB = \frac{2FS}{256}$$

BIPOLAR LOGIC CODING

Input code (Offset binary)	Analogue output (Nominal value)
11111111	+(FS - 1LSB)
11111110	+(FS - 2LSB)
11000000	+½FS
10000001	+1LSB
10000000	0
01111111	−1LSB
01000000	−½FS
00000001	−(FS - 1LSB)
00000000	−FS

ZN6012

LOW COST MONOLITHIC 12-BIT DAC

The ZN6012 is an industry standard monolithic 12-bit digital to analog converter available in a 20 pin plastic DIL. A fast settling time combined with complementary current outputs make the ZN6012 suitable for a wide range of applications including process control circuitry and fast ADCs. A segmented design technique guarantees monotonicity without the need for precision trimming of internal components making the device ideal for cost sensitive applications requiring fine local resolution.

FEATURES

- 12 Bit Monotonic over Temperature
- 600ns Settling Time
- Full Scale Current
- TTL/CMOS Compatible Inputs
- Complementary Current Outputs
- Industry Standard Pinout
- Low Cost

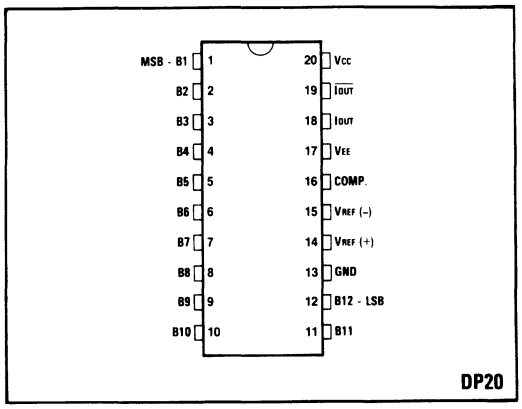


Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Operating temperature range	-40°C to +85°C
Storage temperature range	-55°C to +125°C
Supply voltage +Vcc	+7V
-Vcc	-18V

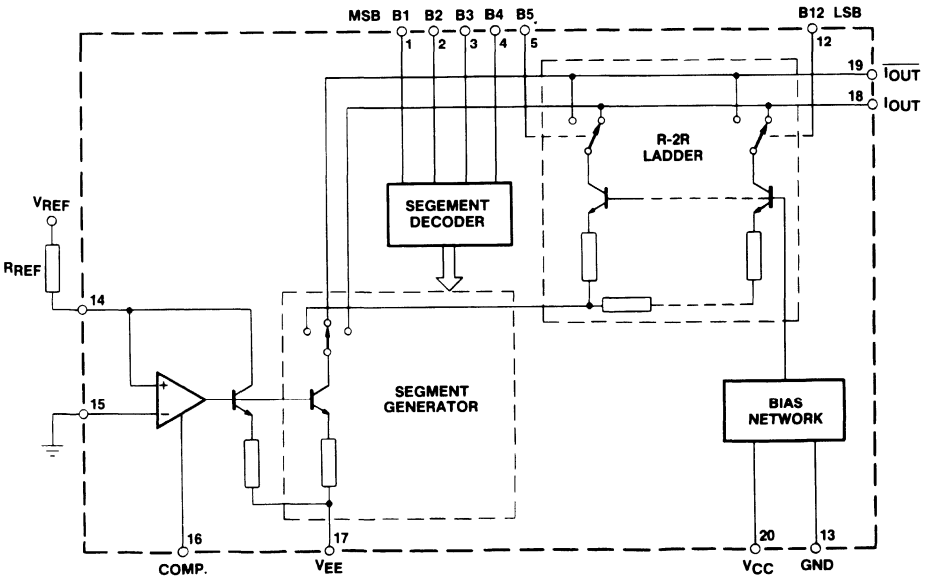


Fig.2 ZN6012 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = +5V, V_{EE} = -15V, I_{REF} = 1.0mA, T_{amb} = -40°C to +85°C

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Resolution		12	12	12	Bits	
Monotonicity		12	12	12	Bits	
Differential nonlinearity	DNL	-	-	±0.025	%FS	Deviation from ideal step size
		12	-	-	Bits	
Nonlinearity	NL	-	-	±0.05	%FS	Deviation from ideal straight line
Full scale current	I_{FS}	-	3.999	-	mA	V_{REF} = 5V, R_{REF} = 5kΩ, T_{amb} = +25°C
Full scale temp.co.	TCI_{FS}	-	±5		ppm/°C	
		-	±0.0005		%FS°C	
Output voltage compliance	V_{OC}	-15	-	+2.5	V	DNL specification guaranteed over compliance range
Setting time	t_S	-	600	-	ns	To ±½ LSB, all bits ON or OFF, T_{amb} = 25°C
Propagation delay - all bits	t_{PLH} t_{PHL}	-	200	-	ns	50% to 50%
Logic input levels Logic '0'	V_{IL}	-	-	0.8	V	
Logic '1'	V_{IH}	2.0	-	-	V	
Logic input current	I_{IL}	-	-130	-	μA	V_{CC} -5.5V, V_{IN} = 2.4V
Logic input current	I_{IH}	-	20	-	nA	V_{CC} = 5.5V, V_{IN} = 0.4V
Reference current range	I_{REF}	-	1.0	-	mA	
Reference bias current	I_{15}	0	0.01	-	μA	
Power supply sensitivity	$PSSI_{FS}$	-	±0.00005	±0.001	%FS/°C	V_S = (+4.5V to +5.5V) V_{EE} = -15V
	$PSSI_{FS}$	-	±0.00025	±0.001	%FS/°C	V_{EE} = -12V to -16V V_S = +5V
Power supply range	V_S	4.5	-	5.5	V	V_{OUT} = 0V
	V_{EE}	-16	-	-12	V	V_{OUT} = 0V
Power supply current	I+	-	18	-	mA	V_{CC} = +5V, V_{EE} = -15V
	I-	-	28	-	mA	V_{CC} = +5V, V_{EE} = -15V
Power dissipation	P_D	-	510	-	mW	V_S = +5V, V_{EE} = -15V

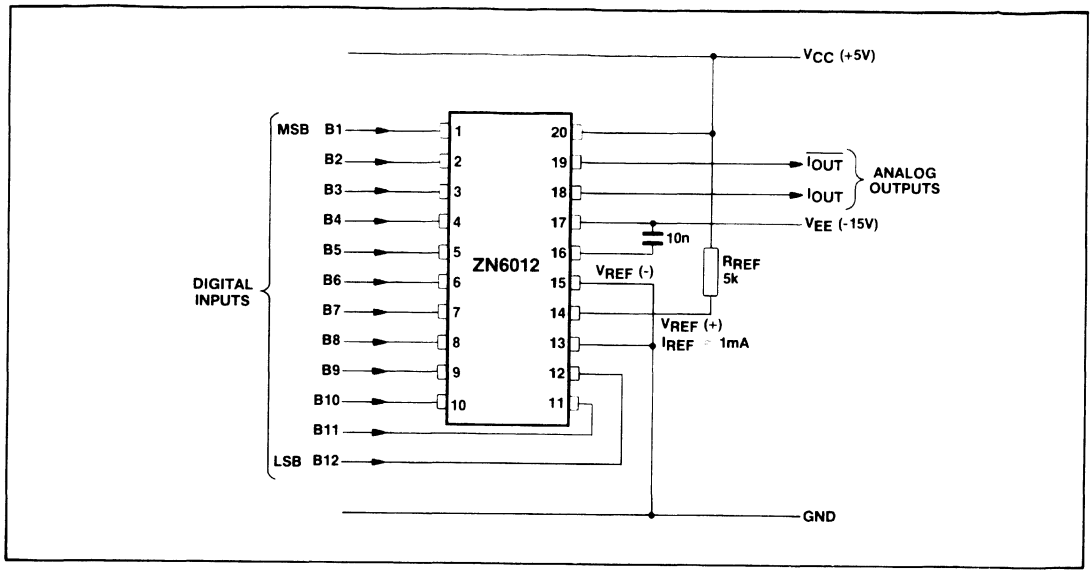


Fig.3 ZN6012 external components

PLESSEY
Semiconductors

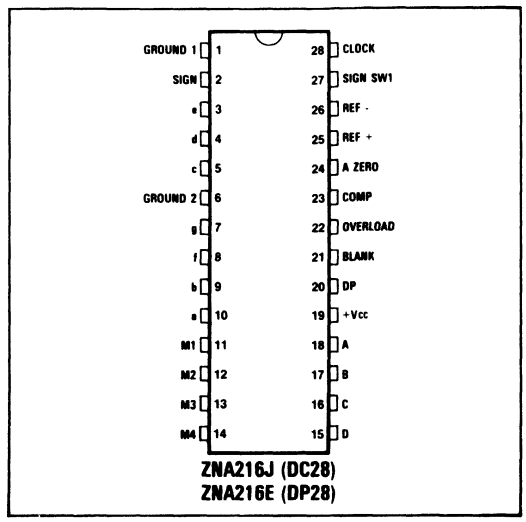
ZNA216

LOW POWER 3¾ DIGIT DVM INTEGRATED CIRCUIT

The ZNA216 DVM IC is a versatile DVM system component which contains all the control logic necessary to construct a dual-slope digital voltmeter, whilst leaving the designer free to configure the analogue circuitry to his own requirements.

The IC has multiplexed data outputs, both in BCD format and in seven-segment format for direct drive of LED displays. A number of useful features are incorporated into the device, including leading zero blanking of the display, flashing overrange indication and an auto zero facility which removes the need for manual zero adjustment.

Apart from the more obvious applications of DVM and DPM the IC can be used to construct any other instrument where an analogue input from, say, a transducer is to be converted into a digital reading, for example a digital thermometer. The ZNA216 may also be used as an A-D converter in single-channel data acquisition systems, or to interface to a microprocessor system.

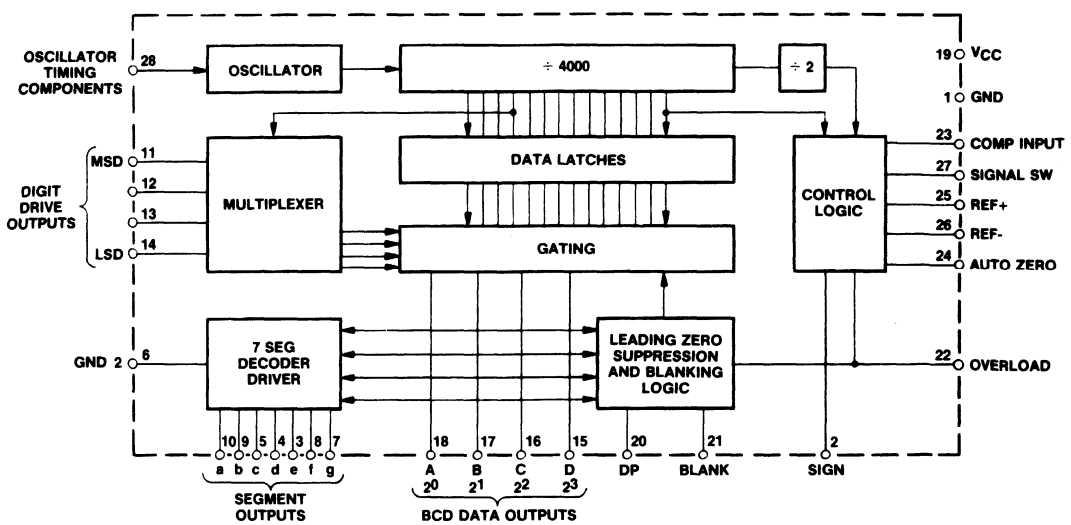


ZNA216J (DC28)
ZNA216E (DP28)

Pin connections - top view

FEATURES

- 3¾ Digit Display (±3999 Max. Reading)
- Automatic Zero Adjustment with 1μV/ °C Temperature Coefficient
- Seven-Segment Outputs for Direct Drive of LED Displays
- BCD Outputs
- Automatic Polarity Detection and Indication
- Flashing Overload Indication, Separate Overload Output
- Blanking Input, e.g. For Low Battery Indication
- Automatic Blanking of Display Leading Zeros
- On-Chip Clock, may be Externally Synchronised
- TTL and CMOS Compatible
- Single +5V Supply
- Pinning Optimised for Easy PCB Layout



System diagram

PINNING AND FUNCTIONAL DETAILS

Pin No.	Name	Function
1	Gnd 1	Supply 0 volts
2	Sign	Open collector output, goes low when −ve input voltage is being measured.
3	e	Open collector segment output, goes low when segment is on.
4	d	Segment output as above.
5	c	Segment output as above.
6	Gnd 2	0 volt supply for segment drivers, must be connected to pin 1.
7	g	Segment output as above.
8	f	Segment output as above.
9	b	Segment output as above.
10	a	Segment output as above.
11	M1	Digit drive output, goes low for the most significant digit to be displayed, first in digit scan sequence.
12	M2	Digit drive output, goes low for the second most significant digit to be displayed, second in digit scan sequence.
13	M3	Digit drive output, goes low for the third most significant digit to be displayed, third in digit scan sequence.
14	M4	Digit drive output, goes low for the least significant digit to be displayed, fourth in digit scan sequence.
15	D	2^3 BCD data output
16	C	2^2 BCD data output.
17	B	2^1 BCD data output.
18	A	2^0 BCD data output.
19	V_{CC}	Supply +5V.
20	DP	When this input is at logic 1, leading zeroes are blanked.
21	Blank	While this input is at logic 1, all segment outputs are off and all BCD data outputs are at logic 1.
22	Overload	If the integrator capacitor does not discharge before the counter reaches 4000, this output goes to logic 1.
23	Comp.	This input is connected to the output of the external comparator.
24	Azero	When this output is high, auto zero correction is applied to the integrator.

Pin No.	Name	Function
25	Ref +	When this output is at logic 1, the +ve reference voltage is connected to the integrator
26	Ref −	When this output is at logic 1, −ve reference voltage is connected to the integrator.
27	Signal switch	When this output is at logic 1, the input voltage to be measured is connected into the integrator.
28	Clock	The external clock oscillator components are connected to this pin (see diagrams). Alternatively, this pin may be driven by an external signal. A measurement is made every 8000 clock periods. The counter toggles on −ve going clock edges and transfer to the latches occurs at the first +ve going clock edge after comparison has been made which avoids false triggering from the integrator output. Maximum clock frequency 50kHz.

ABSOLUTE MAXIMUM RATINGS

Supply voltage	7.0V
Operating temperature	0 to +70°C
Storage temperature	−55 to +125°C

ELECTRICAL CHARACTERISTICS (at T_{amb} = 0 to +70°C, V_{CC} = 5V unless otherwise specified).

Parameter		Min.	Typ.	Max.	Units	Test conditions
Supply voltage		4.5		5.5	V	
Supply current				20	mA	
Low level input voltage	All inputs			0.8	V	
Low level input current	All inputs			−4	μA	V_{in} = 0V
Input clamp diode voltage	All inputs			−1.5 V_{CC} +1.5	V V	I_{in} = −12mA I_{in} = 10mA
High level input voltage	Oscillator RC input	2.5			V	
	All other inputs	2.0			V	
High level input current	Oscillator RC input			100	μA	V_{in} = 2.5V
	All other inputs			4	μA	V_{in} = 5.0V
Low level output voltage	a,b,c,d,e,f,g			0.8	V	I_{sink} = 20mA
	Sign			0.4	V	I_{sink} = 5mA
	Overload, Ref+, Ref−, azero, signal switch, a,b,c,d,M1,M2,M3,M4			0.4	V	I_{sink} = 1.6mA
High level output voltage	Overload, Ref+, Ref−, azero, signal switch, a,b,c,d,M1,M2,M3,M4	2.4			V	I_{out} = 10μA
			V_{CC} −0.1		V	I_{out} = 0
High level output current	a,b,c,d,e,f,g, sign			−10	μA	V_{out} = 5.0V

Note: Although the oscillator and logic will function up to 50kHz, this is not recommended as the analogue circuitry becomes more critical.

THE DUAL SLOPE SYSTEM

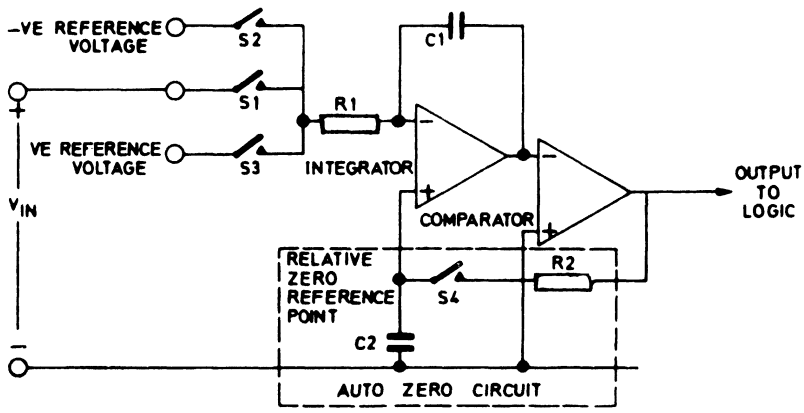


Fig. 1 Dual slope block diagram

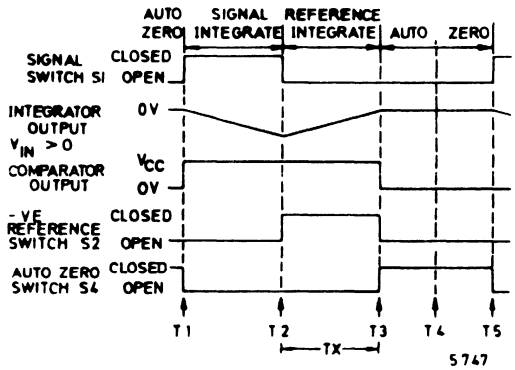


Fig. 2a Timing diagram for in-range input

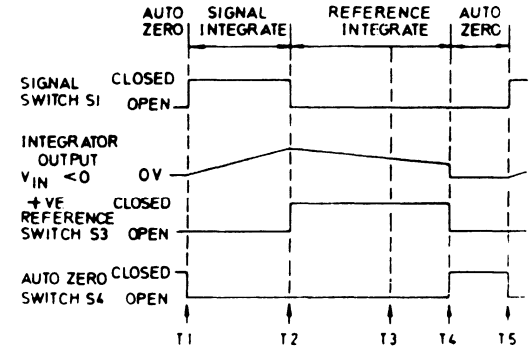


Fig. 2b Timing diagram for overrange input

Dual slope integration is a D.V.M. circuit technique designed to cancel out the effects of drift in circuit components. A block diagram of the analogue section of a dual-slope D.V.M. is shown in Fig. 1, whilst a timing diagram for its operation is shown in Fig. 2.

At time T_1, S1 is closed by the D.V.M. logic, connecting the input signal to the integrator until time T_2, which is 2000 clock periods after T_1. During this time the integrator output ramps positive or negative, depending on input voltage polarity, to a voltage

$$V_o = \frac{-V_{in} 2000\ t_c}{R_1 C_1}$$

where t_c is the clock period.

The polarity of the integrator output voltage during this period, and hence of the input voltage, is sensed by the comparator, whose output is connected to the control logic.

At time T_2, S1 is opened and, depending on the input voltage polarity, either S2 or S3 is closed. This connects a reference voltage of opposite polarity to V_{in} to the integrator input, so that the integrator output ramps back towards zero. The number of clock periods required for the integrator output to reach zero is counted by the D.V.M. counter. When the output reaches zero the comparator output changes state, S2 or S3 opens and the count is stopped. Since the second integration also takes place over a voltage V_o then,

$V_o = \frac{-V_{REF}\, nt_c}{R_1 C_1}$ where n is the count at time T_3

but V_o also equals $\frac{-V_{in}\ 2000 t_c}{R_1 C_1}$

$$\text{thus } n = \frac{2000\ V_{in}}{V_{REF}}$$

R_1, C_1 and t_c have disappeared from this final equation, so the accuracy of the D.V.M. is unaffected by the long-term stability of these parameters. The only factors influencing accuracy are the stability of V_{REF} and variations in the 'on' resistance of the analogue switches S1 to S3. The former can be assured by careful choice of a reference source, e.g. the Plessey ZN423 or ZN458, whilst the effect of the latter can be minimised by making R_1 large compared to the on resistance of S1 to S3.

If V_{REF} is exactly 2V then $n = 1000\ V_{in}$, i.e. the count will be equal to the input voltage in millivolts. For the ZNA216 the maximum reading is 3999. If a count of 4000 occurs before the integrator output reaches zero, as shown in Fig. 2b, then S2 or S3 will open and the overrange output will go high.

In a practical D.V.M., it is unlikely that a reference voltage of exactly 2V will be available, or an input range other than 3.999V may be required. In this case a different resistor value (R_{REF}) will be used for the reference integration. The equation then becomes:

$$n = \frac{2000\ V_{in} \cdot R_{REF}}{V_{REF} \cdot R_1}$$

R_1 and R_{REF} should be high-stability types.

AUTO ZERO

Any offset voltage and bias current in the integrator will be integrated along with the input signal and since, for example, a 3,999V D.V.M. has a resolution of 1mV an offset of a few hundred microvolts can lead to errors in the least significant digit. Manual zero adjustment is time-consuming and has to be repeated frequently due to temperature drift.

The auto zero of the ZNA216 operates during the period T_3 to T_5, or T_4 to T_5 in the case of an overrange input. S4 is closed, S1, S2 and S3 are opened so that only the integrator offset voltage is integrated, thus causing the integrator output to drift either positive or negative. The integrator output is amplified by the comparator (which is nothing more than an extremely high gain amplifier) and this charges C2 via R2 to apply a voltage to the non-inverting input of the integrator. The polarity of this voltage is such as to null out the effects of integrator offset voltage and bias current and thus cancel integrator drift. Depending on comparator gain a zero error of a few hundred nanovolts may be achieved by this method.

HUM REJECTION

Any mains hum pickup superimposed on the input signal will cause errors in the D.V.M. reading. However, if the period T_2-T_1 is made a multiple of the mains period then equal numbers of positive and negative half-cycles of the mains waveform will be integrated and will cancel each other out. For 50Hz mains T_2-T_1 should be 20ms or a multiple thereof, while for 60Hz mains T_2-T_1 should be 16.67ms or a multiple thereof.

Adjustment of the period T_2-T_1 is achieved by varying the frequency of the clock oscillator which controls the operation of the D.V.M.

DISPLAY MULTIPLEXING

The BCD and seven-segment data outputs are multiplexed, the data appearing in the sequence MSD to LSD. To identify which digit is present at the outputs at any time the four digit select outputs go low in turn, synchronous with the relevant digit appearing at the data outputs. The seven segment outputs can be used to drive the cathodes of a multiplexed common-anode LED display whilst the digit select outputs may be used to turn on digit drive transistors which activate each display digit in sequence.

DECIMAL POINT (ZERO BLANKING) INPUT

Before the start of each multiplex cycle a latch in the I.C. is set. This holds the display blanked until non-zero data appears at the BCD outputs, when the latch is reset and the display is unblanked. For example, if the MSD were non-zero the latch could reset immediatey the MSD appeared, so all four digits would be displayed. Conversely if the MSD were zero but the second digit were non-zero then the display would be blanked for the MSD and only three digits would appear. In this way leading zeroes in the display are suppressed. The LSD is always displayed whether zero or not.

The D.P. input can be used to override the zero blanking by taking this pin to logic '0'. This facility allows a correct display to be obtained when a decimal point is used.

For example, if the decimal point is to the left of the MSD then a low-going pulse to the D.P. input synchronous with the MSD output will cause all digits to the right of the decimal point to be displayed, whether zero or not. Thus, if the input voltage were, say .0056V then the display would be .0056. If the zero blanking were not overridden in this way the display would be .--56, which is clearly unsatisfactory.

OSCILLATOR CIRCUIT

The operation of the D.V.M. circuit is controlled by a clock oscillator, which provides drive for the counter, control logic and display multiplexing. Two external components, a resistor and a capacitor, are required to make the oscillator function. The oscillator temperature stability is typically $\pm 0.02\%$ per ^{o}C.

As mentioned earlier, the oscillator frequency should be chosen so that T_2-T_1 is a multiple of the mains period. It should not be chosen so low as to cause noticeable flicker in the display multiplexing, but on the other hand it should not be chosen too high or the design of the analogue circuitry becomes more critical.

The optimum oscillator frequency is 20kHz since this makes T_2-T_1 = 100ms which gives good hum rejection at either 50Hz or 60Hz. This frequency can be obtained by using the component values shown in Fig. 3. The potentiometer may be adjusted to give a frequency of 20kHz measured at pin 28, in which case a high impedance, low capacitance probe should be used to avoid loading the oscillator. Alternatively, the trimmer may be adjusted to give a frequency of 500Hz at any of the digit select outputs, when no special precautions are required.

If required the oscillator timing components may be omitted and the oscillator input may be driven by an external clock at TTL logic level.

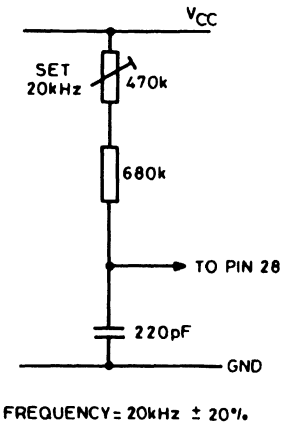


Fig. 3 Oscillator external components

INPUT AND OUTPUT CIRCUITS

Apart from the oscillator input (which is a Schmitt trigger type of circuit) all other inputs are as shown in Fig. 4a. All outputs are as shown in Fig. 4b, except for those designated as open-collector, which have no pull-up resistor.

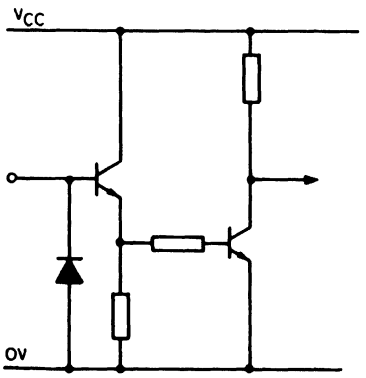


Fig. 4a Input circuit

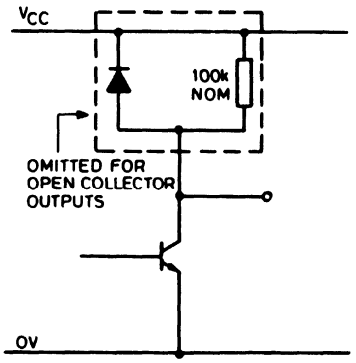


Fig. 5b Output circuit

DISPLAY DRIVING

The 20mA sink capability of the segment outputs allows common anode LED displays to be driven with a minimum of external components, as shown in Fig. 5. The segment current limit resistors should be chosen to give the desired segment current, allowing for the forward voltage drop of the LED, whilst the digit output resistors sould be chosen to give sufficient base current to saturate the digit drive transistors.

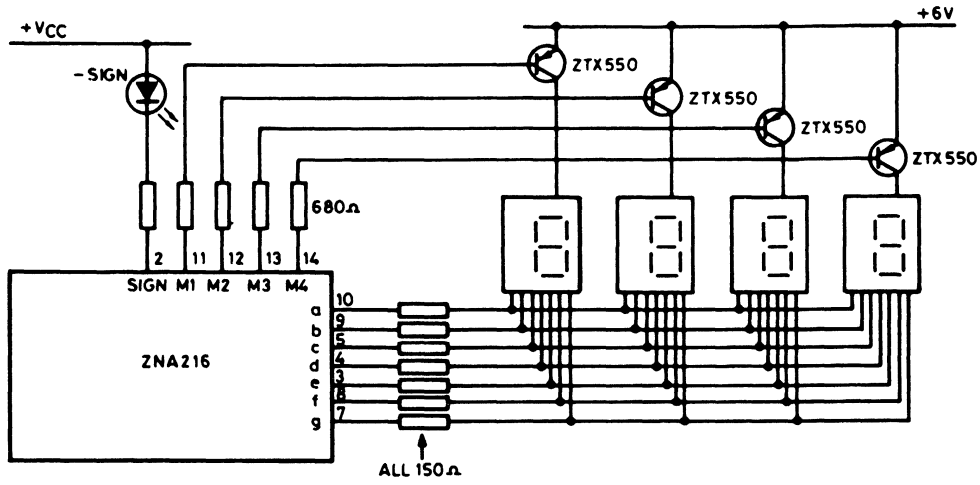


Fig. 5 Display drive circuit

OVERRANGE AND LOW BATTERY INDICATION

If the input voltage exceeds the full-scale range then the display will flash all 'eigths' and the overrange output, pin 22, will go high. Low battery indication may also be provided by the addition of the simple circuit shown in Fig. 6.

Whilst the battery voltage is above 4.4V T_1 will be turned on via R1 and R2. Below this voltage the base potential supplied by these resistors will be insufficient to turn on T_1 and it will then be turned on and off cyclically by the auto-zero output, causing the display to flash whatever reading is present.

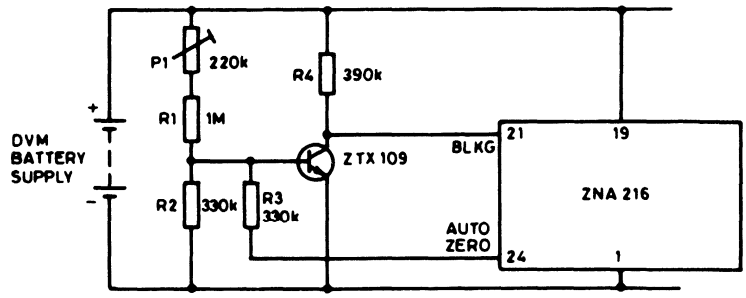


Fig. 6 Low battery indication

A PORTABLE D.V.M.

Fig. 7 shows the circuit of a battery-powered D.V.M. based on the ZNA216, which uses readily available components. ZN424 op-amps are used for the integrator and comparator, whilst bipolar silicon transistors are used for the analogue switches. The basic sensitivity of the instrument is 4V, and additional ranges of 40V and 400V are provided by means of an input attenuator. Printed circuit board and component layouts for the D.V.M. are given in Figs. 8a to 9b.

However, this circuit design should by no means be considered as immutable. Since the analogue circuitry is external to the ZNA216 it may be configured to suit the designer's needs to give higher input impedance, increased sensitivity etc.

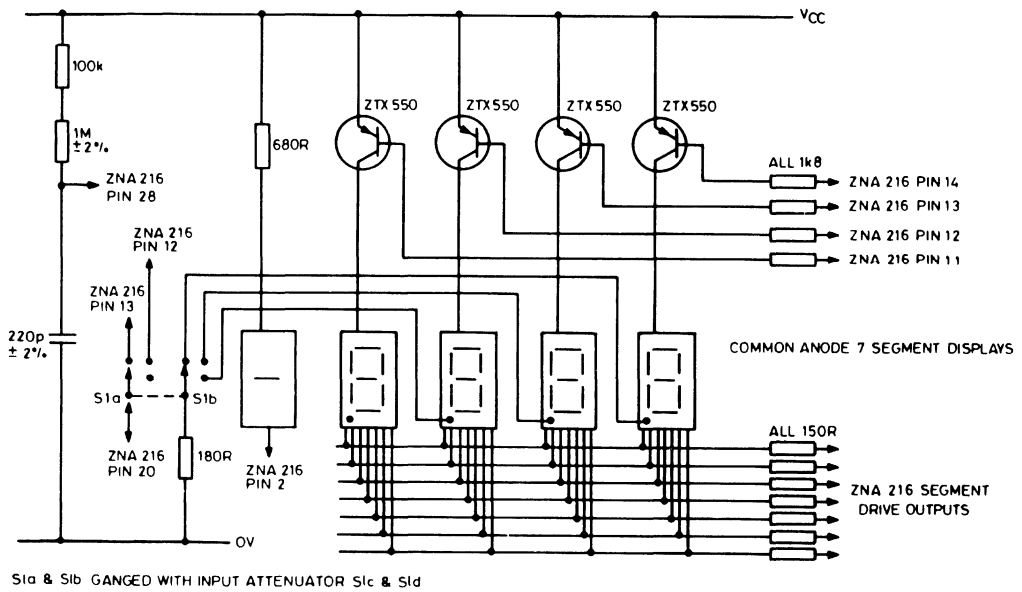


Fig. 7a Battery-powered D.V.M. circuit, display section

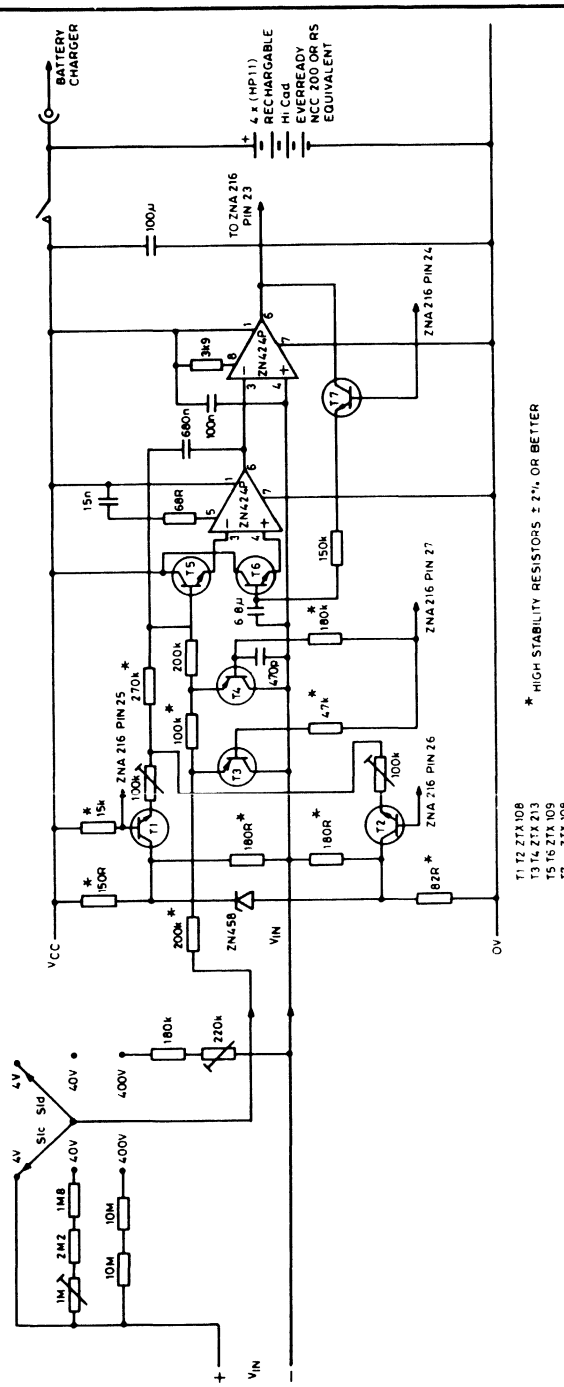


Fig. 7b Battery-powered D.V.M. circuit, analogue section

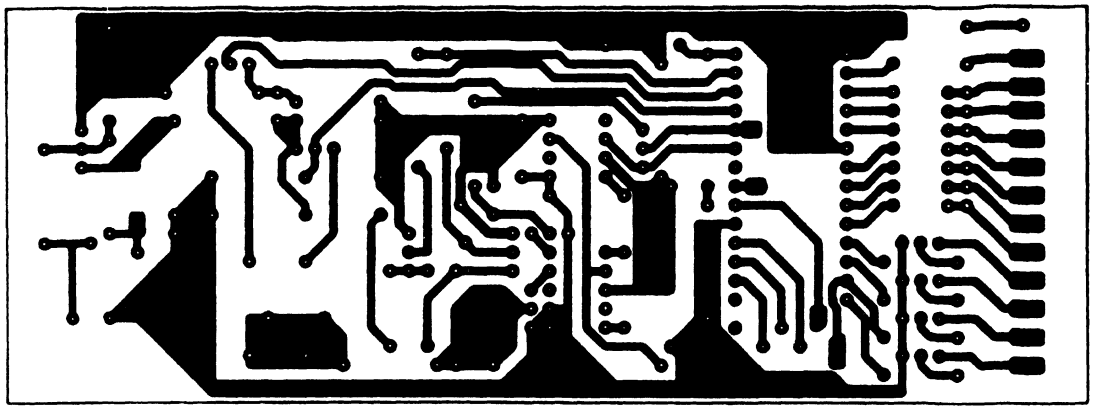


Fig. 8a D.V.M. Main board (1:1)

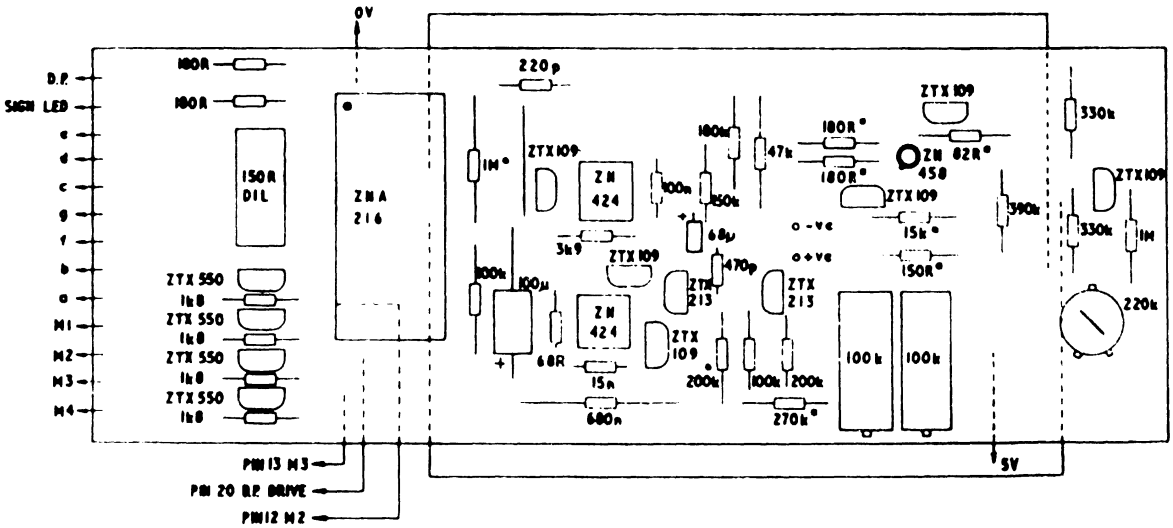


Fig. 8b Component layout for Fig. 8 (1:1)

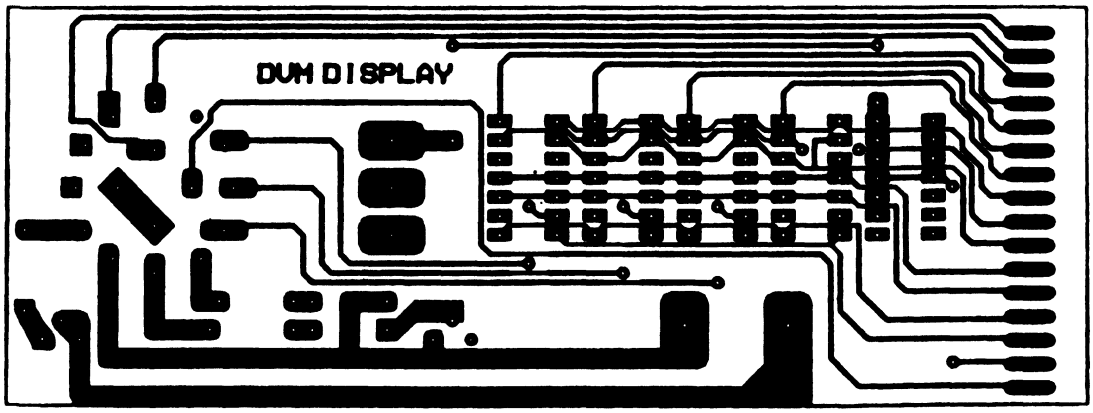


Fig. 9a D.V.M. display board (1:1)

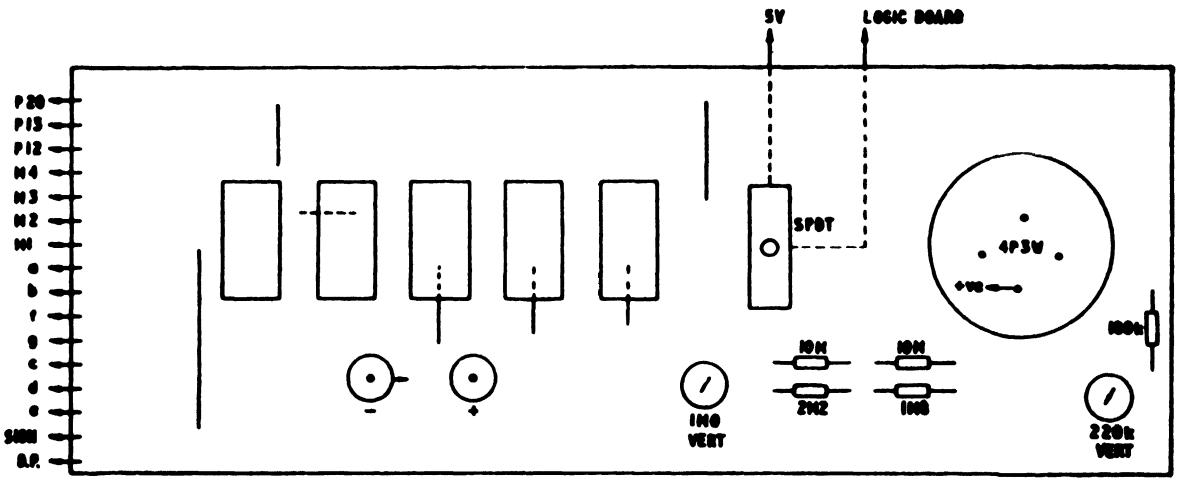


Fig. 9b Component layout for Fig. 9a (1:1)

MICROPROCESSOR INTERFACING

The ZNA216 may be used as a dual-slope A-D converter in data loggers and other data acquisition systems, where its 3¾ decade range offers a resolution comparable to a 13-bit binary ADC, but in a more convenient BCD format.

Fig. 10 is a block diagram which illustrates how the ZNA216 may be interfaced to an 8-bit microprocessor. The principle of operation is that the four multiplexed BCD digits of the ZNA216, plus the sign and overrange bits, are stored in four 4-bit latches so that they are available in parallel form. The contents of the latches can then be read into the microprocessor as two 8-bit words. The latches used are type 74173 which have three-state outputs for direct connection to the μP data bus. Data is clocked into the latches using the positive-going edge of the appropriate digit drive outputs.

The latches are treated as two memory locations by using an address decoder which is connected to their output enable pins. In this way data can be read out of the latches just as from any other memory locations. Once data is in the latches it may be read out whilst the ZNA216 performs the next measurement, thus eliminating any waiting time. The only time when data cannot be read out of the latches is just after the ZNA216 has completed a measurement. At this time the data in the internal latches of the ZNA216 will have been updated and the data in the 74173s may thus be changing. The data in the latches will be stable after two multiplexed cycles of the ZNA216 which is 4ms if a 20kHz clock is used.

Since the auto-zero output of the ZNA216 goes high when a measurement has been completed this output may be used as a BUSY signal. Data should not be read from the 74173 latches until at least 4ms after the auto-zero output has gone high.

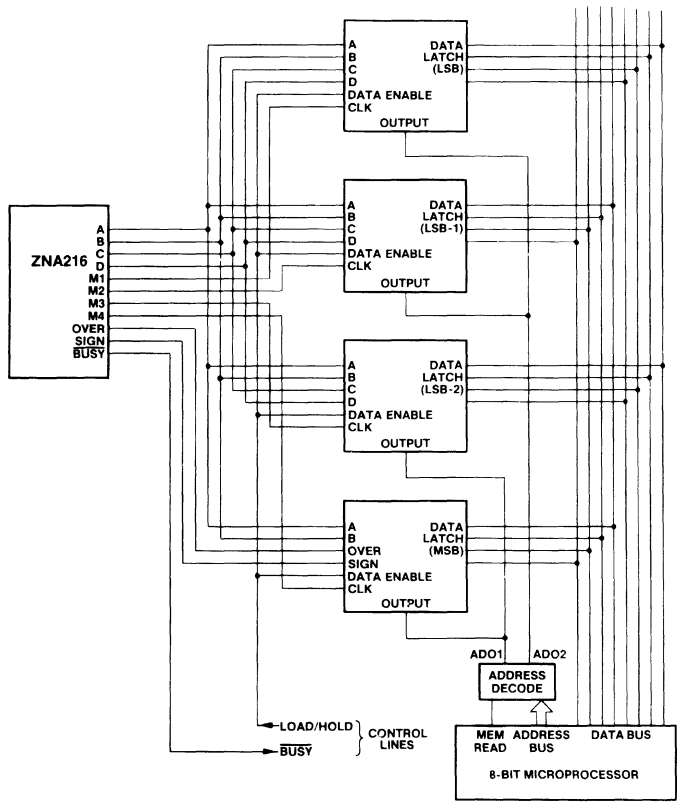


Fig. 10 Interfacing the ZNA216 to a microprocessor

Technical Data

2. Voltage references

PLESSEY
Semiconductors

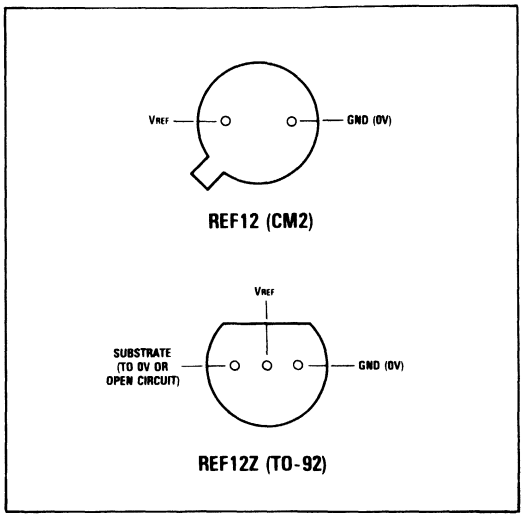
REF12/REF12Z

1.26V MICROPOWER PRECISION REFERENCES

The REF12 and REF12Z are integrated circuits using the bandgap principle to provide a precise reference voltage of 1.26V. There are two package options available: REF12 in 2-pin TO-18 metal can (CM2) and REF12Z in plastic 3-pin TO-92. These references feature a recommended operating current range of 90μA to 2.5mA which make them ideal for all low power and battery applications.

FEATURES

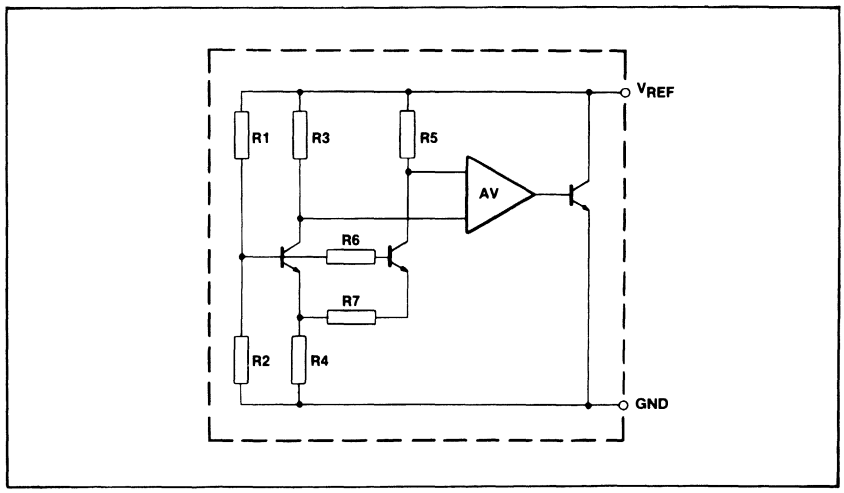
- Low Knee Current — Typically 80 microamps
- Ideal for Battery Operation — Typically 113 microwatts
- REF12Z — 3 Lead TO-92 Plastic Package
- REF12 — 2 Lead TO-18 (CM2) Metal Can Package
- Tight Initial V_{REF} Tolerance ±1%
- Low Temperature Coefficient
- Low Cost
- Operation over Full Military (Metal Can) and Industrial (Plastic) Temperature Ranges



Pin connections - bottom view

ORDERING INFORMATION

Device type	Operating temperature	Package
REF12	-55°C to +125°C	CM2
REF12Z	-40°C to +85°C	TO-92



Internal connections REF12/12Z

ABSOLUTE MAXIMUM RATINGS

Reference current	2.5mA
Operating temperature range	−40 to +85°C REF12Z
	−55 to +125°C REF12
Storage temperature range	−55 to +125°C
Soldering temperature for a maximum time of 10s	
within 1.59mm of the seating plane	300°C
within 0.80mm of the seating plane	265°C

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25°C$ unless otherwise specified).

Parameter	Symbol	Min.	Typ.	Max.	Units	Comments
Output voltage	V_{REF}	1.247	1.26	1.273	V	$I_{REF} = 150\mu A$
Slope resistance	R_{REF}	–	2.5	4.0	Ω	$I_{REF} = 100\mu A$ to 2.5mA note (a)
Turn-on (knee) current	I_{ON}	–	80	90	μA	
Recommended operating current range	I_{REF}	0.09	–	2.5	mA	0 to +125°C See derating curve
Temperature coefficient	TC V_{REF}	–	40	56	ppm/°C	−55 to +125°C note (b)
RMS noise voltage 0.1Hz to 25kHz	E_N	–	1.0	–	$\mu V/\sqrt{HZ}$	
Turn-on time	T_{on}	–	0.4	–	ms	$I_{REF} = 1.5mA$
Turn-off time	T_{off}	–	15	–	ms	
Turn-on time	T_{on}	–	5	–	ms	$I_{REF} = 150\mu A$
Turn-off time	T_{off}	–	110	–	ms	
Stabilising capacitor	Cs	470	–	–	nf	

NOTES

(a) Slope resistance (R_{REF})

Slope resistance is defined as

$$R_{REF} = \frac{\text{Change in } V_{REF} \text{ over a specified current range}}{\text{The change in reference current}}$$

(b) reference voltage temperature coefficient

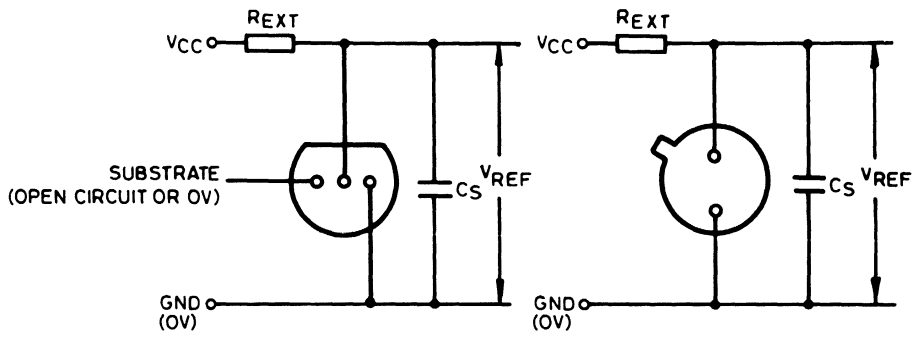
This is the normalised reference voltage change over temperature, divided by the change in temperature. It is expressed in ppm/°C as follows:

$$\text{TC } V_{REF} = \frac{\Delta V_{REF} \times 10^6}{V_{REF} \times \Delta T} \text{ ppm/°C}$$

ΔT = temperature change in °C.

ΔV_{REF} = change in reference voltage over temperature change ΔT.

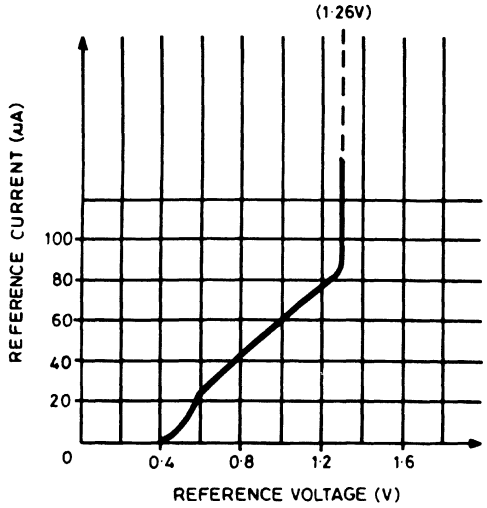
Connection diagram



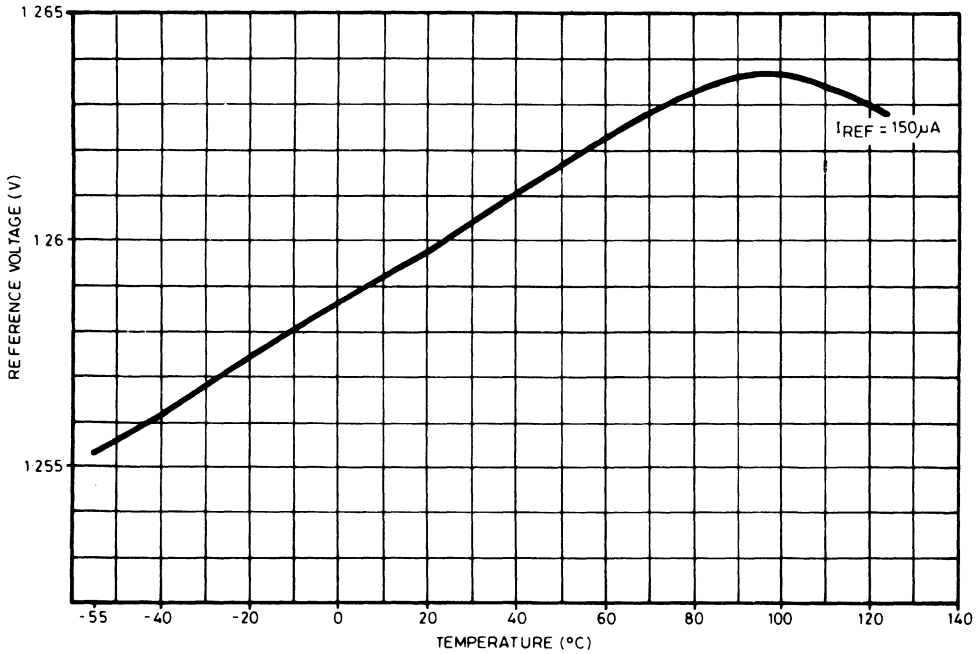
$$R_{EXT} = (V_{CC} - V_{REF})/I_{REF}$$

REF12Z REF12

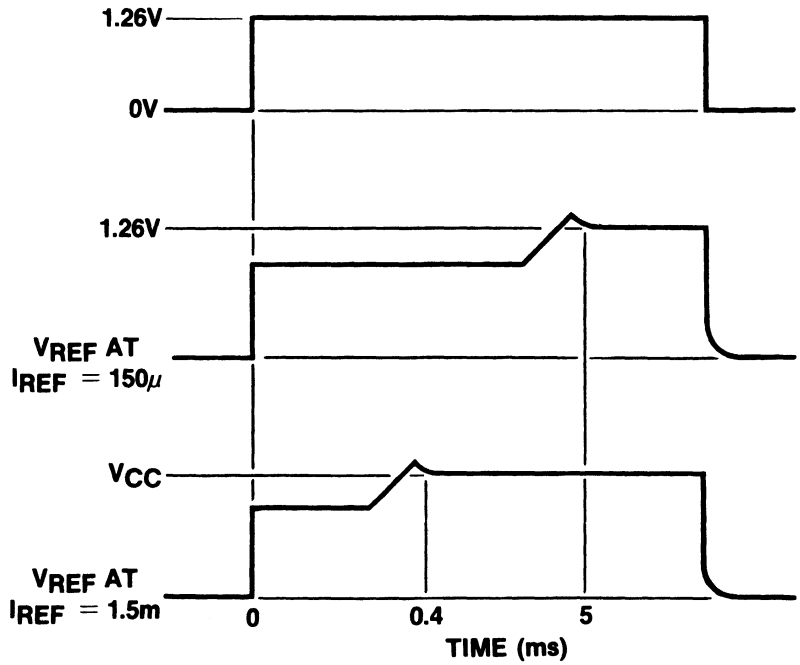
Bottom view



Typical reference characteristic



Typical temperature characteristic



Typical response time

Typical derating curve

PLESSEY
Semiconductors

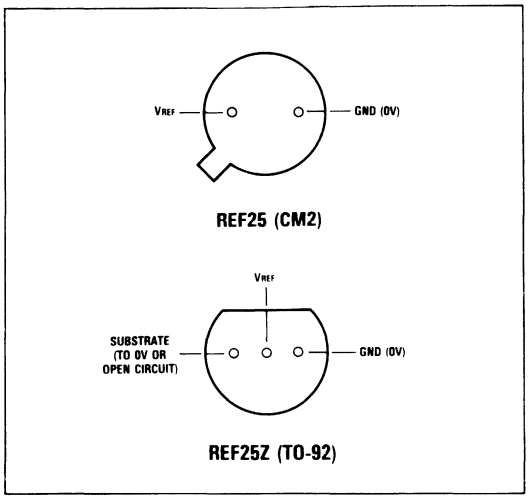
REF25/REF25Z

2.5V MICROPOWER PRECISION REFERENCES

The REF25 and REF25Z are integrated circuits using the bandgap principle to provide a precise stable reference voltage of 2.5V without the need for an external shaping capacitor. There are two package options available: REF25 in 2-pin TO-18 metal can (CM2) and REF25Z in plastic 3-pin TO-92. These references feature a recommended operating current range of 60μA to 5mA which make them ideal for all low power and battery applications.

FEATURES

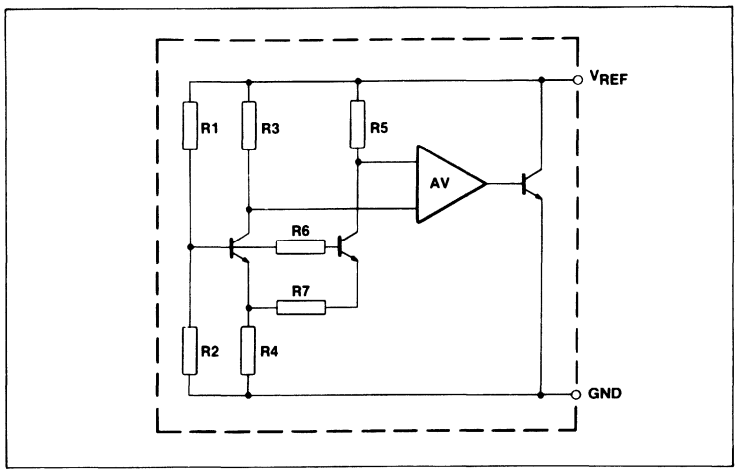
- Low Knee Current — Typically 40 microamps
- Ideal for Battery Operation — 150 microwatts
- Internally Shaped
- REF25Z — 3 Lead TO-92 Plastic Package
- REF25 — 2 Lead TO-18 (CM2) Metal Can Package
- Tight Initial V_{OUT} Tolerance ±1%
- Low Temperature Coefficient
- Low Slope Resistance
- Low Cost
- Operation over Full Military (Metal Can) and Industrial (Plastic) Temperature Ranges



Pin connections - bottom view

ORDERING INFORMATION

Device type	Operating temperature	Package
REF25	-55°C to +125°C	CM2
REF25Z	-40°C to +85°C	TO-92



Internal connections REF25/25Z

ABSOLUTE MAXIMUM RATINGS

Reference current	5mA
Operating temperature range	0 to +70°C
Storage temperature range	−55 to +125°C
Soldering temperature for a maximum time of 10s	
within 1.59mm of the seating plane	300°C
within 0.80mm of the seating plane	265°C

ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C unless otherwise specified).

Parameter	Symbol	Min.	Typ.	Max.	Units	Comments
Output voltage	V_{REF}	2.475	2.500	2.525	V	REF25 } I_{REF} = 150μA
		2.450	2.500	2.550		REF25Z }
Slope resistance	R_{REF}	–	1.2	1.5	Ω	REF25 } I_{REF} = 150μA to 5mA note (a)
		–	1.2	2.0		REF25Z }
Turn-on (knee) current	I_{ON}	–	40	–	μA	
Recommended operating current range	I_{REF}	0.06	–	5.0	mA	
Temperature coefficient	TC V_{ref}	–	25	55	ppm/°C	REF25 } I_{REF} = 150μA note (b)
		–	35	70		REF25Z }
RMS noise voltage 1Hz to 10kHz	E_N	–	35	–	μV	Peak to peak
Turn-on time	T_{on}	–	80	–	μs	I_{ref} = 150μA
Turn-off time	T_{off}	–	7	–		
Turn-on time	T_{on}	–	65	–	μs	I_{ref} = 500μA
Turn-off time	T_{off}	–	2	–		

NOTES

(a) Slope resistance (R_{REF})

Slope resistance is defined as

$$R_{REF} = \frac{\text{Change in } V_{ref} \text{ over a specified current range}}{\text{The change in reference current}}$$

(b) Reference voltage temperature coefficient (TC V_{ref})

This is the normalised reference voltage change over temperature, divided by the change in temperature. It is expressed in ppm/°C as follows:

$$TC\ V_{ref} = \frac{\Delta V_{ref} \times 10^6}{V_{ref} \times \Delta T} \quad ppm/°C$$

ΔT = temperature change in °C.

ΔV_{ref} = change in reference voltage over temperature change ΔT.

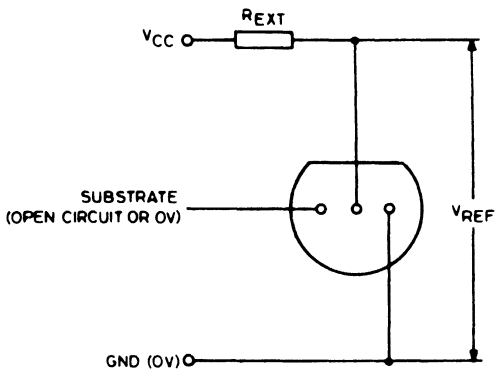
(c) Line regulation (ΔV_{ref} L)

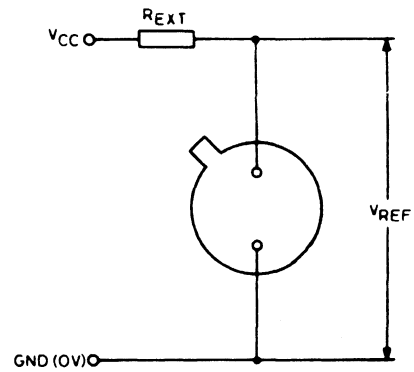
The ratio of the change in reference voltage to the change in input voltage.

$$\Delta V_{ref}\ L = \left(\frac{R_{ref} \times 100}{V_{ref} \times R_s}\right) \quad \%/V$$

R_S = Source resistance.

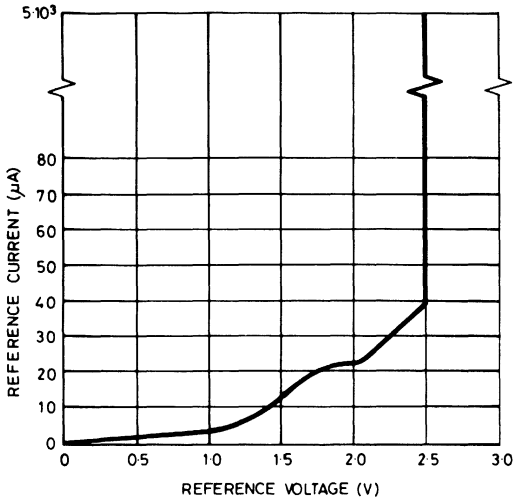
External connections



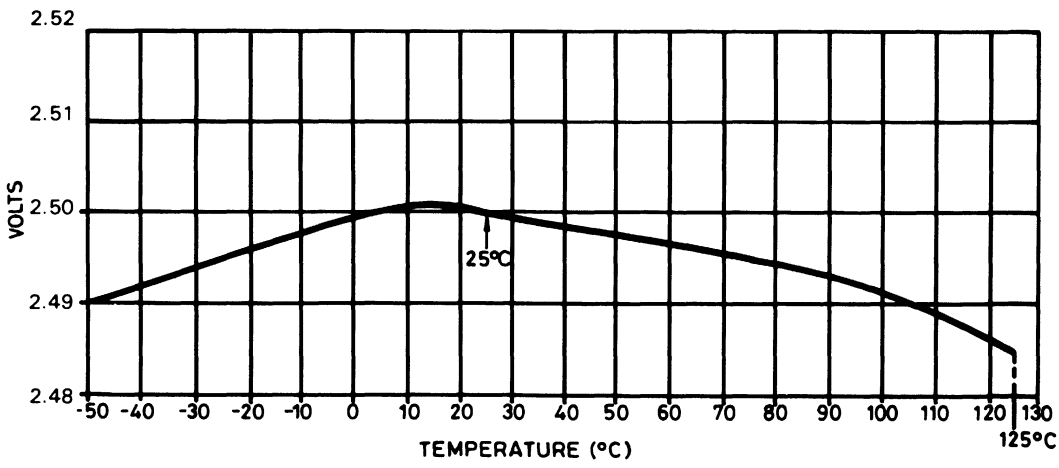


$R_{EXT} = (V_{CC} - V_{REF})/I_{REF}$

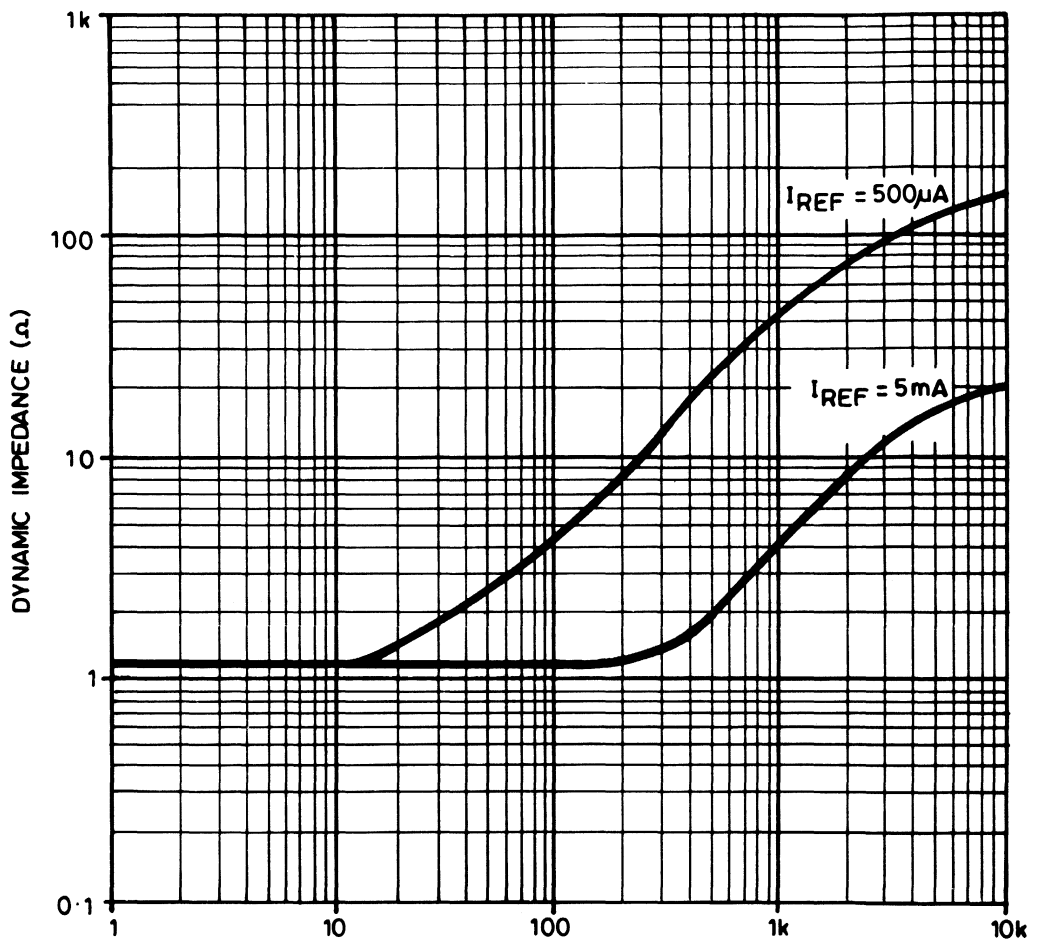
REF25Z **REF25**



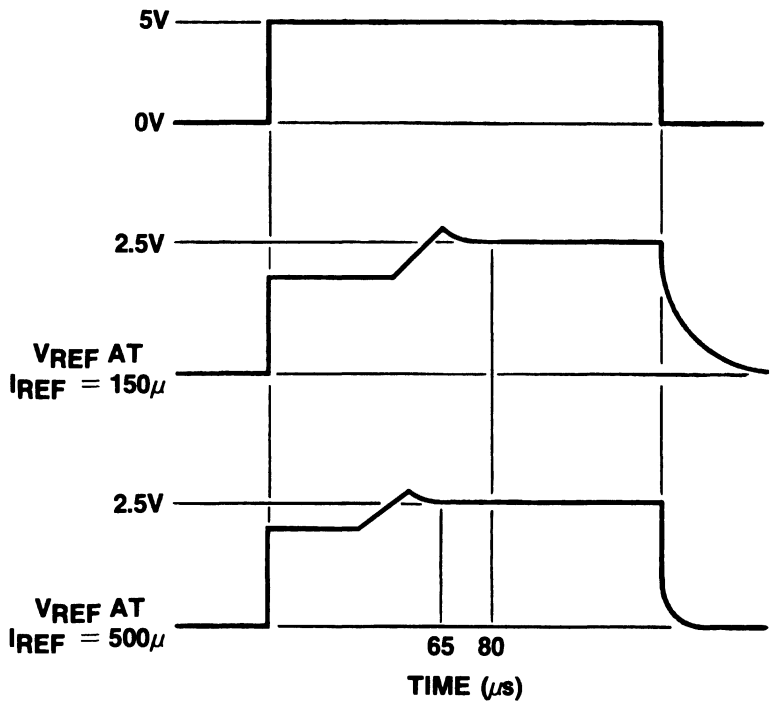
Typical reference characteristic



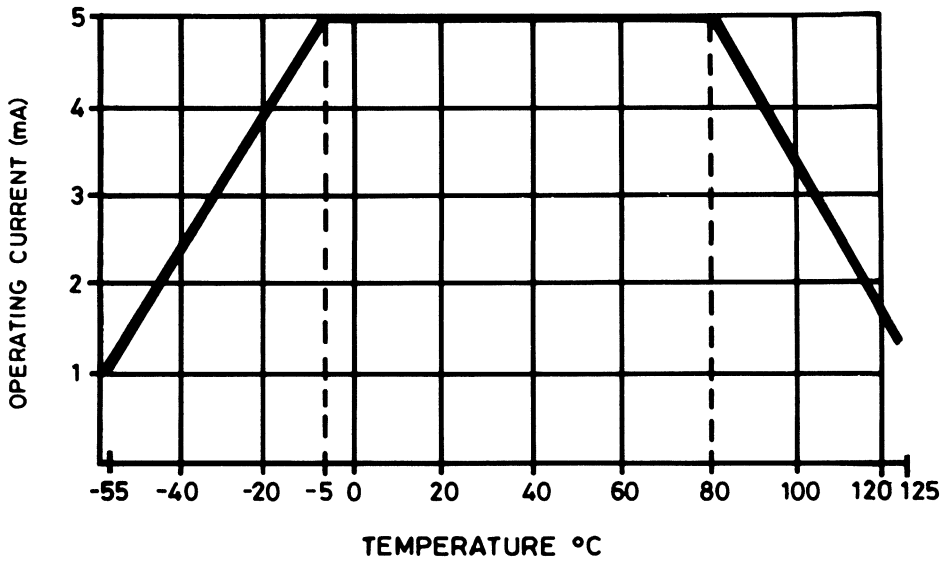
Typical temperature characteristic



Typical dynamic impedance



Typical response time



Typical derating curve

REF25D

2.5V MICROPOWER PRECISION REFERENCE

The REF25D is an integrated circuit using the bandgap principle to provide a precise stable reference voltage of 2.5V without the need for an external shaping capacitor. The REF25D features a recommended operating current range of 60μA to 5mA which makes it ideal for all low power and battery applications.

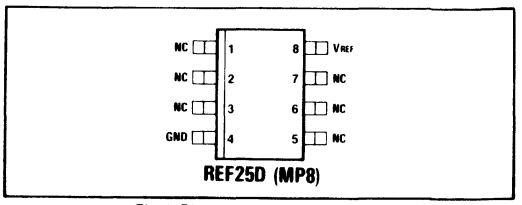


Fig.1 Pin connections - top view

FEATURES

- Low Knee Current — Typically 40 microamps
- Ideal for Battery Operation — 150 microwatts
- Internally Shaped
- Miniature Plastic Surface Mount Package (MP8)
- Tight Initial V_{OUT} Tolerance ±1%
- Low Temperature Coefficient
- Low Slope Resistance
- Low Cost
- Industrial Temperature Range: -40°C to +85°C

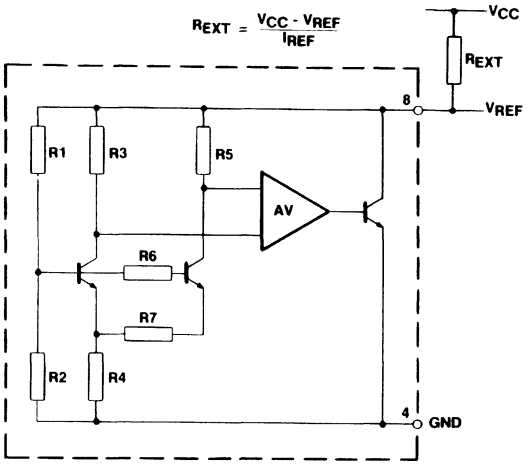


Fig.2 REF25D circuit diagram

ABSOLUTE MAXIMUM RATINGS

Reference current	5mA
Operating temperature range	-40°C to +85°C
Storage temperature	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25°C

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output voltage	V_{REF}	2.475	2.500	2.525	V	I_{REF} = 150μA
Slope resistance	R_{REF}		1.2	2.0	Ω	I_{REF} = 150μA to 5mA. Note (a)
Turn-on (knee) current	I_{ON}		40	60	μA	
Recommended operating current range	I_{REF}	0.06		5.0	mA	-5°C to 80°C (see Fig.7)
Temperature coefficient	TC V_{REF}		35	70	ppm/°C	I_{REF} = 150μA. Note (b)
RMS noise voltage 1Hz to 10kHz	E_N		35		μV	Peak to peak
Turn-on time	T_{on}		80		μs	I_{REF} 150μA (see Fig.6)
Turn-off time	T_{off}		7		μs	
Turn-on time	t_{on}		65		μs	I_{REF} = 500μA (see Fig.6)
Turn-off time	T_{off}		2		μs	

NOTES

(a) Slope resistance (R_{REF})

Slope resistance is defined as

$$R_{REF} = \frac{\text{Change in } V_{REF} \text{ over a specified current range}}{\text{The change in reference current}}$$

(b) Reference voltage temperature coefficient (TC V_{REF})

This is the normalised reference voltage change over temperature, divided by the change in temperature. It is expressed in ppm/°C as follows:

$$TC\ V_{REF} = \frac{\Delta V_{REF} \times 10^6}{V_{REF} \times \Delta T} \quad ppm/°C$$

ΔT = temperature change in °C.

ΔV_{REF} = change in reference voltage over temperature change ΔT.

(c) Line regulation (ΔV_{REF} L)

The ratio of the change in reference voltage to the change in input voltage.

$$\Delta V_{REF}\ L = \left| \frac{R_{REF} \times 100}{V_{REF} \times R_s} \right| \quad \%/V$$

R_S = Source resistance.

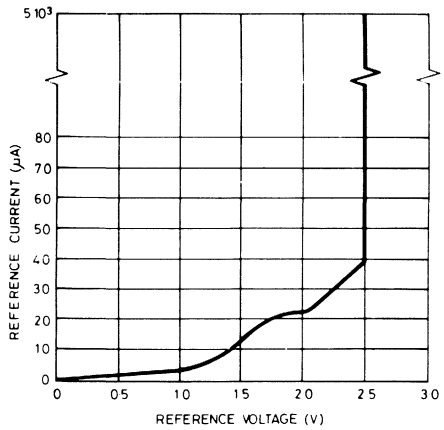


Fig.3 Typical reference characteristic

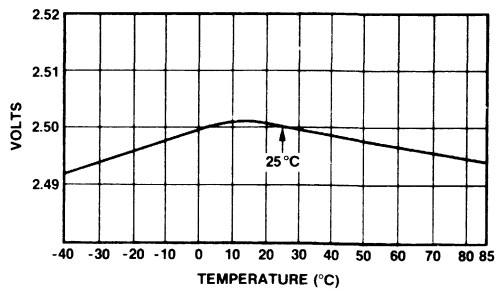


Fig.4 Typical temperature characteristic

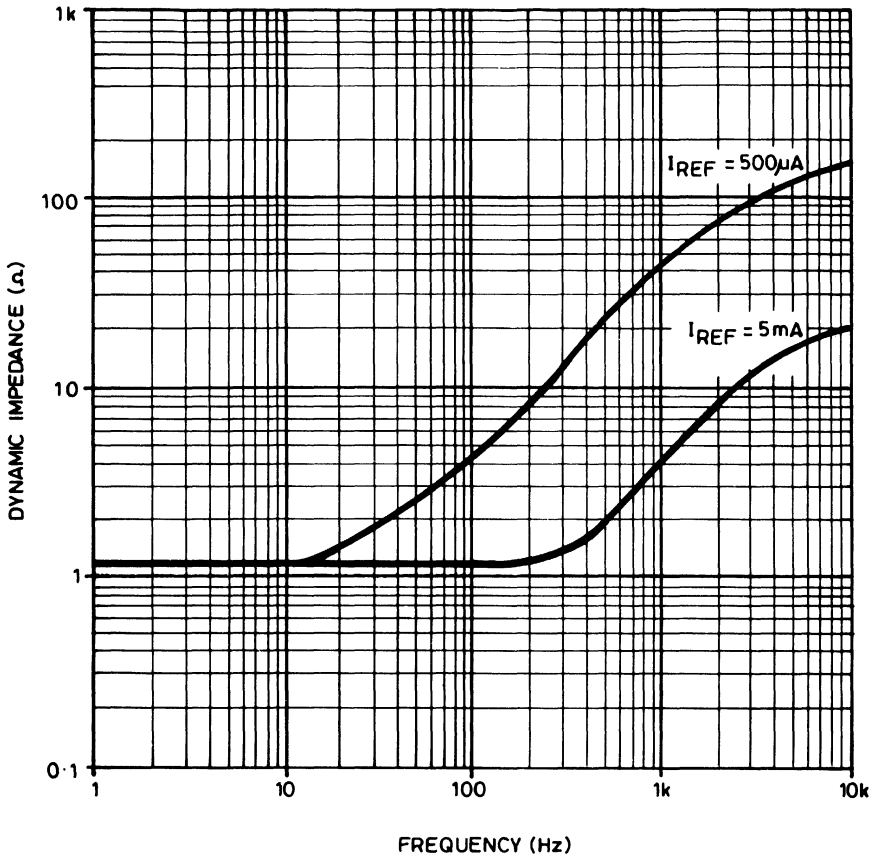


Fig.5 Typical dynamic impedance

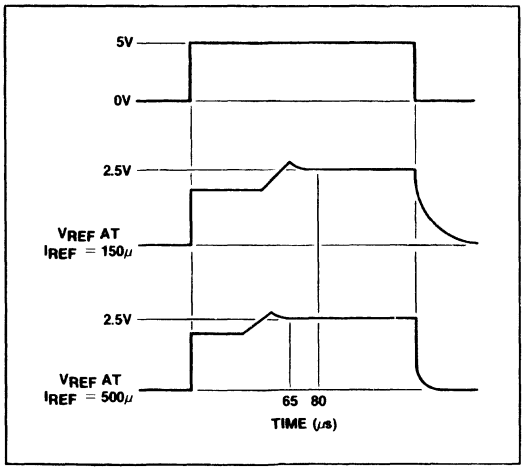


Fig.6 Typical response time

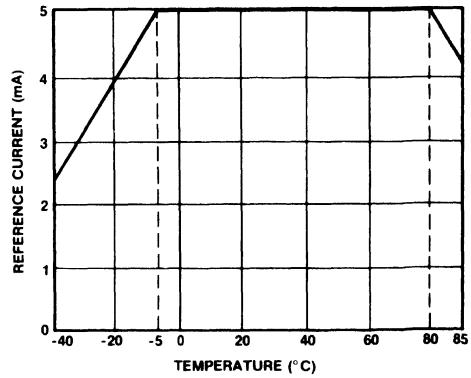


Fig.7 Typical derating curve

PLESSEY
Semiconductors

REF50/REF50Z

5V MICROPOWER PRECISION REFERENCES

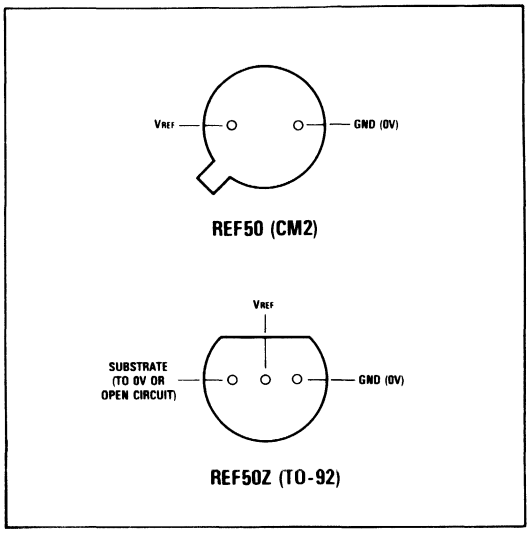
The REF50 and REF50Z are micropower integrated circuits using the bandgap principle to provide a precise reference voltage of 5V. There are two package options available: REF50 in 2-pin TO-18 metal can (CM2) and REF50Z in plastic 3-pin TO-92. These references feature a recommended operating current range of 60μA to 5mA which make them ideal for all low power and battery applications.

FEATURES

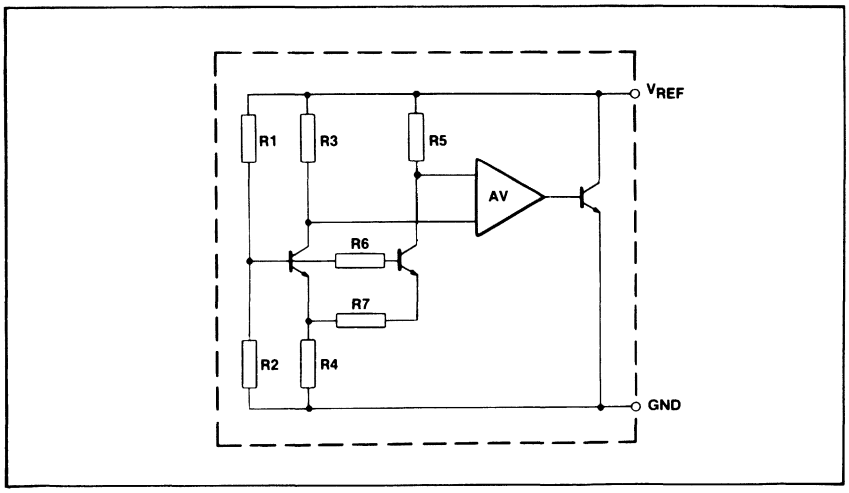
- Low Knee Current — Typically 50 microamps
- Ideal for Battery Operation
- REF50Z — 3 Lead TO-92 Plastic Package
- REF50 — 2 Lead TO-18 (CM2) Metal Can Package
- Tight Initial V_{REF} Tolerance ±1%
- Low Temperature Coefficient
- Low Cost
- Operation over Full Military (Metal Can) and Industrial (Plastic) Temperature Ranges

ORDERING INFORMATION

Device type	Operating temperature	Package
REF50	-55°C to +125°C	CM2
REF50Z	-40°C to +85°C	TO-92



Pin connections - bottom view



Internal connections REF50/50Z

ABSOLUTE MAXIMUM RATINGS

Reference current 5mA
Operating temperature range
REF50 . . . . . −55 to +125°C
REF50Z . . . . . −40 to +85°C
Storage temperature . . . . . −55 to +125°C
Soldering temperature for a maximum time of 10s
within 1.59mm of the seating plane . . . . . 300°C
within 0.80mm of the seating plane . . . . . 265°C

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25°C$ unless otherwise stated).

Parameter	Symbol	Min.	Typ.	Max.	Units	Comments
Output voltage	V_{REF}	4.95	5.00	5.05	V	$I_{REF} = 150\mu A$
Slope resistance	R_{REF}	–	3.0	3.5	Ω	$I_{REF} = 150\mu A$ to 5mA note (a)
Turn-on (knee) current	I_{ON}	–	50	60	μA	
Recommended operating current range	I_{REF}	0.06	–	5.0	mA	−5 to +80°C
Temperature coefficient	TC V_{REF}	–	30	60	ppm/°C	REF50 } $I_{REF} = 150\mu A$
		–	40	70		REF50Z }
RMS noise voltage 1Hz to 10kHz	E_N	–	35	–	μV	Peak to peak
Turn-on time	T_{on}	–	200	–	μs	$I_{REF} = 150\mu A$
Turn-off time	T_{off}	–	10	–		
Turn-on time	T_{on}	–	100	–	μs	$I_{REF} = 500\mu A$
Turn-off time	T_{off}	–	2	–		

Note It should be noted that in some instances to achieve optimum operation a 10nF capacitor should be connected between V_{REF} and G_{ND}.

NOTES

(a) Slope resistance (R_{REF})

Slope resistance is defined as

$$R_{REF} = \frac{\text{Change in } V_{REF} \text{ over a specified current range}}{\text{The change in reference current}}$$

(b) Reference voltage temperature coefficient (TC V_{REF})

This is the normalised reference voltage change over temperature, divided by the change in temperature. It is expressed in ppm/°C as follows:

$$\text{TC } V_{REF} = \frac{\Delta V_{REF} \times 10^6}{V_{REF} \times \Delta T} \quad \text{ppm/°C}$$

ΔT = temperature change in °C.

ΔV_{REF} = change in reference voltage over temperature change ΔT.

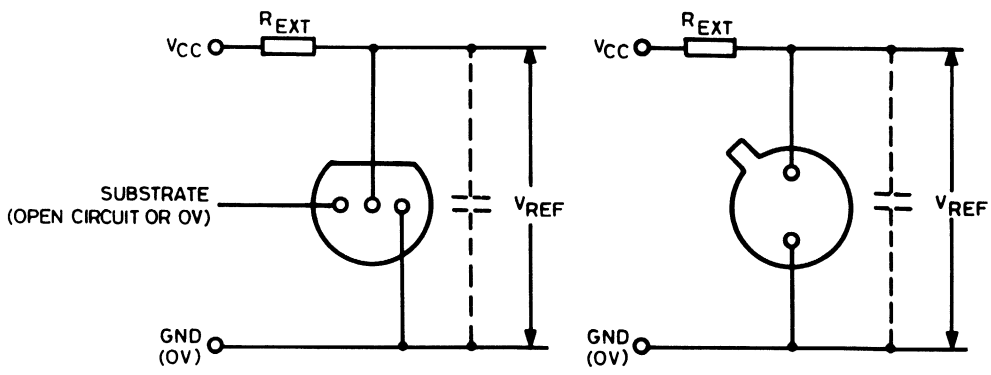
(c) Line regulation (ΔV_{REF} L)

The ratio of the change in reference voltage to the change in input voltage.

$$\Delta V_{REF}\ L = \left(\frac{R_{REF} \times 100}{V_{REF} \times R_s}\right) \quad \%/V$$

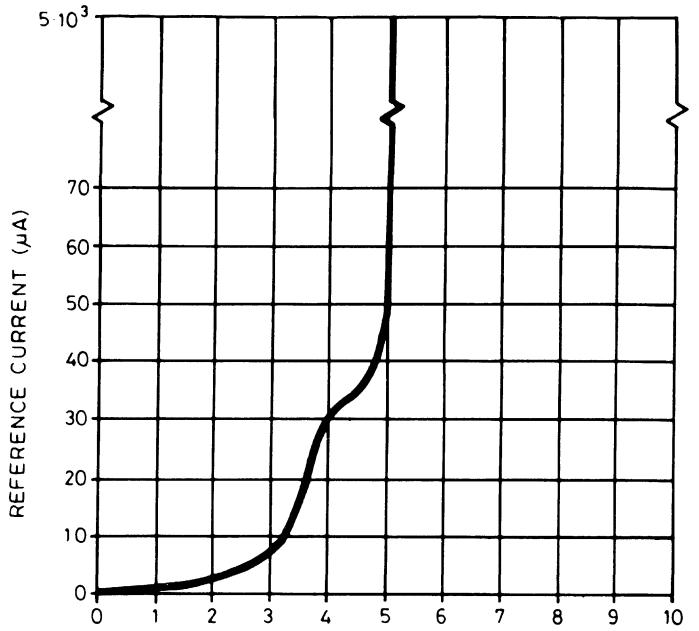
R_S = Source resistance.

Connection diagram

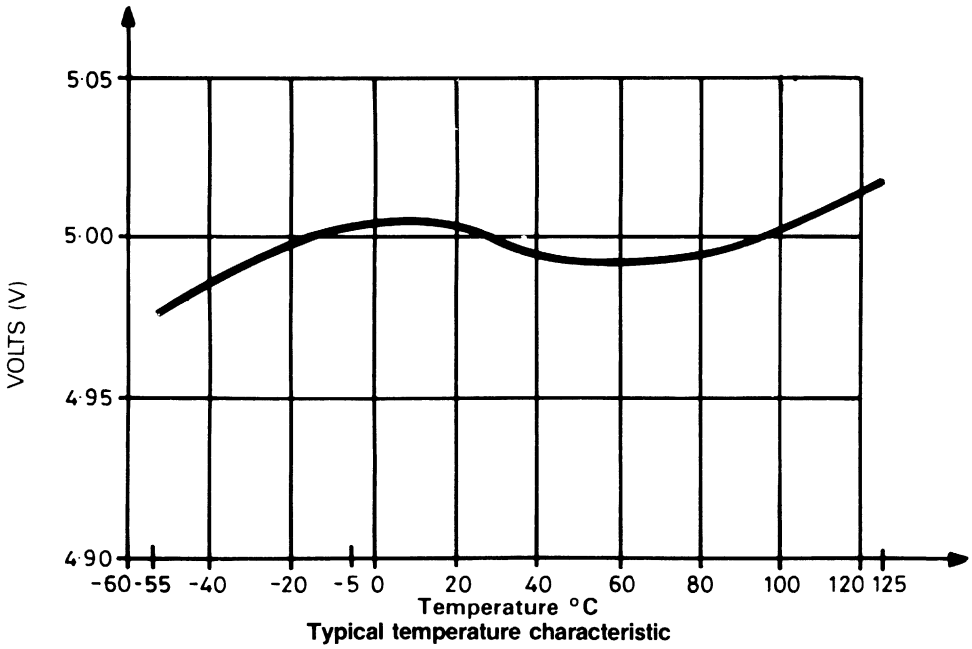


$$R_{EXT} = (V_{CC} - V_{REF})/I_{REF}$$

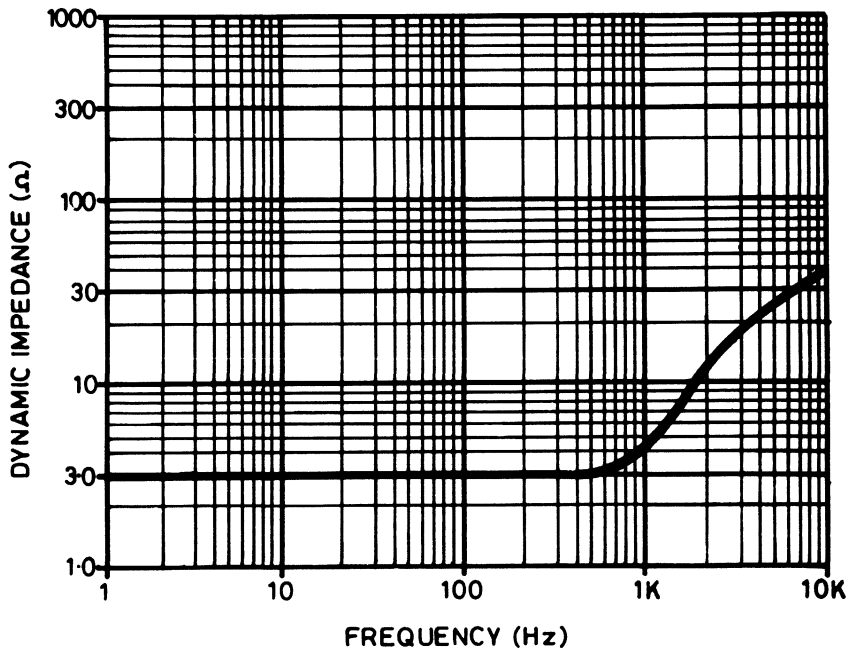
REF50Z **REF50**



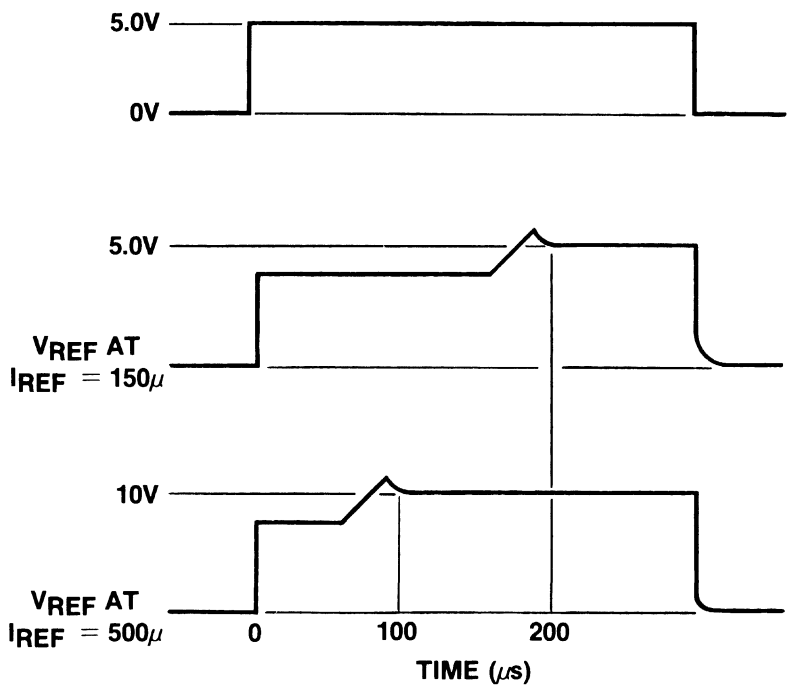
Typical reference characteristic



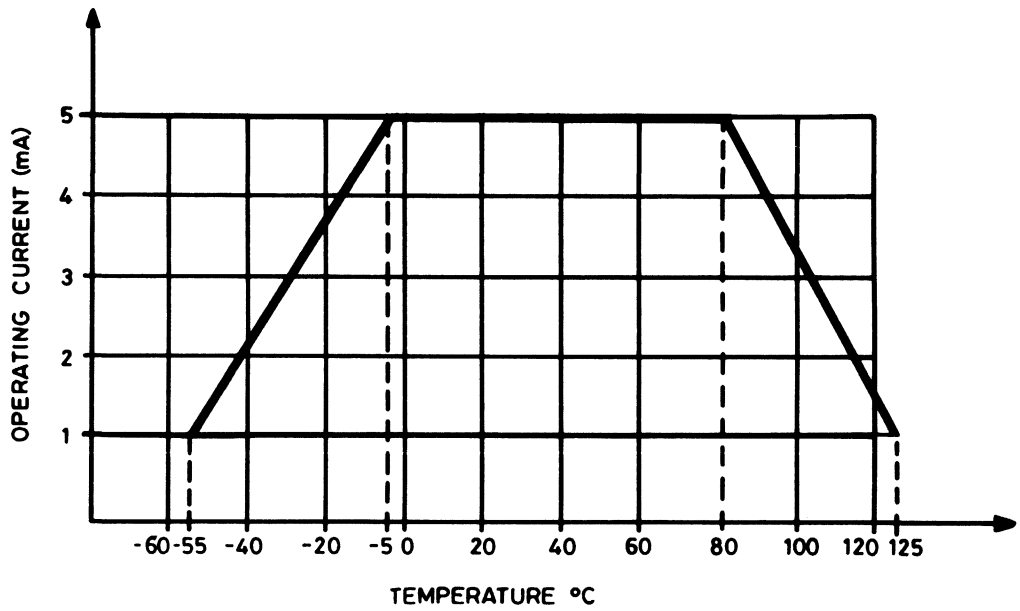
Typical temperature characteristic



Typical dynamic impedance



Typical response time



Typical derating curve

SR12D

1.2V PRECISION VOLTAGE REFERENCE

The SR12D is a monolithic integrated circuit utilising the bandgap principle to provide a precise reference voltage of 1.23V.

This reference device is packaged in a standard SOT-23 small outline package, making it ideal for all surface mount applications.

FEATURES

- Packaged in a Standard SOT-23 Surface Mount Package
- Low Knee Current — Typcially 80 microamps
- Low Temperature Coefficient

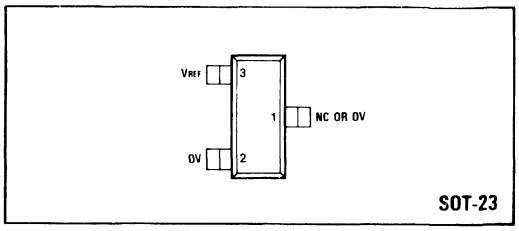


Fig.1. Pin connections (top view)

ABSOLUTE MAXIMUM RATINGS

Reference current	2.5mA
Operating temperature range	0°C to +70°C
Storage temperature range	-55°C to +125°C

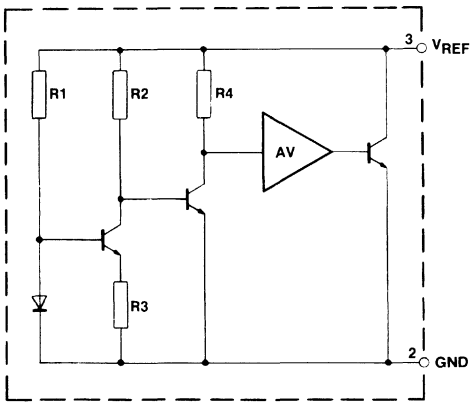


Fig.2 SR12D circuit diagram

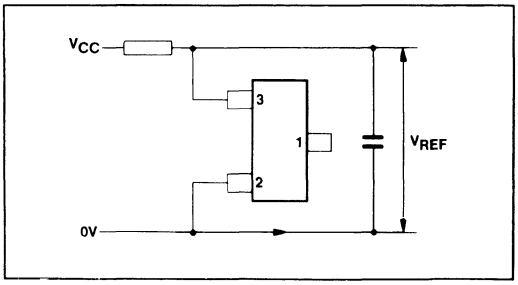


Fig.3 SR12D external connections

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25°C

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output voltage	V_{REF}	1.218	1.230	1.242	V	I_{REF} = 150μA
Slope resistance	R_{REF}	-	2.5	4.0	Ω	I_{REF} = 100μA to 2.5mA
Knee current	I_{ON}	-	80	90	μA	
Recommended operating current range	I_{REF}	0.09	-	2.5	mA	
Temperature coefficient	TC V_{REF}	-	40		ppm/°C	

SR25D

2.5V PRECISION VOLTAGE REFERENCE

The SR25D is a monolithic integrated circuit utilising the bandgap principle to provide a precise reference voltage of 2.5V.

This reference device is packaged in a standard SOT-23 small outline package, making it ideal for all surface mount applications.

FEATURES

- Packaged in a Standard SOT-23 Surface Mount Package
- Low Knee Current — Typically 80 microamps
- Low Temperature Coefficient

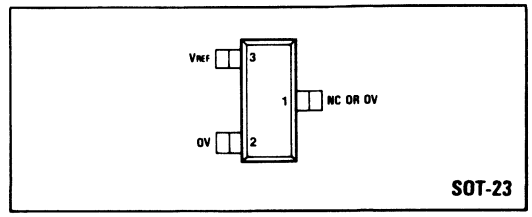


Fig.1. Pin connections (top view)

ABSOLUTE MAXIMUM RATINGS

Reference current	5mA
Operating temperature range	0°C to +70°C
Storage temperature range	-55°C to +125°C

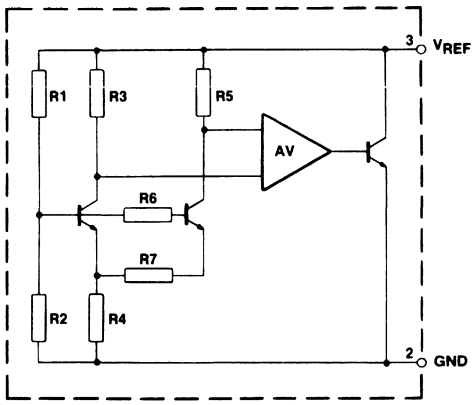


Fig.2 SR25D circuit diagram

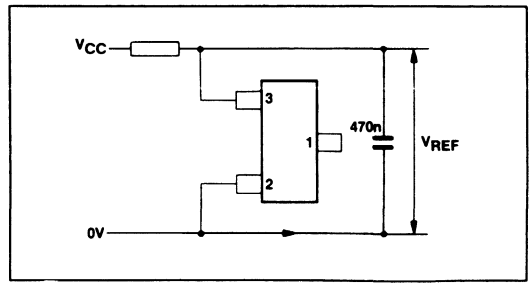


Fig.3 SR25D external connections

It should be noted that to achieve optimum operation a 470nF capacitor should be connected between V_{REF} and GND.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

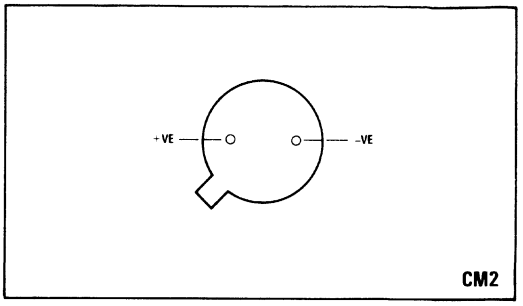
T_{amb} = 25°C

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output voltage	V_{REF}	2.425	2.5	2.575	V	I_{REF} = 150μA
Slope resistance	R_{REF}	-	1.2	2.0		I_{REF} = 150μA to 5mA
Knee current	I_{ON}	-	60	80	μA	
Recommended operating current range	I_{REF}	0.08	-	5	mA	
Temperature coefficient	TC V_{REF}	-	35	90	ppm/°C	

ZN404

2.45V PRECISION REFERENCE REGULATOR

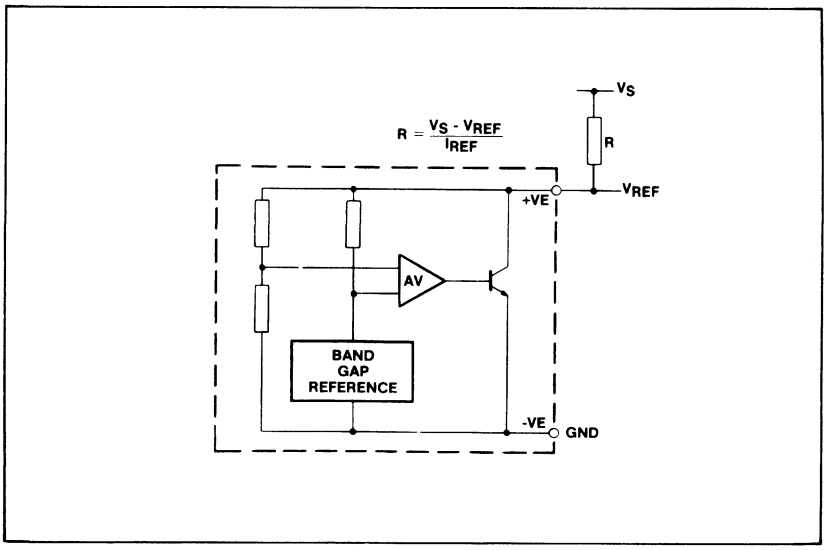
The ZN404 is a monolithic integrated circuit providing a precise stable regulator source of 2.45V in a two lead package without the need for an external shaping capacitor.



Pin connections - bottom view

FEATURES

- Low Temperature Coefficient
- Low Slope Resistance
- Very Good Long Term Stability
- Low Noise
- Internally Shaped
- Tight Tolerance
- Two Pin Package



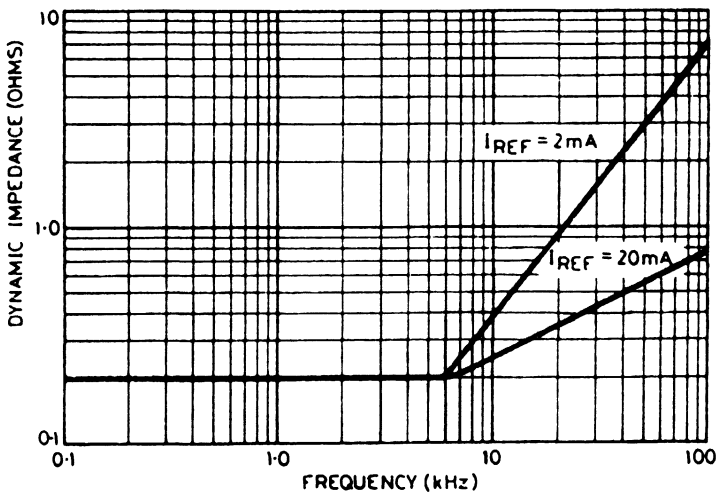
Circuit diagram

ABSOLUTE MAXIMUM RATINGS

Dissipation	300mW
Operating temperature range	0 to +70°C
Storage temperature range	−55 to +125°C

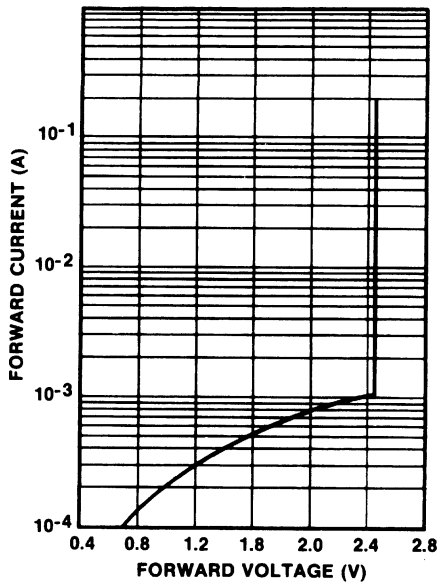
ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C unless otherwise specified).

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Output voltage	V_{REF}	2.38	2.45	2.52	V	Measured at 2mA
Slope resistance	R_{REF}	–	0.2	0.4	Ω	
Reference current	I_{REF}	2	–	120	mA	
Maximum change in V_{REF}	ΔV_{REF}	–	6	25	mV	0 to +70°C
RMS noise voltage 1Hz-10kHz		–	10	–	μV	
V_{REF} drift at 70°C		–	±10	–	ppm/1000 hours	

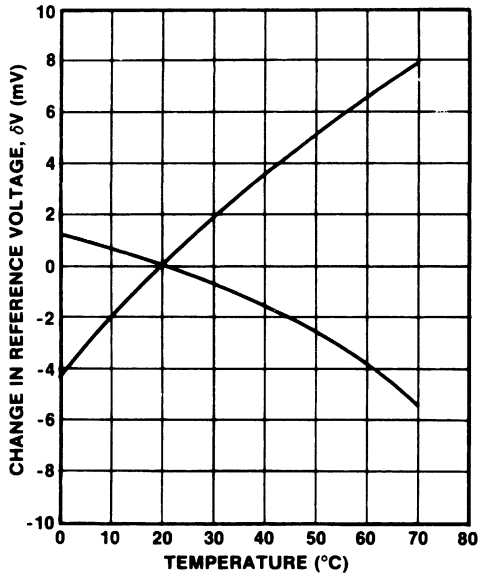


Dynamic impedance

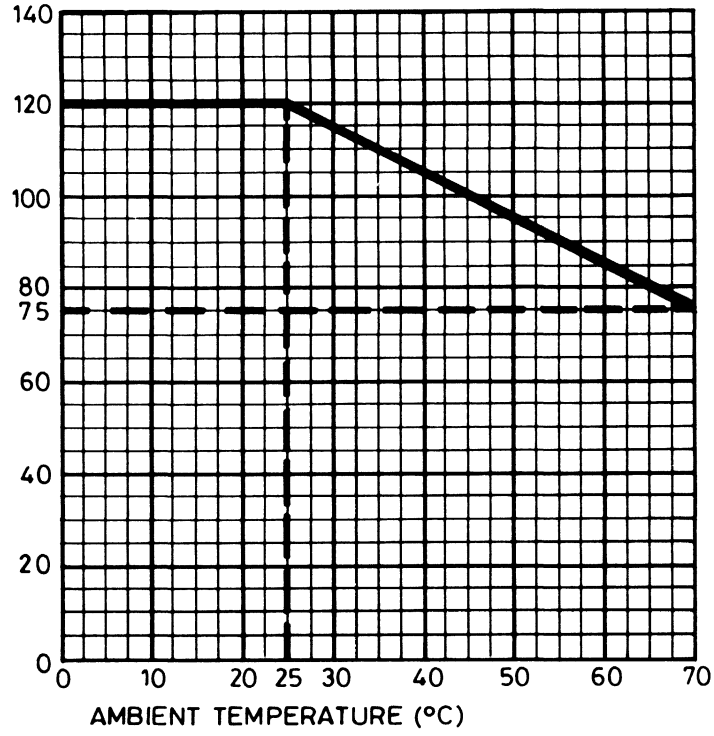
Forward characteristic (typical)



Temperature characteristic (typical)



Derating curve

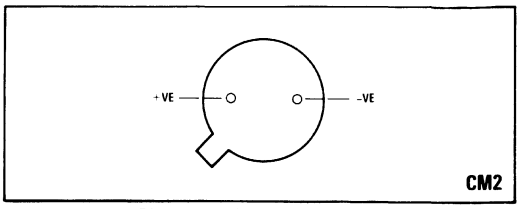


PLESSEY
Semiconductors

ZN423

PRECISION VOLTAGE REFERENCE SOURCE

The ZN423 is a monolithic integrated circuit utilising the energy bandgap voltage of a base-emitter junction to produce a precise, stable, regulator source of 1.26V. This is derived via an external dropping resistor for supply voltages of 1.5V upwards. The temperature coefficient of the ZN423, unlike conventional Zener diodes, remains constant with reference current. The noise figure associated with breakdown mechanisms is also considerably reduced.



Pin connections - bottom view

FEATURES

- Low Voltage
- Low Temperature Coefficient
- Very Good Long Term Stability
- Low Slope Resistance
- Low RMS Noise
- Tight Tolerance
- High Power Supply Rejection Ratio
- Two Pin Package

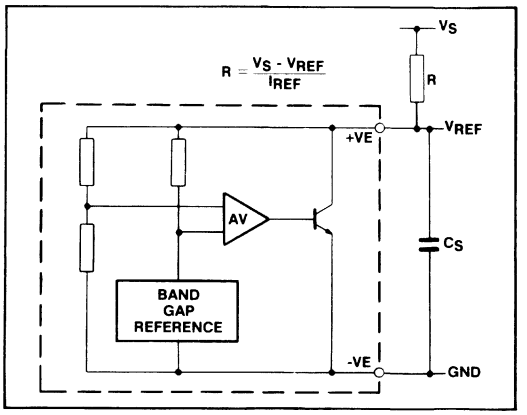


Fig.1 Circuit diagram

ABSOLUTE MAXIMUM RATINGS

Reference current I_{REF}	20mA
Operating temperature range	-55°C to +125°C
Storage temperature range	-65°C to +165°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25°C

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Output voltage	V_{REF}	1.2	1.26	1.32	V	
Slope resistance	R_{REF}		0.5	1.0	Ω	Note 1
Reference current	I_{REF}	1.5		12	mA	
Temperature coefficient			30		ppm/°C	
Shaping capacitance	C_S	0.1			μF	
External resistance	R_{EXT}	100			Ω	Note 2
RMS noise voltage 1Hz to 10kHz			6		μV	
Power supply rejection ratio V_{REF} = 1.26V I_{REF} = 2.5mA V_{CC} = 5.0V	PSRR		60		dB	Note 3
V_{REF} drift at 125°C	σV_{REF}		10 100		ppm/1000 hours ppm/year	

NOTES
1. I_{REF} = 5mA 2. $R_{EXT} = (V_{CC1} - V_{REF})/I_{REF}$ 3. $PSRR = R_{EXT}/R_{REF}$

Reference current I_{REF} (max.) v operating temperature.

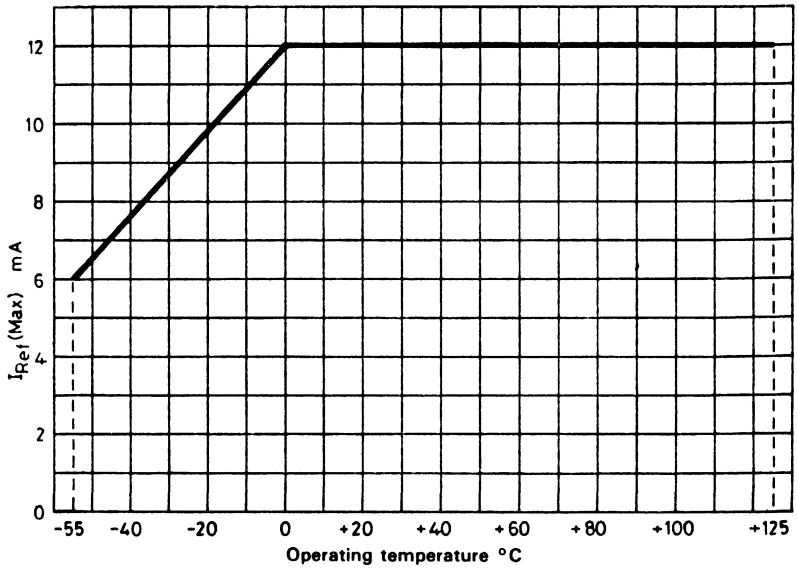


Fig.2 Derating curve

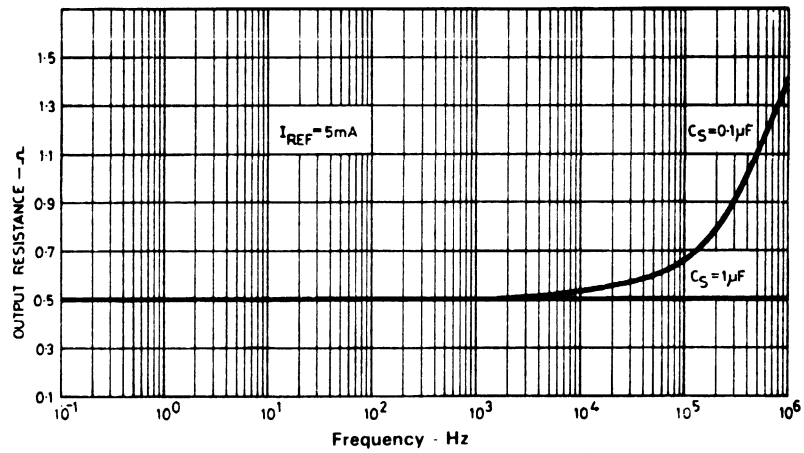


Fig.3 Slope resistance v frequency (I_{REF} = 5mA)

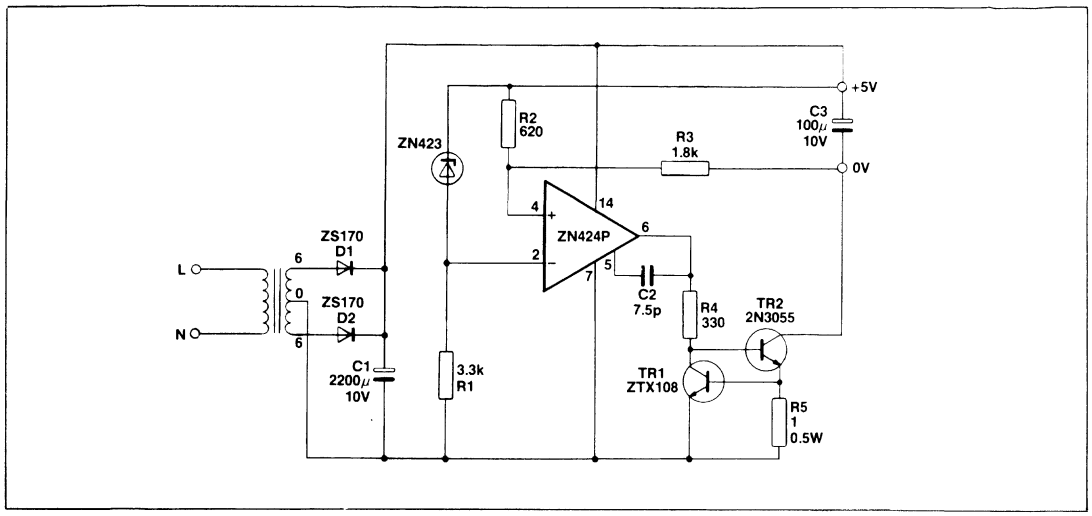


Fig.4 5V, 0.5A power supply

APPLICATIONS

5V, 0.5A Power Supply

The circuit shown in Fig.4 is essentially a constant current source modified by the feedback components R2 and R3 to give a constant voltage output.

The output of the ZN424P need only be 2V above the negative rail, by placing the load in the collector of the output transistor TR2. Current control is achieved by TR1 and R5. This simple circuit has the following performance characteristics:

Output noise and ripple (full load) = 1mV rms
Load regulation (0 to 0.5A) = 0.1%
Temperature coefficient = ±100ppm/°C
Current limit = 0.65A.

5V, 1.0A Power Supply

The circuit detailed in Fig.5 provides improved performance over that in Fig.4. This is achieved by feeding the ZN423 reference and the ZN424P error amplifier from a more stable source, derived from the emitter-follower stage (TR1). The supply rejection ratio is improved by the factor R1/R5, where R5 is the slope resistance of the ZN423.

The output voltage is given by:

$$\frac{(R3 + R4)}{R3} \quad V_{REF}$$

and may be adjusted by replacing R3 with a 220 and a 500Ω preset potentiometer.

The output is protected against short circuits by TR2 setting a current limit of 1.6A.

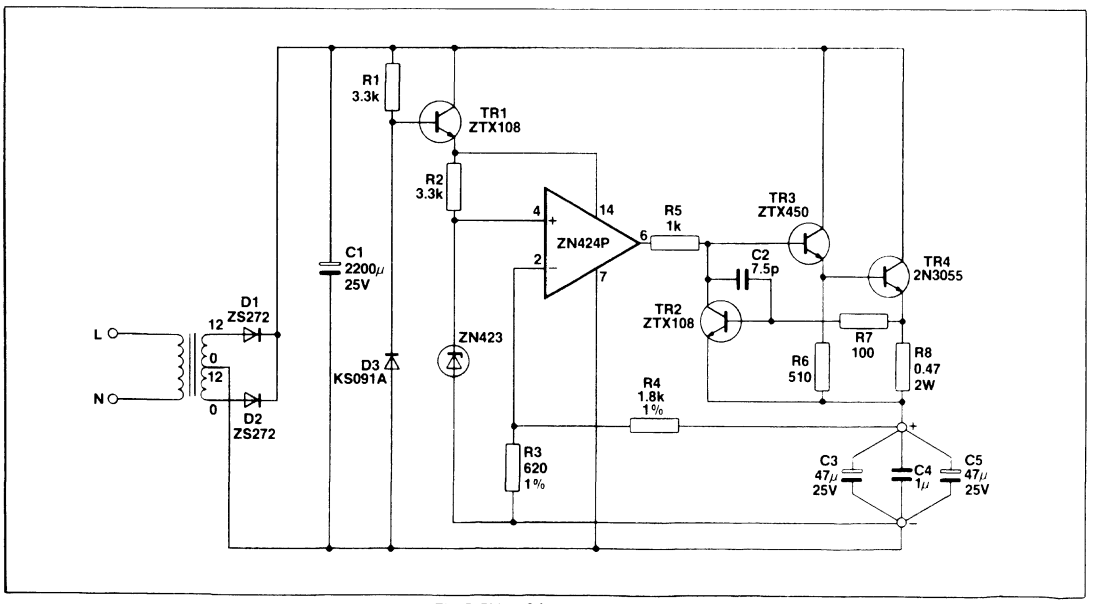


Fig.5 5V, 1.0A power supply

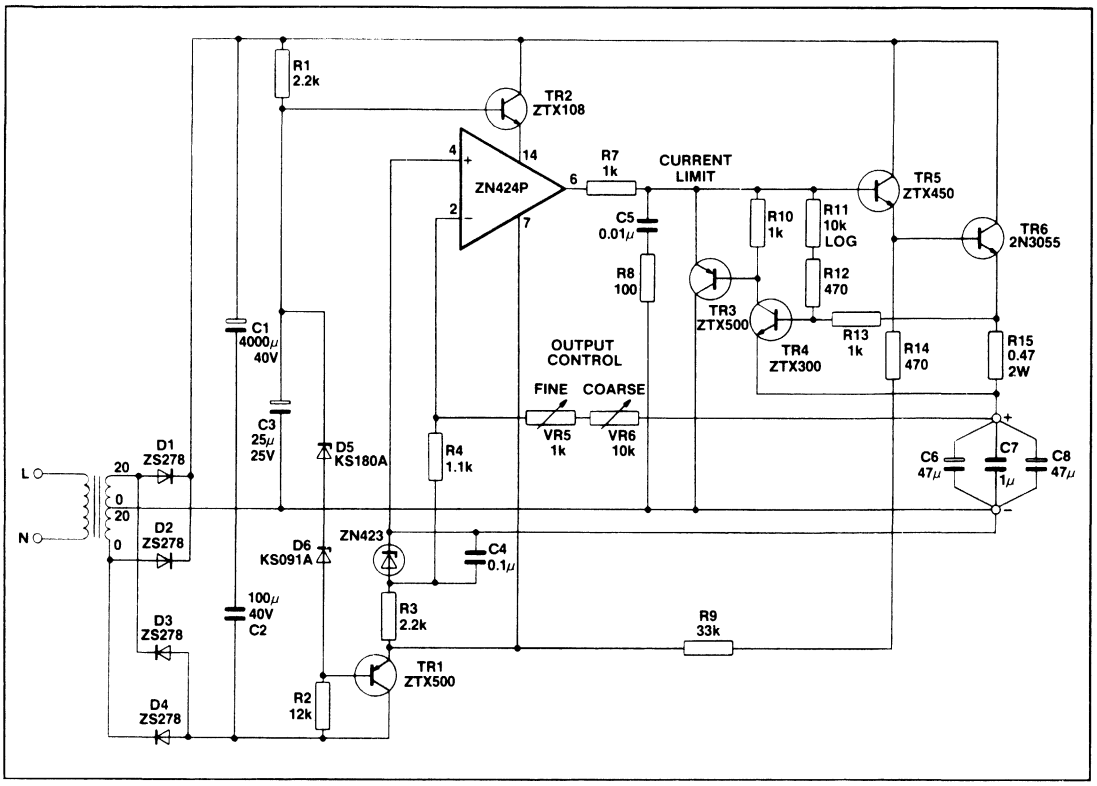


Fig.6 0V to 12V, 1A power supply

0V to 12V, 1A Power Supply

The circuit of Fig.6 provides a continuously variable, highly stable voltage for load currents up to 1A. The output voltage is given by:

$$V_O = \frac{(VR5 + VR6)}{R4} V_{REF}$$

and is controlled by VR5 and VR6 which should be high quality components (preferably wire wound).

The emitter follower stages TR1 and TR2 buffer the bias and reference from the output stage. The negative rail allows the output to operate down to 0V.

The current limit stage monitors output current through R15. As the potential across R15 increases due to load current, TR4 conducts and supplies base current for TR3, thus diverting part of the output from the ZN424P via TR3 to TR5.

Shaping is achieved by the network C5, R8 together with the output decoupling capacitors which also maintain low output resistance at frequencies above 100kHz.

The power supply has the following performance characteristics:

Output noise and ripple (full load) $<100\mu$V rms
Output resistance (0 to 1A) 1MΩ
Temperature coefficient ± 100ppm/°C

Variable 100mA to 2A Current Source

In the circuit of Fig.7 the output current is set by the resistor R in the collector of TR2, which may be switched to offer a range of output currents from 100mA to 2A with fine control by means of VR3 which varies the reference voltage to the non-inverting input of the ZN424P.

The feedback path from the output to the inverting input of the ZN424P maintains a constant voltage across R, equal to ($V_{CC} - V_{IN}$) and hence a constant current to the load given by ($V_{CC} - V_{IN}$)/R.

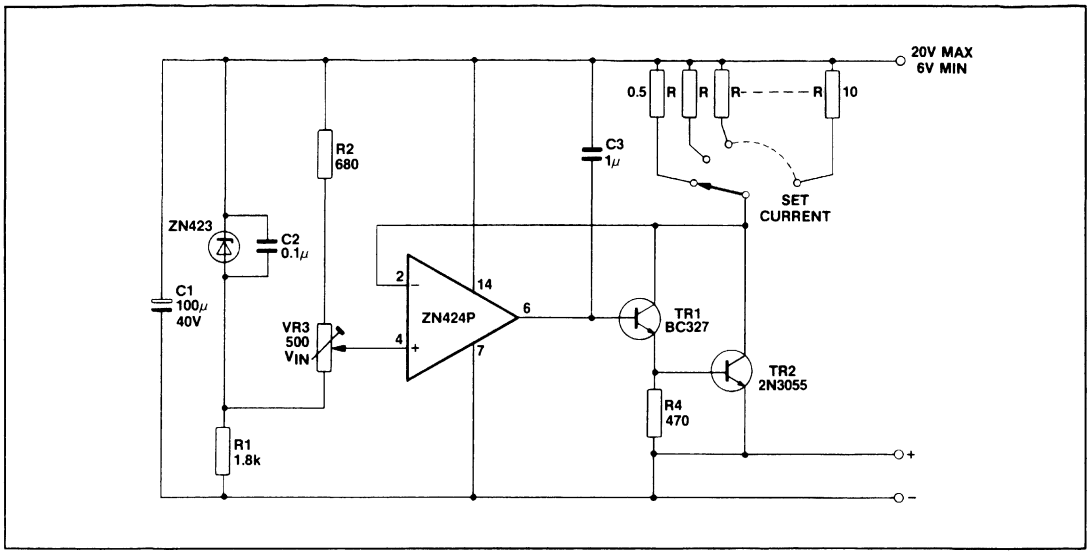


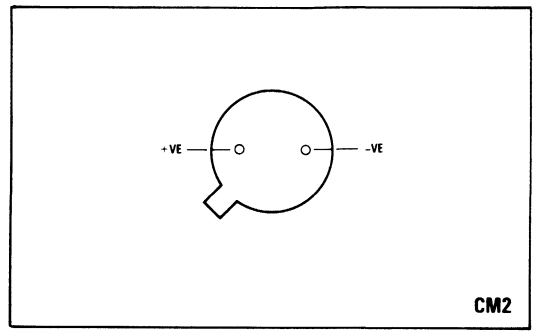
Fig.7 Variable current source

PLESSEY
Semiconductors

ZN458

2.45V PRECISION REFERENCE REGULATOR

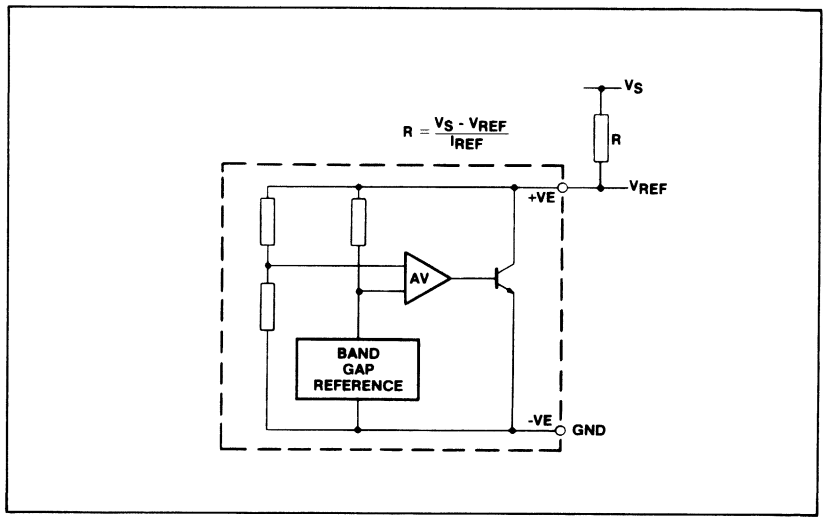
The ZN458 is a monolithic integrated circuit providing a precise stable reference source of 2.45V in a two lead package without the need for an external shaping capacitor.



Pin connections - bottom view

FEATURES

- Guaranteed 5mV Maximum Deviation over Full Temperature Range
- Low Temperature Coefficient 0.003%/ °C
- Low Slope Resistance — 0.1 Ohms
- Very Good Long Term Stability — 10ppm
- Low Noise — 10 microvolts
- Internally Shaped
- Tight Tolerance ±1.43%
- Two Pin Package
- Wide Operating Current 2-120mA



Circuit diagram

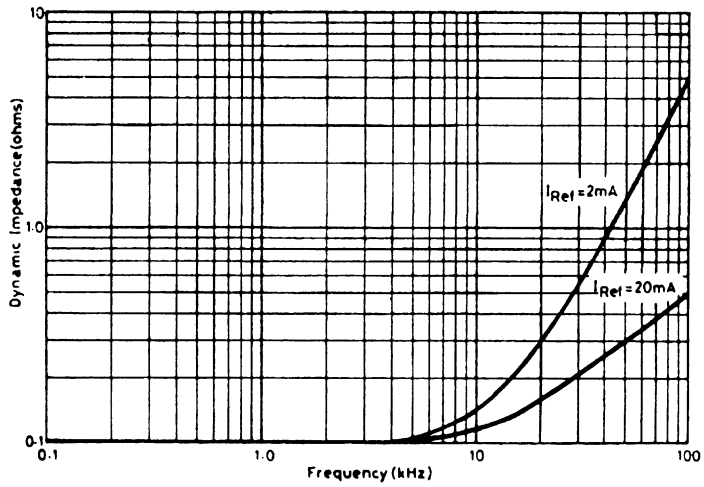
ABSOLUTE MAXIMUM RATINGS

Dissipation	300mW
Operating temperature range	−20 to +70°C
Storage temperature range	−55 to +150°C

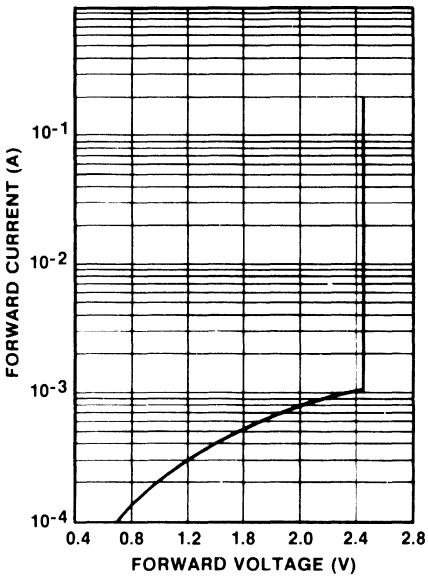
ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C unless otherwise specified).

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Output voltage	V_{REF}	2.42	2.45	2.49	V	Measured at 2mA
Slope resistance	R_{REF}	–	0.1	0.2	Ω	
Reference current	I_{REF}	2.0	–	120	mA	
Maximum change in V_{REF} ZN458	ΔV_{REF}	–	10	17	mV	0 to +70°C
Maximum change in V_{REF} ZN458A	ΔV_{REF}	–	6	8.5	mV	0 to +70°C
Maximum change in V_{REF} ZN458B	ΔV_{REF}	–	4	5	mV	0 to +70°C
RMS noise voltage 1Hz-10kHz		–	10	–	μV	
V_{REF} drift at 70°C		–	±10	–	ppm/1000 hours	

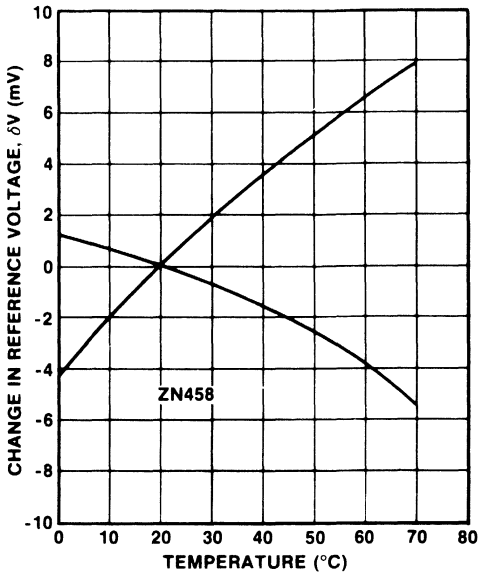
Dynamic impedance



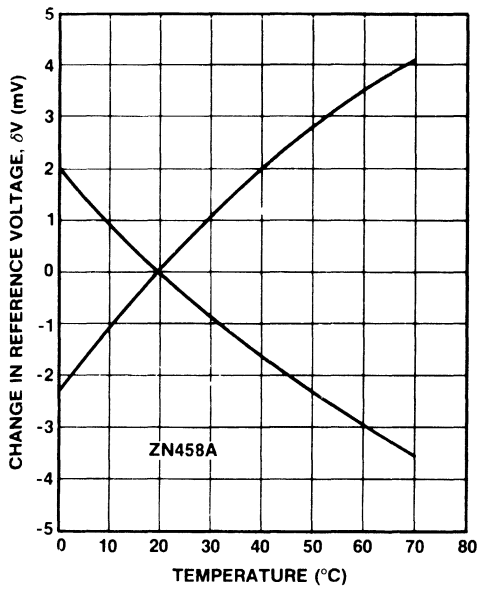
Forward characteristic

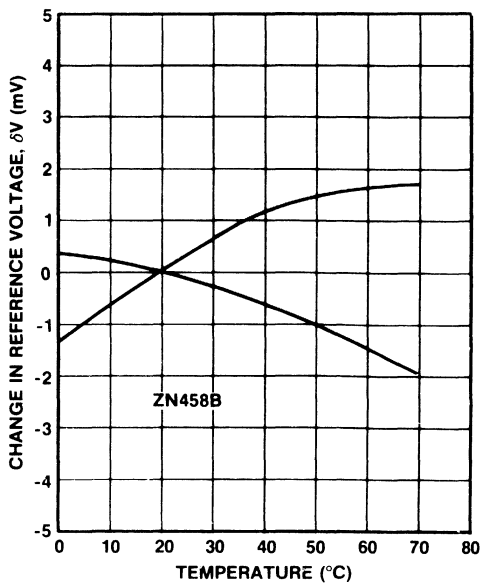


Temperature characteristic (typical)

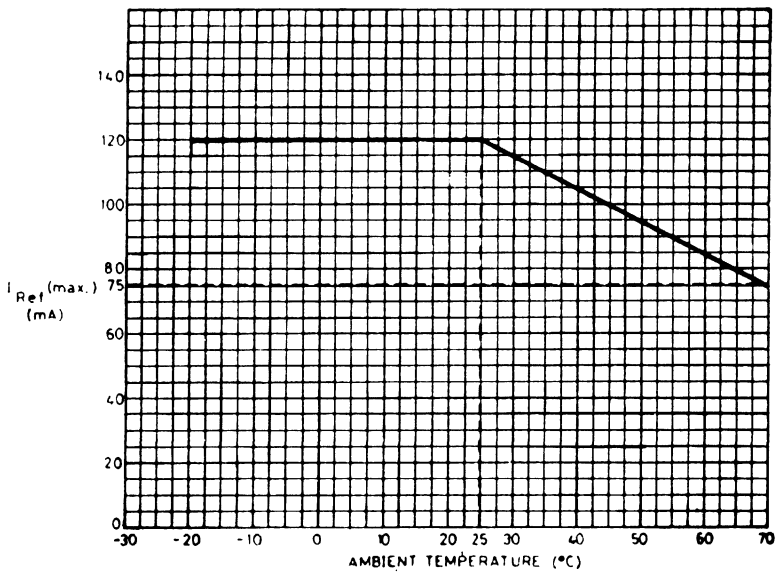


Temperature characteristics (typical)





Derating curve



PLESSEY
Semiconductors

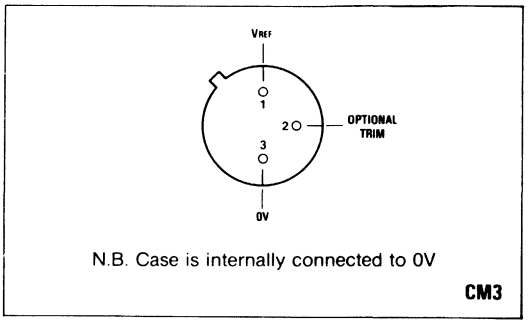
ZNREF025

2.5V LOW POWER PRECISION REFERENCE SOURCE

The ZNREF025 is a monolithic integrated circuit providing a precise stable reference voltage of 2.50V at 500μA.

The circuit features a knee current of 150μA and operation over a wide range of temperatures and currents.

The ZNREF025 is available in a 3-pin metal can package with pin 2 offering a trim facility whereby the output voltage can be adjusted as shown in Fig.1. This facility is used when compensating for system errors or setting the reference output to a particular value. When the trim facility is not used, pin 2 should be left open circuit.



N.B. Case is internally connected to 0V

CM3

Pin connections (bottom view)

FEATURES

- Trimmable Output
- Excellent Temperature Stability
- Low Output Noise Figure
- Available in Two Temperature Ranges
- 1 and 2% Initial Voltage Tolerance Versions Available
- No External Stabilising Capacitor required in most cases
- Low Slope Resistance

ORDERING INFORMATION

Device	Tol. %	TC (ppm/°C)	Temperature range
ZNREF025 A1	1	50	-55°C to +125°C
ZNREF025 C1	1	50	0°C to +70°C
ZNREF025 C2	2		

ABSOLUTE MAXIMUM RATINGS

Reference current	10mA*
Power dissipation	300mW
Operating temperature range	See ordering information
Storage temperature range	-55°C to +175°C
Soldering temperature for a maximum time of 10s	
Within $\frac{1}{16}$ in of the seating plane	300°C
Within $\frac{1}{32}$ in of the seating plane	265°C

*Below -25°C this figure should be linearly derated to 1.5mA maximum at -55°C.

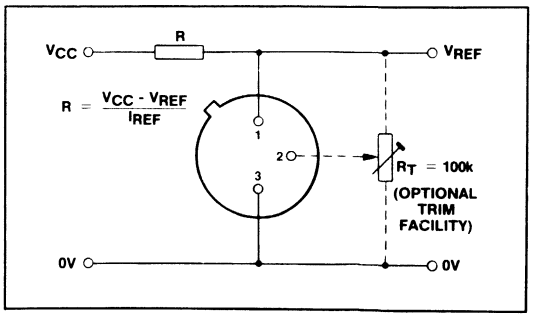


Fig.1 ZNREF025 application circuit

TEMPERATURE DEPENDENT ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Initial voltage tolerance %	Grade A −55 to 125°C		Grade C 0 to 70°C		Units
			Typ.	Max.	Typ.	Max.	
Output voltage change over relevant temperature range (See note (a))	ΔV_{REF}	1 & 2	16.0	22.5	2.7	8.8	mV
Output voltage temperature coefficient (See note (b))	TCV_{REF}	1 & 2	35	50	15	50	ppm/°C

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25°C$ and Pin 2 o/c unless otherwise specified). **(LOAD CAPACITANCE** should be less than 220pF or greater than 22nF).

Parameter	Symbol	Min.	Typ.	Max.	Units	Comments
Output voltage 1% tolerance (A1 C1) 2% tolerance (C2)	V_{REF}	 2.475 2.450	 2.500 2.500	 2.525 2.550	V	$I_{REF} = 500\mu A$
Output voltage adjustment range	ΔV_{TRIM}	–	±5	–	%	$R_T = 100k\Omega$
Change in TCV_{REF} with output adjustment	$TC\Delta V_{TRIM}$	–	0.8	–	ppm/°C/%	
Operating current range	I_{REF}	0.15	–	10	mA	See note (c)
Turn-on time Turn-off time	t_{on} t_{off}	– –	40 0.3	– –	μS	$R_L = 1k\Omega$
Output voltage noise (over the range 0.1 to 10Hz)	e_{np-p}	–	50	–	μV	Peak to peak measurement
Slope resistance	R_{REF}	–	1.5	2.0	Ω	I_{REF} 0.5mA to 5mA See note (d)

NOTES

(a) Output change with temperature (ΔV_{REF})
The absolute maximum difference between the maximum output voltage and the minimum output voltage over the specified temperature range

$$\Delta V_{REF} = V_{max} - V_{min}$$

(b) Output temperature coefficient (TCV_{REF})
The ratio of the output change with temperature to the specified temperature range expressed in ppm/°C.

$$TCV_{REF} = \frac{\Delta V_{REF} \times 10^6}{V_{REF} \times \Delta T} \text{ ppm/°C}$$

ΔT = Full temperature change.

(c) Operating current (I_{REF})
Maximum operating current must be derated as indicated in maximum ratings.

(d) Slope resistance (R_{REF})
The slope resistance is defined as R_{REF} = change in V_{REF} overspecified current range

$\Delta I_{REF} = 5 - 0.5 = 4.5mA$ (typically)

(e) Line regulation

The ratio of change in output voltage to the change in input voltage producing it.

$$\frac{R_{REF} \times 100}{V_{REF} \times R_S} \text{ %/V}$$

R_S = Source resistance

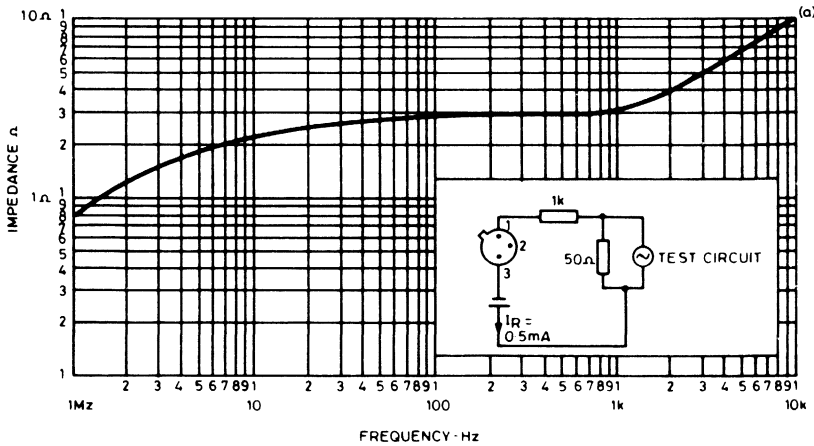


Fig.2 Dynamic impedance (typical)

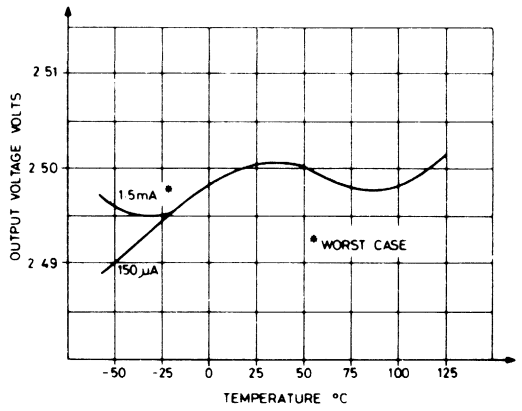


Fig.3 Typical temperature characteristics

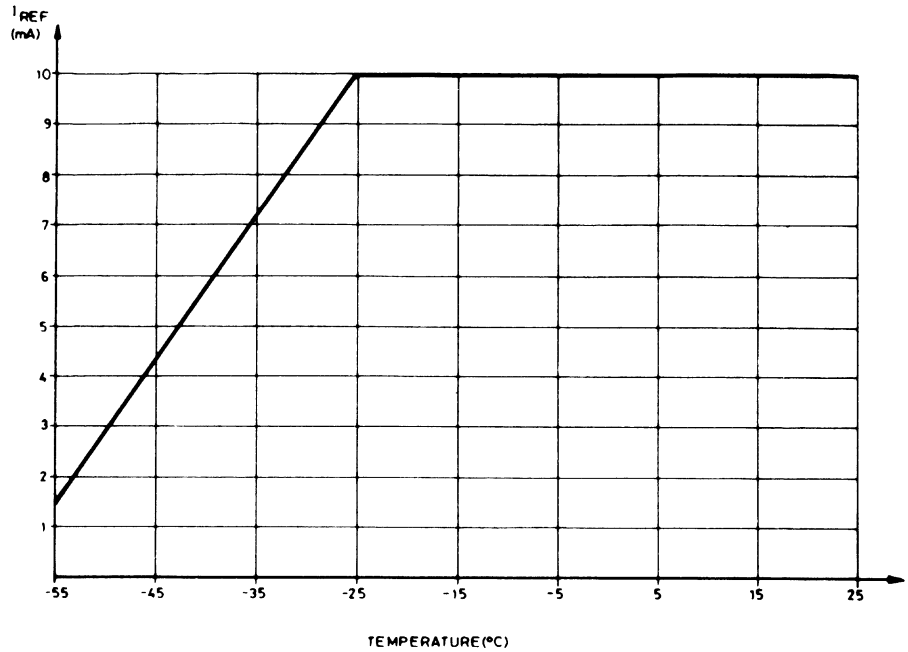


Fig.4 I_{REF} derating for ZNREF025

PLESSEY
Semiconductors

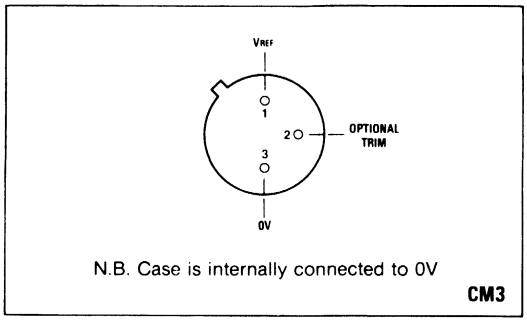
ZNREF040

4V LOW POWER PRECISION REFERENCE SOURCE

The ZNREF040 is a monolithic integrated circuit providing a precise stable reference voltage of 4.01V at 500μA.

The circuit features a knee current of 150μA and operation over a wide range of temperatures and currents.

The ZNREF040 is available in a 3-pin metal can package with pin 2 offering a trim facility whereby the output voltage can be adjusted as shown in Fig.1. This facility is used when compensating for system errors or setting the reference output to a particular value. When the trim facility is not used, pin 2 should be left open circuit.



N.B. Case is internally connected to 0V

CM3

Pin connections (bottom view)

FEATURES

- Trimmable Output
- Excellent Temperature Stability
- Low Output Noise Figure
- Available in Two Temperature Ranges
- 1 and 2% Initial Voltage Tolerance Versions Available
- No External Stabilising Capacitor required in most cases
- Low Slope Resistance

ORDERING INFORMATION

Device	Tol. %	TC (ppm/°C)	Temperature range
ZNREF040 A1	1	50	-55°C to +125°C
ZNREF040 C1	1	50	0°C to +70°C
ZNREF040 C2	2		

ABSOLUTE MAXIMUM RATINGS

Reference current	75mA*
Power dissipation	300mW
Operating temperature range	See ordering information
Storage temperature range	-55°C to +175°C
Soldering temperature for a maximum time of 10s	
Within $\frac{1}{16}$ in of the seating plane	300°C
Within $\frac{1}{32}$ in of the seating plane	265°C

*Above 25°C this figure should be linearly derated to 20mA at +125°C.

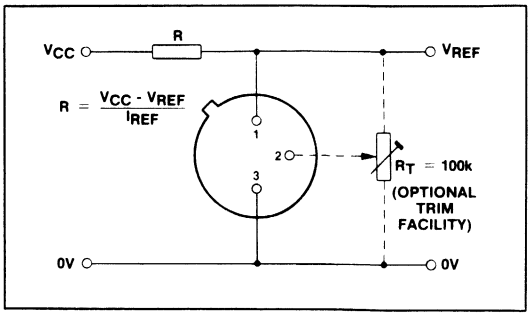


Fig.1 ZNREF040 application circuit

TEMPERATURE DEPENDENT ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Initial voltage tolerance %	Grade A −55 to 125°C		Grade C 0 to 70°C		Units
			Typ.	Max.	Typ.	Max.	
Output voltage change over relevant temperature range (See note (a))	ΔV_{REF}	1 & 2	25.6	36	4.2	14	mV
Output voltage temperature coefficient (See note (b))	TCV_{REF}	1 & 2	35	50	15	50	ppm/°C

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25°C$ and Pin 2 o/c unless otherwise specified).

Parameter	Symbol	Min.	Typ.	Max.	Units	Comments
Output voltage 1% tolerance (A1 C1) 2% tolerance (C2)	V_{REF}	 3.97 3.93	 4.01 4.01	 4.05 4.09	V	$I_{REF} = 500\mu A$
Output voltage adjustment range	ΔV_{TRIM}	–	±5	–	%	$R_T = 100k\Omega$
Change in TCV_{REF} with output adjustment	$TC\Delta V_{TRIM}$	–	0.8	–	ppm/°C/%	
Operating current range	I_{REF}	0.15	–	75	mA	See note (c)
Turn-on time Turn-off time	t_{on} t_{off}	– –	40 0.3	– –	μs	$R_L = 1k\Omega$
Output voltage noise (over the range 0.1 to 10Hz)	$e_{np\text{-}p}$	–	50	–	μV	Peak to peak measurement
Slope resistance	R_{REF}	–	2	3	Ω	I_{REF} 0.5mA to 5mA, See note (d)

NOTES

(a) Output change with temperature (ΔV_{REF})
The absolute maximum difference between the maximum output voltage and the minimum output voltage over the specified temperature range

$$\Delta V_{REF} = V_{max} - V_{min}$$

(b) Output temperature coefficient (TCV_{REF})
The ratio of the output change with temperature to the specified temperature range expressed in ppm/°C.

$$TCV_{REF} = \frac{\Delta V_{REF} \times 10^6}{V_{REF} \times \Delta T} \text{ ppm/°C}$$

ΔT = Full temperature change.

(c) Operating current (I_{REF})
Maximum operating current must be derated as indicated in maximum ratings.

(d) Slope resistance (R_{REF})
The slope resistance is defined as R_{REF} = change in V_{REF} overspecified current range

$\Delta I_{REF} = 5 - 0.5 = 4.5mA$ (typically)

(e) Line regulation

The ratio of change in output voltage to the change in input voltage producing it.

$$\frac{R_{REF} \times 100}{V_{REF} \times R_S} \text{ %/V}$$

R_S = Source resistance

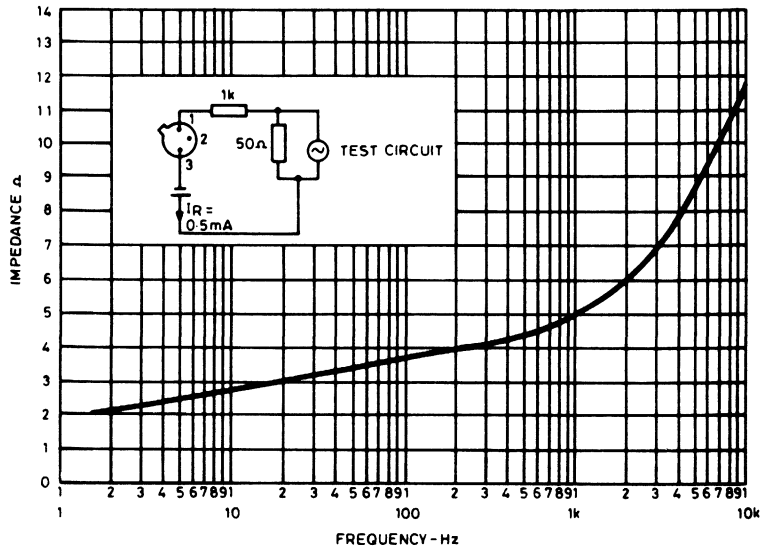


Fig.2 Dynamic impedance (typical)

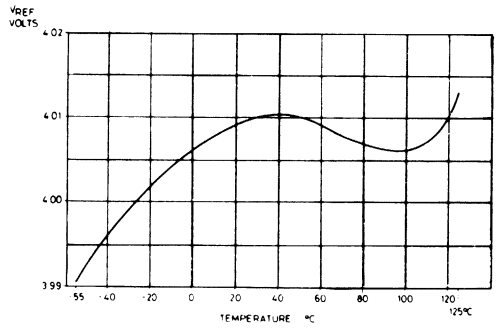


Fig.3 Typical temperature characteristics

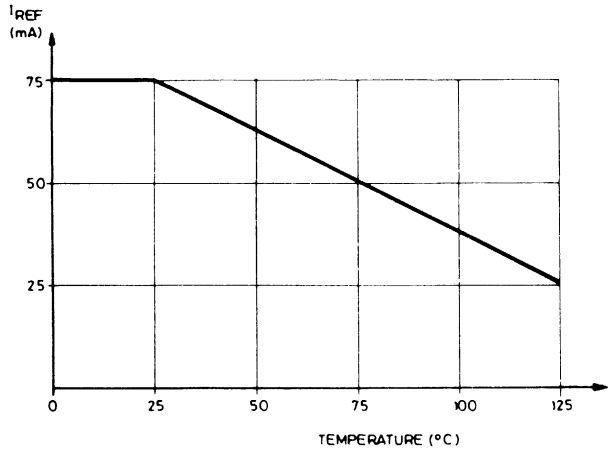


Fig.4 I_{REF} derating for ZNREF040

PLESSEY
Semiconductors

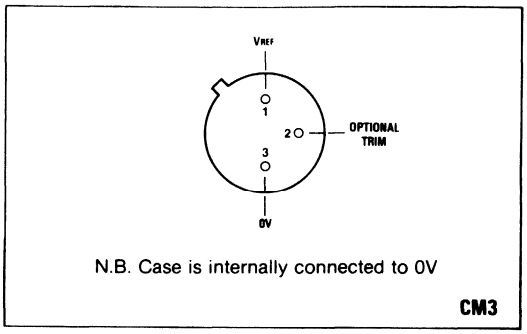
ZNREF050

5V LOW POWER PRECISION REFERENCE SOURCE

The ZNREF050 is a monolithic integrated circuit providing a precise stable reference voltage of 4.90V at 500μA.

The circuit features a knee current of 150μA and operation over a wide range of temperatures and currents.

The ZNREF050 is available in a 3-pin metal can package with pin 2 offering a trim facility whereby the output voltage can be adjusted as shown in Fig.1. This facility is used when compensating for system errors or setting the reference output to a particular value. When the trim facility is not used, pin 2 should be left open circuit.



N.B. Case is internally connected to 0V

CM3

Pin connections (bottom view)

FEATURES

- Trimmable Output
- Excellent Temperature Stability
- Low Output Noise Figure
- Available in Two Temperature Ranges
- 1 and 2% Initial Voltage Tolerance Versions Available
- No External Stabilising Capacitor required in most cases
- Low Slope Resistance

ORDERING INFORMATION

Device	Tol. %	TC (ppm/°C)	Temperature range
ZNREF050 A1	1	50	-55°C to +125°C
ZNREF050 C1	1	50	0°C to +70°C
ZNREF050 C2	2		

ABSOLUTE MAXIMUM RATINGS

Reference current	60mA*
Power dissipation	300mW
Operating temperature range	See ordering information
Storage temperature range	-55°C to +175°C
Soldering temperature for a maximum time of 10s	
Within 1/16 in of the seating plane	300°C
Within 1/32 in of the seating plane	265°C

*Above 25°C this figure should be linearly derated to 20mA at +125°C.

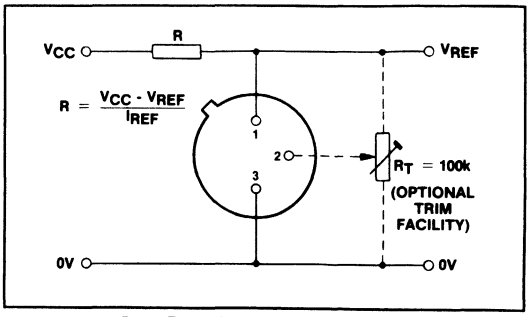


Fig.1 ZNREF050 application circuit

TEMPERATURE DEPENDENT ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Initial voltage tolerance %	Grade A −55 to 125°C		Grade C 0 to 70°C		Units
			Typ.	Max.	Typ.	Max.	
Output voltage change over relevant temperature range (See note (a))	ΔV_{REF}	1 & 2	32	45	5.4	17.2	mV
Output voltage temperature coefficient (See note (b))	TCV_{REF}	1 & 2	35	50	15	50	ppm/°C

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25°C$ and Pin 2 o/c unless otherwise specified).

Parameter	Symbol	Min.	Typ.	Max.	Units	Comments
Output voltage 1% tolerance (A1 C1) 2% tolerance (C2)	V_{REF}	 4.85 4.80	 4.90 4.90	 4.95 5.00	V	$I_{REF} = 500\mu A$
Output voltage adjustment range	ΔV_{TRIM}	–	±5	–	%	$R_T = 100k\Omega$
Change in TCV_{REF} with output adjustment	$TC\Delta V_{TRIM}$	–	0.8	–	ppm/°C/%	
Operating current range	I_{REF}	0.15	–	60	mA	See note (c)
Turn-on time Turn-off time	t_{on} t_{off}	– –	40 0.3	– –	μs	$R_L = 1k\Omega$
Output voltage noise (over the range 0.1 to 10Hz)	$e_{np\text{-}p}$	–	50	–	μV	Peak to peak measurement
Slope resistance	R_{REF}	–	1.5	2	Ω	I_{REF} 0.5mA to 5mA, See note (d)

NOTES

(a) Output change with temperature (ΔV_{REF})
The absolute maximum difference between the maximum output voltage and the minimum output voltage over the specified temperature range

$$\Delta V_{REF} = V_{max} - V_{min}$$

(b) Output temperature coefficient (TCV_{REF})
The ratio of the output change with temperature to the specified temperature range expressed in ppm/°C.

$$TCV_{REF} = \frac{\Delta V_{REF} \times 10^6}{V_{REF} \times \Delta T} \text{ ppm/°C}$$

ΔT = Full temperature change.

(c) Operating current (I_{REF})
Maximum operating current must be derated as indicated in maximum ratings.

(d) Slope resistance (R_{REF})
The slope resistance is defined as R_{REF} = change in V_{REF} overspecified current range

$\Delta I_{REF} = 5 - 0.5 = 4.5mA$ (typically)

(e) Line regulation

The ratio of change in output voltage to the change in input voltage producing it.

$$\frac{R_{REF} \times 100}{V_{REF} \times R_S} \text{ %/V}$$

R_S = Source resistance

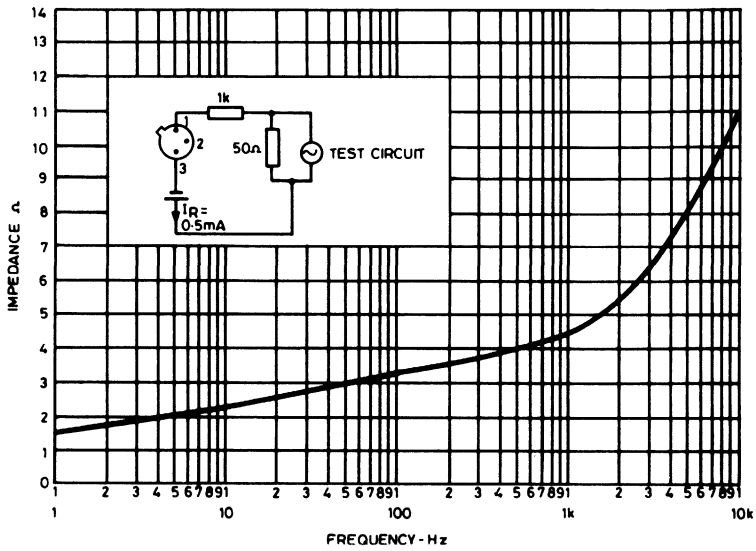


Fig.2 Dynamic impedance (typical)

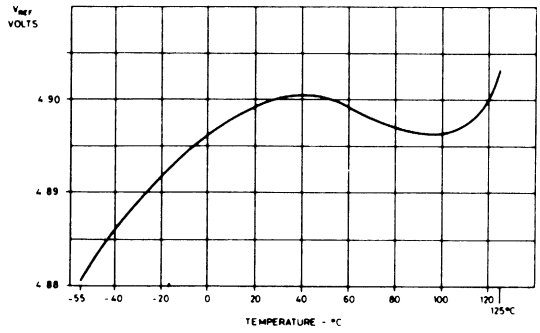


Fig.3 Typical temperature characteristics

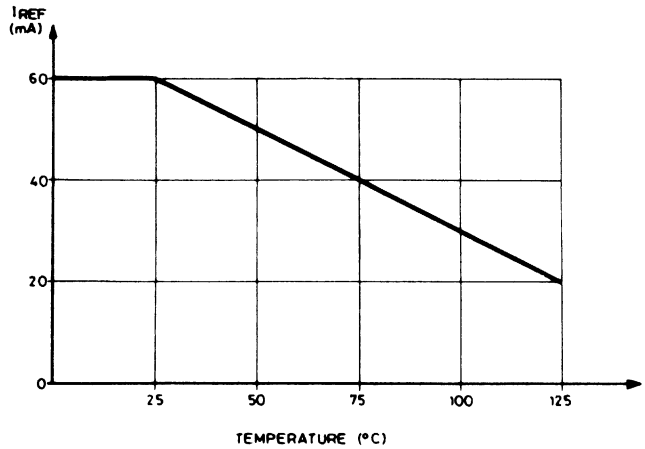


Fig.4 I_{REF} derating for ZNREF050

PLESSEY
Semiconductors

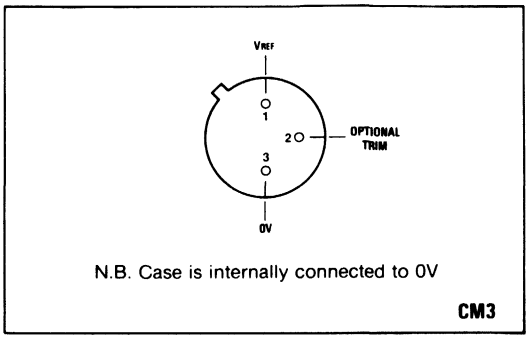
ZNREF062

6.2V LOW POWER PRECISION REFERENCE SOURCE

The ZNREF062 is a monolithic integrated circuit providing a precise stable reference voltage of 6.17V at 500μA.

The circuit features a knee current of 150μA and operation over a wide range of temperatures and currents.

The ZNREF062 is available in a 3-pin metal can package with pin 2 offering a trim facility whereby the output voltage can be adjusted as shown in Fig.1. This facility is used when compensating for system errors or setting the reference output to a particular value. When the trim facility is not used, pin 2 should be left open circuit.



Pin connections (bottom view)

FEATURES

- Trimmable Output
- Excellent Temperature Stability
- Low Output Noise Figure
- Available in Two Temperature Ranges
- 1 and 2% Initial Voltage Tolerance Versions Available
- No External Stabilising Capacitor required in most cases
- Low Slope Resistance

ORDERING INFORMATION

Device	Tol. %	TC (ppm/°C)	Temperature range
ZNREF062 AB	1	50	-55°C to +110°C
ZNREF062 C1	1	50	0°C to +70°C
ZNREF062 C2	2		

ABSOLUTE MAXIMUM RATINGS

Reference current	50mA*
Power dissipation	300mW
Operating temperature range	See ordering information
Storage temperature range	-55°C to +175°C
Soldering temperature for a maximum time of 10s	
Within 1/16 in of the seating plane	300°C
Within 1/32 in of the seating plane	265°C

*Below -25°C this figure should be linearly derated to 20mA at +110°C.

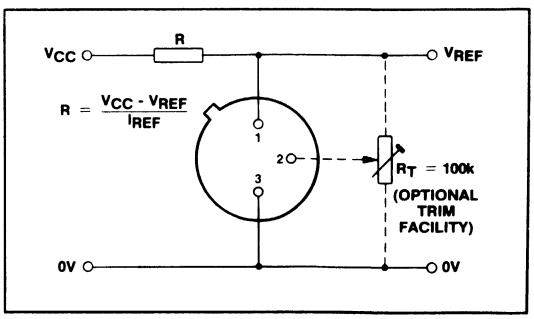


Fig.1 ZNREF062 application circuit

TEMPERATURE DEPENDENT ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Initial voltage tolerance %	Grade AB -55 to 110°C		Grade C 0 to 70°C		Units
			Typ.	Max.	Typ.	Max.	
Output voltage change over relevant temperature range (See note (a))	ΔV_{REF}	1 & 2	26	40	6.5	22	mV
Output voltage temperature coefficient (See note (b))	TCV_{REF}	1 & 2	25	40	15	50	ppm/°C

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25°C$ and Pin 2 o/c unless otherwise specified).

Parameter	Symbol	Min.	Typ.	Max.	Units	Comments
Output voltage 1% tolerance (AB C1) 2% tolerance (C2)	V_{REF}	 6.11 6.05	 6.17 6.17	 6.23 6.29	V	$I_{REF} = 500\mu A$
Output voltage adjustment range	ΔV_{TRIM}	–	±5	–	%	$R_T = 100k\Omega$
Change in TCV_{REF} with output adjustment	$TC\Delta V_{TRIM}$	–	0.8	–	ppm/°C/%	
Operating current range	I_{REF}	0.15	–	50	mA	See note (c)
Turn-on time Turn-off time	t_{on} t_{off}	– –	40 0.3	– –	μs	$R_L = 1k\Omega$
Output voltage noise (over the range 0.1 to 10Hz)	$e_{np\ p}$	–	50	–	μV	Peak to peak measurement
Slope resistance	R_{REF}	–	2	3	Ω	I_{REF} 0.5mA to 5mA, See note (d)

NOTES

(a) Output change with temperature (ΔV_{REF})
The absolute maximum difference between the maximum output voltage and the minimum output voltage over the specified temperature range

$$\Delta V_{REF} = V_{max} - V_{min}$$

(b) Output temperature coefficient (TCV_{REF})
The ratio of the output change with temperature to the specified temperature range expressed in ppm/°C.

$$TCV_{REF} = \frac{\Delta V_{REF} \times 10^6}{V_{REF} \times \Delta T} \text{ ppm/°C}$$

ΔT = Full temperature change.

(c) Operating current (I_{REF})
Maximum operating current must be derated as indicated in maximum ratings.

(d) Slope resistance (R_{REF})
The slope resistance is defined as R_{REF} = change in V_{REF} overspecified current range

$\Delta I_{REF} = 5 - 0.5 = 4.5mA$ (typically)

(e) Line regulation

The ratio of change in output voltage to the change in input voltage producing it.

$$\frac{R_{REF} \times 100}{V_{REF} \times R_S} \text{ %/V}$$ R_S = Source resistance

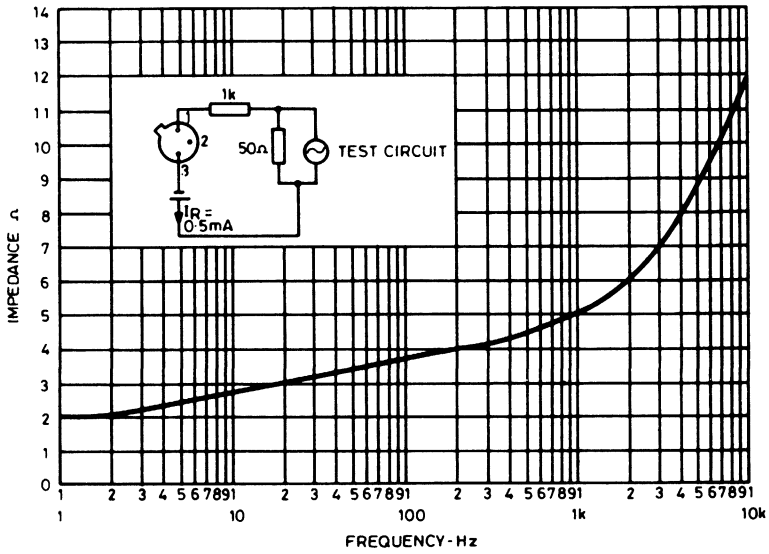


Fig.2 Dynamic impedance (typical)

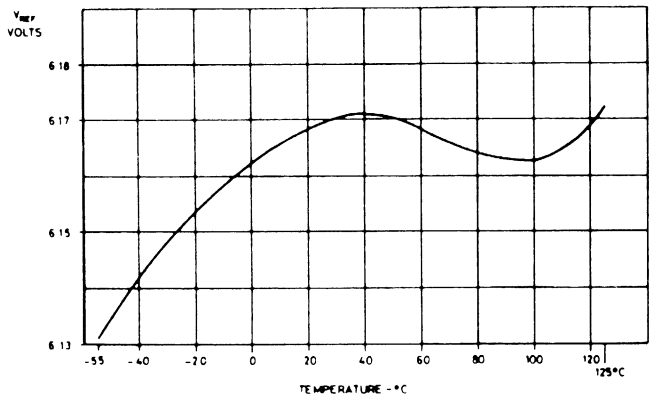


Fig.3 Typical temperature characteristics

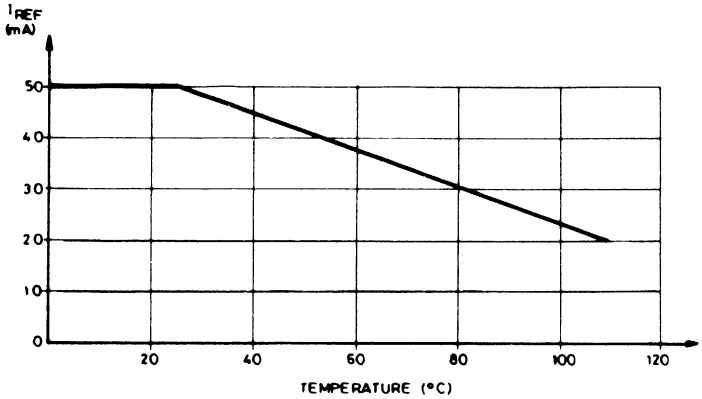


Fig.4 I_{REF} derating for ZNREF062

PLESSEY
Semiconductors

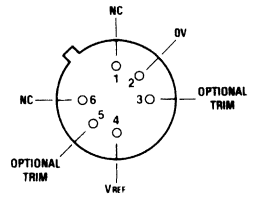
ZNREF100

10V LOW POWER PRECISION REFERENCE SOURCE

The ZNREF100 is a monolithic integrated circuit providing a precise stable reference voltage of 9.80V at 500μA.

The circuit features a knee current of 150μA and operation over a wide range of temperatures and currents.

The ZNREF100 is available in a 6-pin metal can package with pins 3 and 5 offering a trim facility whereby the output voltage can be adjusted as shown in Fig.1. This facility is used when compensating for system errors or setting the reference output to a particular value. When the trim facility is not used, pins 3 and 5 should be left open circuit.



No connection should be made to pins 1 and 6

CM6

Pin connections (bottom view)

FEATURES

- Trimmable Output
- Excellent Temperature Stability
- Low Output Noise Figure
- Available in Two Temperature Ranges
- 1 and 2% Initial Voltage Tolerance Versions Available
- No External Stabilising Capacitor required in most cases
- Low Slope Resistance

ORDERING INFORMATION

Device	Tol. %	TC (ppm/°C)	Temperature range
ZNREF100 A1	1	50	-55°C to +125°C
ZNREF100 C1	1	50	0°C to +70°C
ZNREF100 C2	2		

ABSOLUTE MAXIMUM RATINGS

Reference current	50mA*
Power dissipation	500mW
Operating temperature range	See ordering information
Storage temperature range	-55°C to +175°C
Soldering temperature for a maximum time of 10s	
Within 1/16 in of the seating plane	300°C
Within 1/32 in of the seating plane	265°C

*Above 25°C this figure should be linearly derated to 16mA at +125°C.

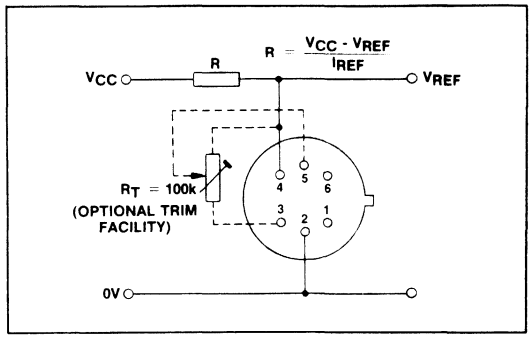


Fig.1 ZNREF100 application circuit

TEMPERATURE DEPENDENT ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Initial voltage tolerance %	Grade A −55 to 125°C		Grade C 0 to 70°C		Units
			Typ.	Max.	Typ.	Max.	
Output voltage change over relevant temperature range (See note (a))	ΔV_{REF}	1 & 2	64	90	10.8	34.4	mV
Output voltage temperature coefficient (See note (b))	TCV_{REF}	1 & 2	35	50	15	50	ppm/°C

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25°C$ and pins 3 and 5 o/c unless otherwise noted).

Parameter	Symbol	Min.	Typ.	Max.	Units	Comments
Output voltage 1% tolerance (A1 C1) 2% tolerance (C2)	V_{REF}	 9.70 9.60	 9.80 9.80	 9.90 10.00	V	$I_{REF} = 500\mu A$
Output voltage adjustment range	ΔV_{TRIM}	–	±2.5	–	%	$R_T = 100k\Omega$
Change in TCV_{REF} with output adjustment	$TC\Delta V_{TRIM}$	–	0.8	–	ppm/°C/%	
Operating current range	I_{REF}	0.15	–	50	mA	See note (c)
Turn-on time Turn-off time	t_{on} t_{off}	– –	40 0.3	– –	μs	$R_L = 1k\Omega$
Output voltage noise (over the range 0.1 to 10Hz)	e_{np-p}	–	50	–	μV	Peak to peak measurement
Slope resistance	R_{REF}	–	3	4	Ω	I_{REF} 0.5mA to 5mA, See note (d)

NOTES

(a) Output change with temperature (ΔV_{REF})
The absolute maximum difference between the maximum output voltage and the minimum output voltage over the specified temperature range

$$\Delta V_{REF} = V_{max} - V_{min}$$

(b) Output temperature coefficient (TCV_{REF})
The ratio of the output change with temperature to the specified temperature range expressed in ppm/°C.

$$TCV_{REF} = \frac{\Delta V_{REF} \times 10^6}{V_{REF} \times \Delta T} \text{ ppm/°C}$$

ΔT = Full temperature change.

(c) Operating current (I_{REF})
Maximum operating current must be derated as indicated in maximum ratings.

(d) Slope resistance (R_{REF})
The slope resistance is defined as R_{REF} = change in V_{REF} overspecified current range

$\Delta I_{REF} = 5 - 0.5 = 4.5mA$ (typically)

(e) Line regulation

The ratio of change in output voltage to the change in input voltage producing it.

$$\frac{R_{REF} \times 100}{V_{REF} \times R_S} \text{ %/V}$$ R_S = Source resistance

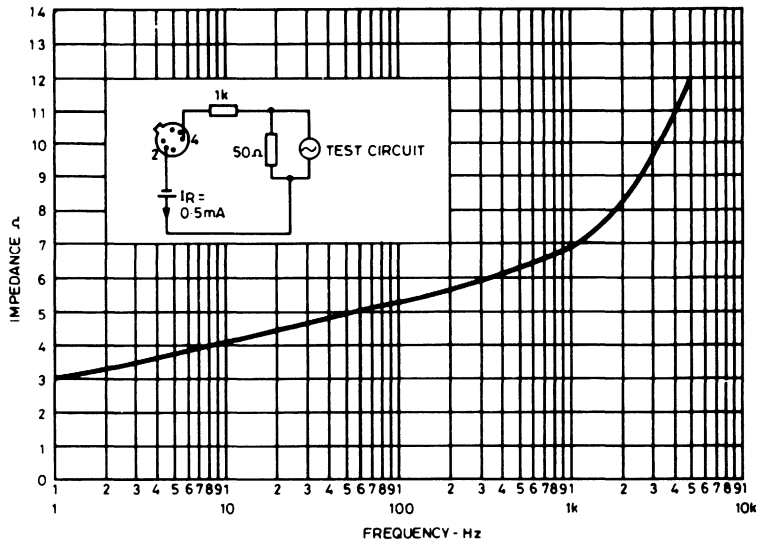


Fig.2 Dynamic impedance (typical)

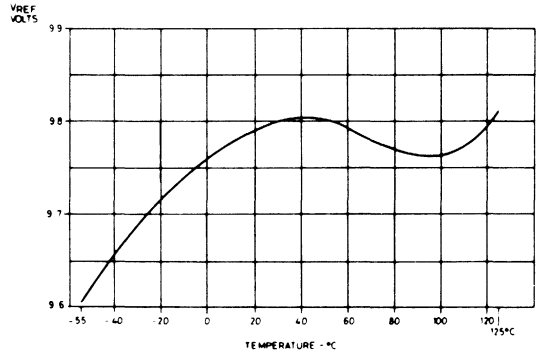


Fig.3 Typical temperature characteristics

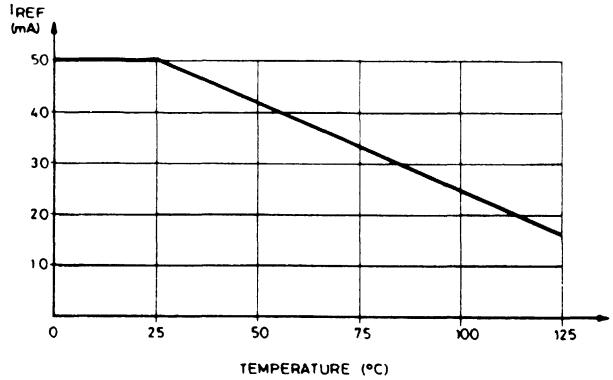


Fig.4 I_{REF} derating for ZNREF100

Application Notes

Digital to Analogue Converters

1. A digital to analogue converter (DAC) is a device which converts a digital data input into a corresponding analogue output. This output usually takes the form of a voltage or current.

1.1 Ideal output characteristics

If a unipolar voltage output and normal binary coding are assumed, then the ideal transfer function of a linear DAC may be written as:

$$V_{out} = V_{FS} \ (B_1.2^{-1} + B_2.2^{-2} + B_3.2^{-3} + ... + B_n.2^{-n})$$

where B_1 is the most significant bit input (MSB) and B_n is the least significant bit input (LSB). Bits 1 to n can each assume a value of '1' or '0'. The number of bit inputs a DAC possesses is known as the **resolution** of the converter.

The smallest increment of output voltage is that contributed by the LSB and is equal to $V_{FS}.2^{-n}$.

The terms 'MSB', 'LSB' etc., are frequently used interchangeably to describe either the digital input or the corresponding analogue output.

The maximum output from a DAC is known as full-scale output (V_{FSO}).

It occurs when all inputs are '1' and is equal to $V_{FS}\left(\frac{(2^n - 1)}{2^n}\right)$. For example the maximum output of a 3-bit DAC is ⅞ V_{FS}.

The transfer function graph of an ideal 3-bit DAC is shown in Fig. 1. For each of the 8 input codes there exists a discrete analogue output level,

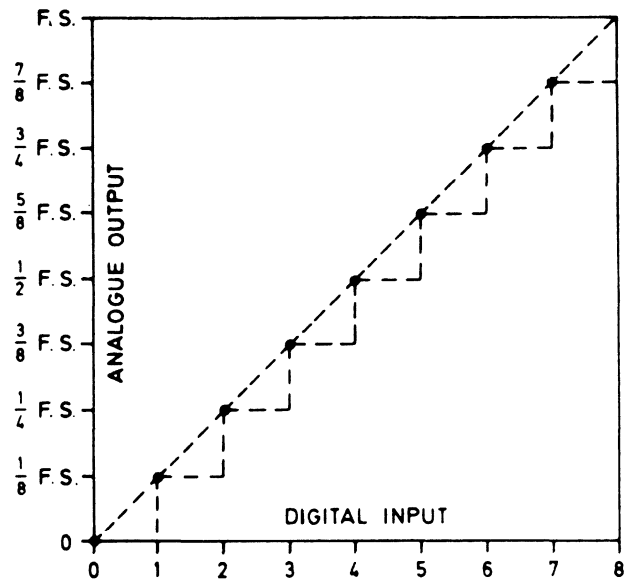


Fig. 1 Transfer characteristics of ideal 3-bit DAC

represented by a point on the graph. It should be emphasised that the transfer characteristic is not a continuous function and it is, therefore, not strictly correct to join the points with a continuous line, since this would imply that non-integral input codes and corresponding levels existed. However, a straight line is often drawn between zero and full-scale to represent the 'ideal' transfer function on which all the points should lie.

Similarly, if the input code of a DAC is incremented using, say a binary counter and clock generator, then the analogue output will be a staircase waveform. DAC transfer functions are frequently drawn as a staircase, since this is a convenient way of illustrating various errors that may occur in a DAC. However, such a graph is, strictly speaking, a plot of analogue output v time rather than output v input code.

1.2 Practical DAC circuits

Fig.2 shows an example of a 3-bit DAC circuit based on a voltage-switching R-2R ladder network, a technique widely used in Plessey converters.

Each 2R element is connected either to 0V or V_{FS} (V_{REF}) by transistor switches. Binary weighted voltages are produced at the output of the R-2R ladder, the value being proportional to the digital input number.

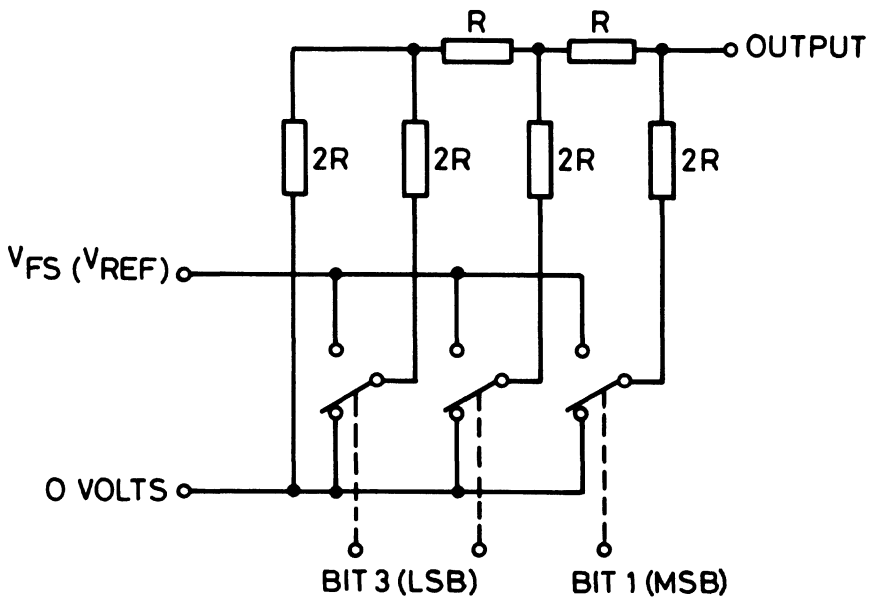


Fig. 2 3-bit voltage switching DAC

For example, it is fairly easy to see that if bit 1 is '1' and bit 2 and 3 are '0' then an output of $V_{FS}/2$ is produced. This is because the resistance of the ladder looking from the output through the first R is 2R, which forms a 2:1 attenuator with the 2R in series with the MSB switch. Output voltages for other input codes can similarly by calculated, and it can be seen that the ladder may be extended to any number of bits.

1.3 D-A parameters and definitions

1.3.1 Converter errors

The ideal DAC assumes that all the resistors are perfectly matched and that the switches have zero resistance. In a practical converter this will not be the case and various errors will occur in the output.

1.3.2 Monotonicity

When the input code of a DAC is increased in 1 LSB steps the analogue output of the DAC should also increase, staircase fashion. If the output always increases in this manner then the DAC is said to be monotonic, i.e. the output is a single-valued function of the input. If, due to errors in the bit weighting, the output of the DAC decreases at any step, as shown in Fig. 3, then the DAC is said to be non-monotonic.

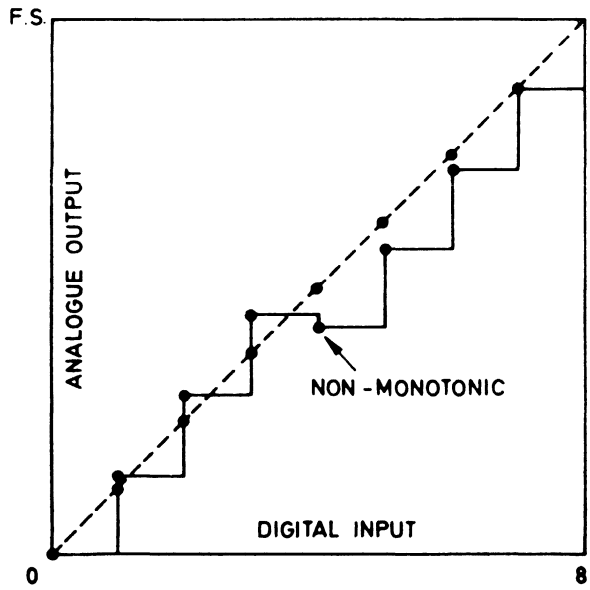


Fig. 3 Non-monotonic DAC

1.3.3 Offset (zero error)

Assuming unipolar operation and normal binary coding, when the input code is zero then the DAC outputs should also be zero. However, due to package lead resistances and offset voltages in the switches this will not be the case, and a small output offset may exist. This has the effect of shifting the transfer function so that it no longer passes through zero, as shown in Fig. 4.

1.3.4 Gain error

If the reference voltage of a DAC is exactly the nominal value then the transfer characteristics of the converter should follow the ideal straight line. However, due to imperfections in the converter the transfer function may diverge from this line, as shown in Fig. 4. This error is known as gain error and is the difference between the slope of the actual transfer characteristic and the slope of the ideal transfer characteristic.

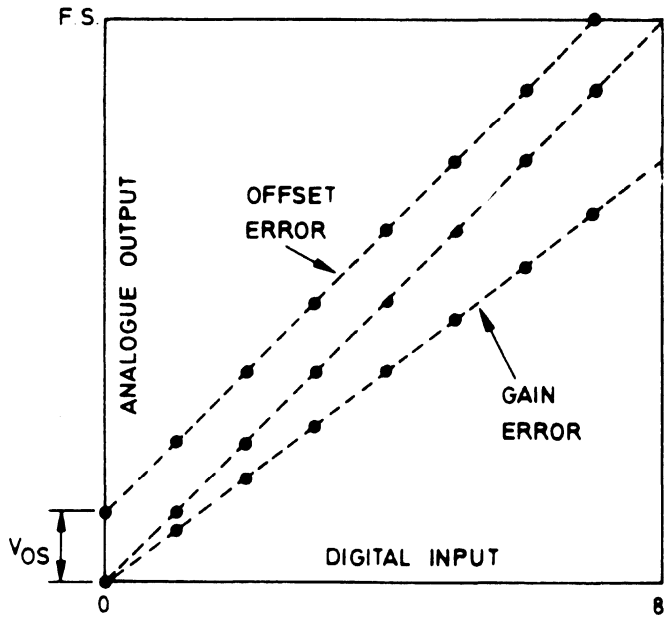


Fig. 4 Illustrating offset and gain errors

1.3.5 Linearity errors

Offset and gain errors may be trimmed out so that the end points of the transfer characteristics lie at zero and V_{FSO}. However, even when this has been done, some or all of the intermediate points may not lie on the 'ideal' line. These errors, which cannot be trimmed out, are known as linearity errors.

1.3.6 Non-linearity (linearity error)

This is the maximum amount, given either as a percentage of full-scale or a fraction of an LSB, by which any point on the transfer characteristic deviates from the ideal straight line passing through zero and V_{FSO}. Non-linearity is illustrated in Fig. 5. A linearity error within the range $\pm$ ½LSB assures monotonic operation. Note however that the converse is not true and a DAC may still be monotonic with large linearity errors, which is also shown by Fig. 5.

1.3.7 Differential non-linearity

This is the maximum difference, specified as a fraction of an LSB, between the actual and ideal size of any one LSB analogue increment. This can be seen as an error in the step height of a DAC staircase. A positive value of differential non-linearity means that the step height is larger than nominal, whilst a negative value means that it is smaller than nominal. If it is more negative than −1LSB then the DAC is non-monotonic. However, positive differential non-linearity may assume any value and a DAC can still be monotonic, as shown in Fig. 5.

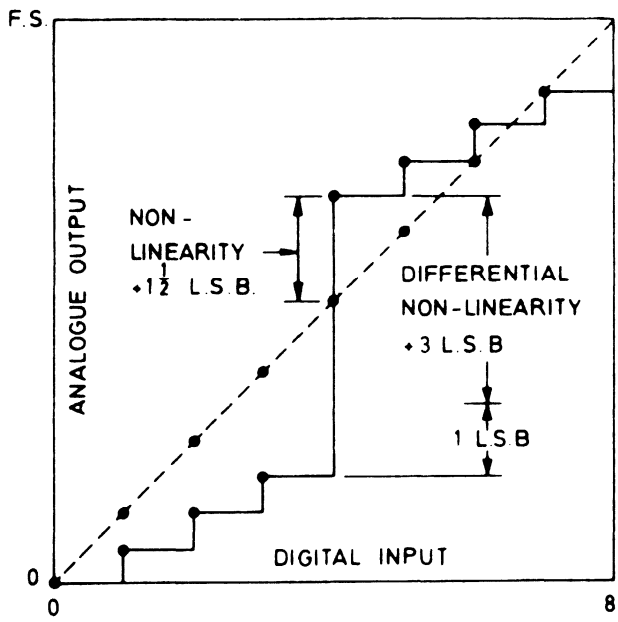


Fig. 5 Illustrating linearity errors

1.3.8 Resolution

As stated earlier, the resolution of a DAC is simply the number of bit inputs that a DAC possesses, which indicates the smallest analogue increment that the converter can produce as a fraction of V_{FS}. e.g. 8 bits = 1 part in 2^8(256). Resolution implies nothing about the accuracy of a DAC, which is defined by linearity and other errors.

1.3.9 Useful resolution

If an n bit DAC has a differential non-linearity of say −1.5LSB then it is non-monotonic. However, if the LSB input is made permanently '0' then the DAC becomes an n − 1 bit device with an LSB equal to twice the original LSB. The differential non-linearity error thus becomes −0.75(new)LSB and the device is monotonic at a resolution of n − 1 bits. This is illustrated in Fig. 6, which shows the transfer characteristic of a 3-bit DAC that has a useful resolution of 2 bits.

Due to manufacturing tolerances a proportion of n-bit converters will have only n - 1 or n - 2 bit useful resolution. In applications not requiring n - bit useful resolution these reduced resoution versions offer a significant price advantage. The useful resolution of Plessey DACs is guaranteed over their full operating temperature range.

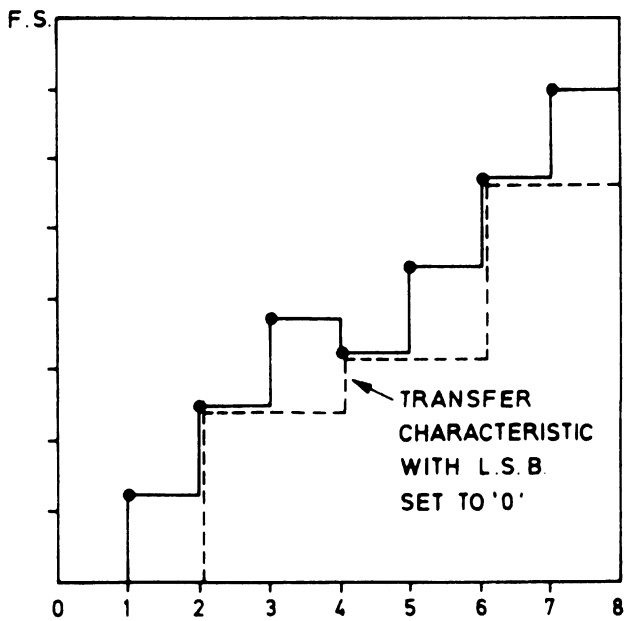


Fig. 6 Non-monotonic 3-bit DAC with a useful resolution of 2 bits

1.3.10 Settling time

Settling time is the time taken after a transition of the input code for the output of a DAC to settle to within ± ½LSB of its final value. This varies depending on which bits are being changed. It may be specified for a change of 1LSB which generally gives the most optimistic (fastest) figure. More conservative figures are given by the most major transition (where the MSB changes in one direction and all other bits change in the opposite direction, e.g. 01111111 to 10000000 or vice versa) or by a change from all bits off to all bits on (00000000 to 11111111) or vice versa.

1.4 Bipolar operation

The discussion so far has been concerned only with DACs producing a single polarity (usually positive) output voltage. In some applications a bipolar (both positive and negative) output range may be required.

This can be achieved by adding a negative offset of $\frac{V_{REF}}{2}$ to the analogue output, as shown in Fig. 7. For all input codes where the MSB is '0' the output voltage is then negative, and for output codes where the MSB is '1' the output voltage is positive. Where the input coding is normally binary but the output voltage is offset by $\frac{-V_{REF}}{2}$ then the input code is referred to as offset binary.

The transfer function of a 3-bit DAC with offset binary coding is shown in Fig. 8.

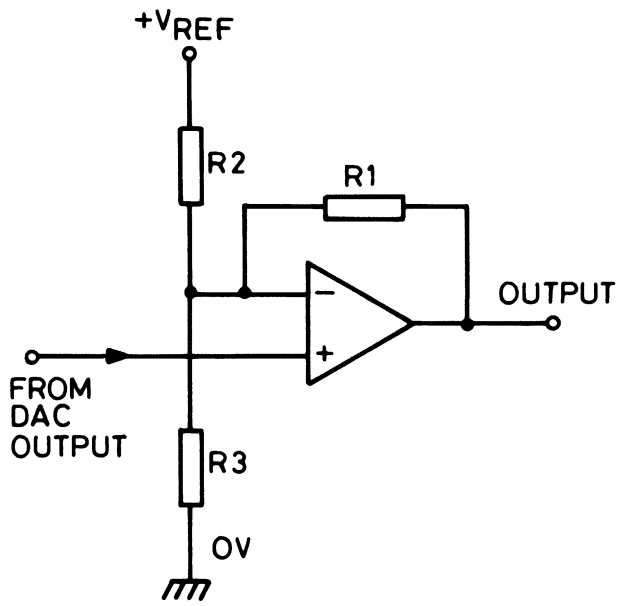


Fig. 7 Bipolar operation of a DAC

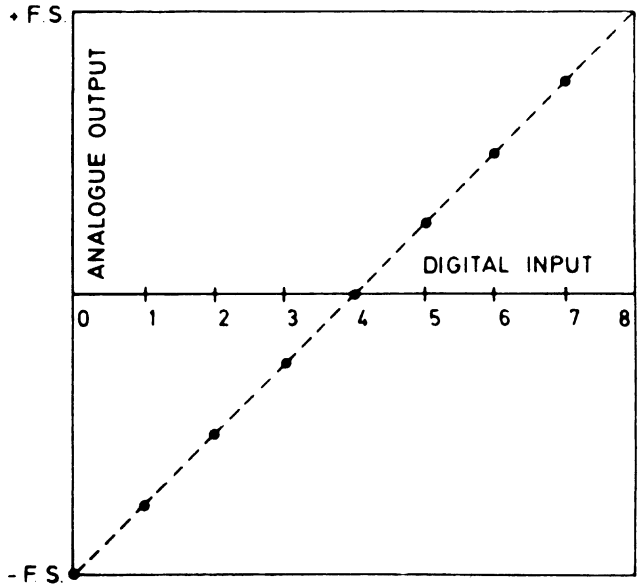


Fig. 8 Bipolar operation of a 3-bit DAC

Analogue to Digital Converters

2. An analogue to digital converter (ADC) is a device which converts an analogue input into a corresponding digital output code.

2.1 Ideal output characteristics

Assuming a unipolar input voltage and binary coded output the transfer function of an ideal n-bit ADC is given by:

$$V_{FS} \quad (B_1.2^{-1} + B_2.2^{-2} + ... + B_n.2^{-n}) = V_{in} \pm \tfrac{1}{2}LSB.$$

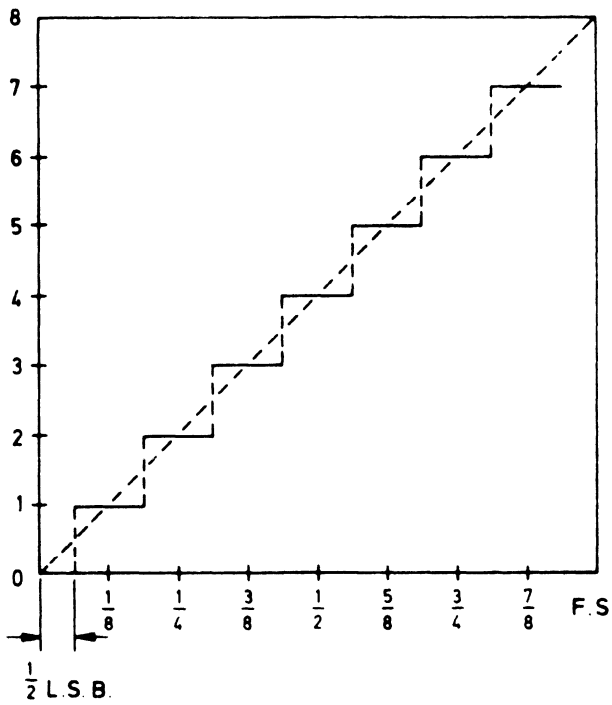


Fig. 9 Ideal 3-bit ADC transfer characteristic

The transfer function of an ideal 3-bit ADC is shown in Fig. 9. In this case there are 8 digital output codes corresponding to the 8 input codes of a DAC. However, unlike the analogue output of a DAC, the analogue input of an ADC can vary continuously, which means that each digital output code, with the exception of 0 and 7, exists over an analogue increment of 1LSB. The zero of an ADC is usually trimmed so that the transitions between codes occur $\pm$ ½LSB on either side of the nominal analogue input for a particular code. For example, the nominal input for output code 2 is ¼ V_{FS}. The transition from 1 to 2 occurs at $\frac{3}{16}$ V_{FS} and the transition from 2 to 3 occurs at $\frac{5}{16}$ V_{FS}.

As with a DAC, an 'ideal' straight line may be drawn through the transfer characteristic of an ADC.

2.2 Practical A-D conversion methods

There are many methods of performing an analogue to digital conversion; all of these methods are used in the current range of Plessey A-D converters.

2.2.1 Parallel (flash) conversion

In an n-bit parallel converter (Fig. 10) a resistor ladder is used to generate $2^n - 1$ voltage levels from 1LSB to $(2^n - 1) \times$ LSB which are fed to the reference inputs of $2^n - 1$ voltage comparators. The analogue input signal is fed to the second input of each comparator, and is thus compared simultaneously with each of the $2^n - 1$ voltage levels. At the point in the comparator chain where the reference voltage exceeds the input voltage the comparator outputs will change over from low to high. The comparator outputs are encoded into whatever digital output coding is required.

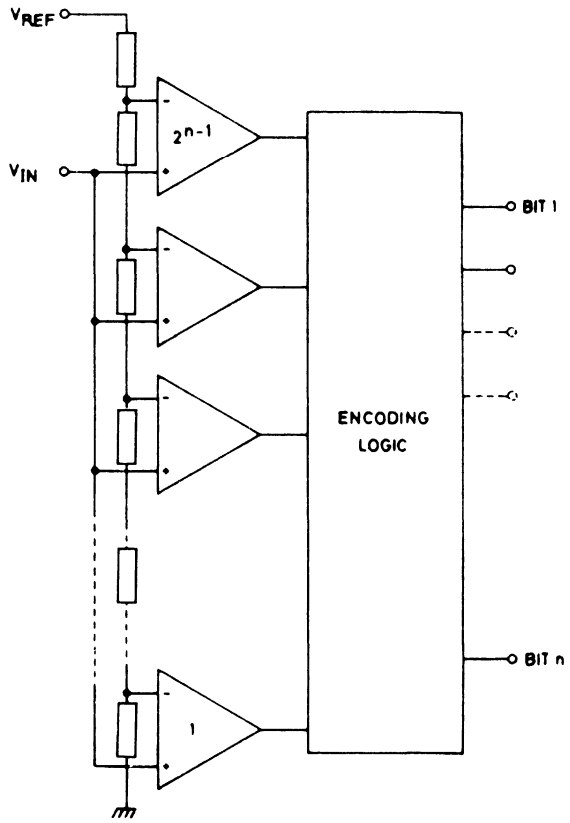


Fig. 10 Parallel A-D converter

Since the only delays involved in the conversion are the propagation delay of one comparator plus the logic propagation delays, parallel converters are very fast and may perform in excess of 10 million conversions per second. However, due to the large number of comparators required (63 for a 6-bit converter, 255 for an 8-bit converter) they are expensive to produce. Applications include digital video systems, digital storage oscilloscopes and radar data processing.

2.2.2 Staircase and comparator

In this type of ADC the input code of a DAC is incremented by a binary counter to give a staircase waveform, as shown in Fig. 11. This is compared with the analogue input and when the staircase exceeds the analogue voltage the comparator output changes state and stops the clock. The count reached by the binary counter is thus the ADC output code. This method of A-D conversion is relatively simple and cheap, but is also relatively slow, requiring $2^n - 1$ clock pulses for a full-scale conversion, where n is the number of bits. This conversion method is used in the ZN425 series of dual-purpose D-A/A-D converters.

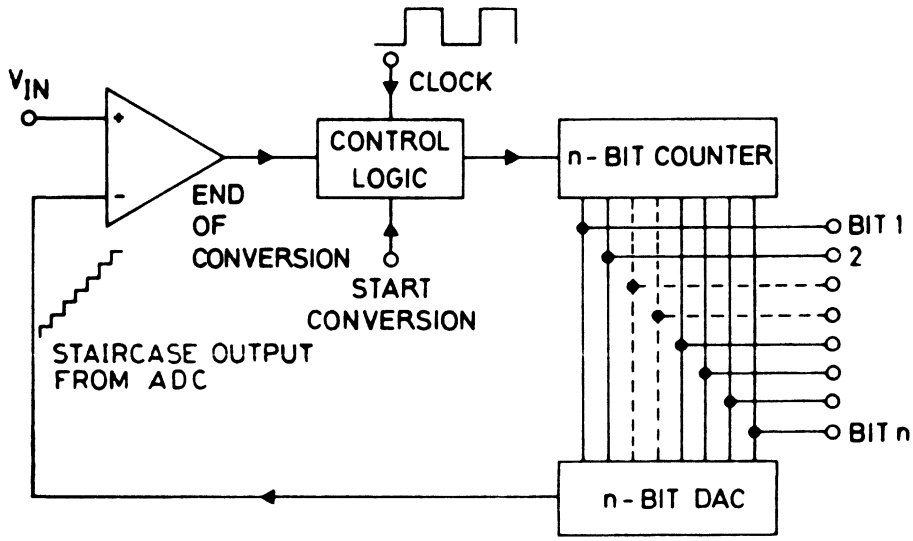


Fig. 11 Staircase (ramp) and compare ADC

2.2.3 Tracking converters

As its name implies, a tracking converter can follow changing analogue inputs. The principle operation is similar to that of the staircase and compare type of converter, but it uses an up/down counter and a window comparator, as shown in Fig. 12. When the DAC output is less than the analogue input the comparator instructs the counter to count up and the DAC output thus increases. If the DAC output is greater than the analogue input the comparator causes the counter to count down, thus decreasing the DAC output. When the DAC output is equal to the analogue input ± ½LSB, the input is within the 'window' of the comparator and the counter is stopped. This is illustrated in Fig. 13. A tracking converter has speed advantages over a staircase and compare type, since the counter of the latter type can only count up, and must therefore be reset between conversions. In the case of a tracking converter, once it has performed an initial conversion starting from zero, any subsequent conversions require only that number of clock pulses necessary to track any increase or decrease in input voltage.

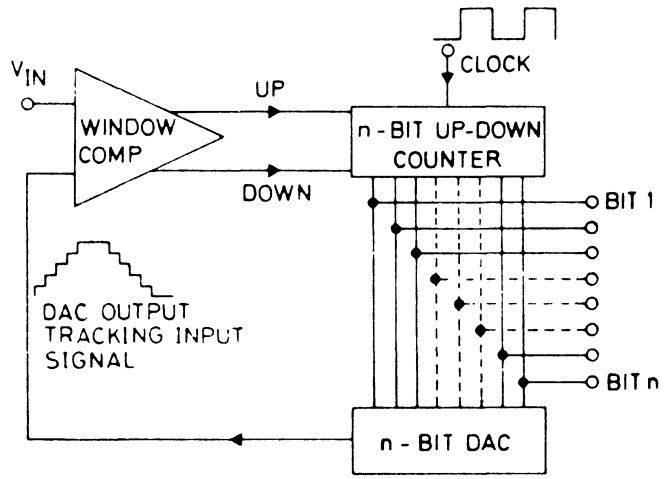


Fig. 12 Tracking ADC

As an extreme example consider an analogue input that changes from V_{FSO} to (V_{FSO} − 1LSB). The staircase and compare converter will require $2^n - 1$ clock pulses for the first conversion and $2^n - 2$ clock pulses for the second conversion. The tracking converter on the other hand, will require $2^n - 1$ clock pulses for the first conversion but only one clock pulse for the second conversion. This is illustrated in Fig. 14.

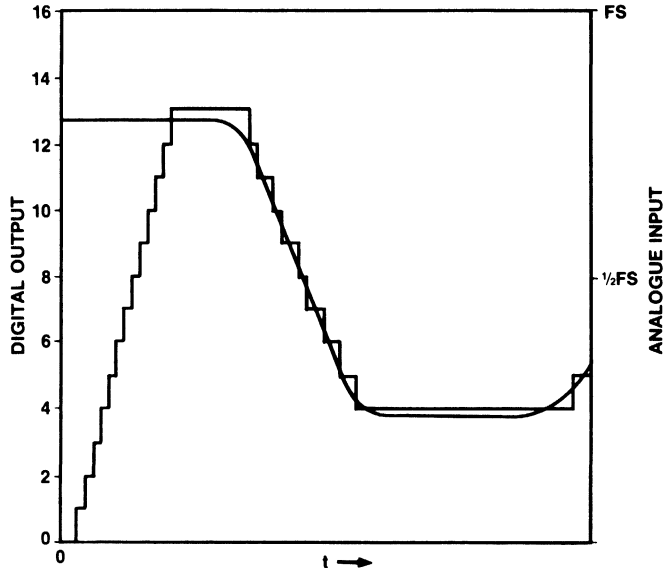


Fig.13 Operation of tracking ADC

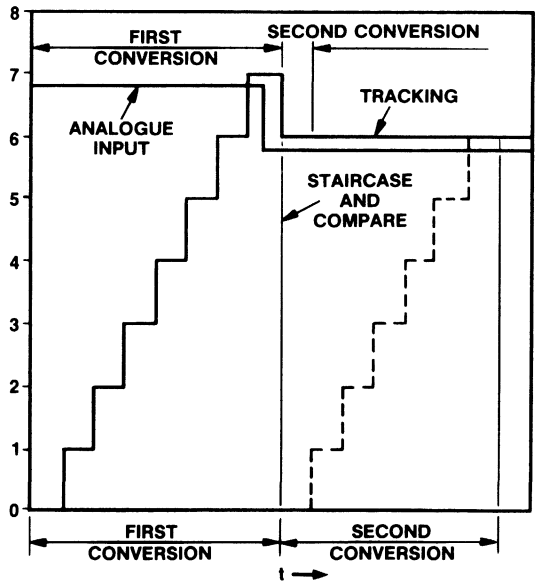


Fig.14 Comparison of ramp and compare and tracking ADC

In general it can be said that a tracking converter will follow signals whose rate of change is less than $\pm$ 1LSB $\times$ clock frequency. If this condition is met there is no need to use a sample-and-hold circuit on the analogue input.

A tracking technique is used in the ZN433 series of converters.

2.2.4 Successive approximation converters

The operation of a staircase and compare ADC is analogous to weighing, say an 11 gramme weight, on a balance by adding one gramme weights until the scale tips, which is clearly a very slow method. A faster procedure, known as successive approximation, uses weights of 16, 8, 4 2 and 1 grammes. The 16 gramme weight is tried first and is discarded because it tips the scale. The 8 gramme weight is tried next, and is left on the pan. Next the 4 gramme weight is tried and discarded, and the 2 and 1 gramme weights are tried and retained. The final result is the sum of the weights remaining on the scale pan, and the operation has taken 5 'cycles' as opposed to 11 'cycles' for the staircase and compare method.

The principle of a successive approximation ADC is identical. The MSB of a DAC is first set to '1' and the output is compared to the analogue input. If it is greater than the input the MSB is reset to '0', otherwise it is left at '1'. The next bit is then set to '1' and the DAC output is again compared to the analogue input. Again it is either reset or left at '1' depending on the result of the comparison. This procedure is repeated for every bit down to the LSB, and the final code to the DAC is the output code of the ADC. A successive approximation cycle is illustrated in Fig. 15.

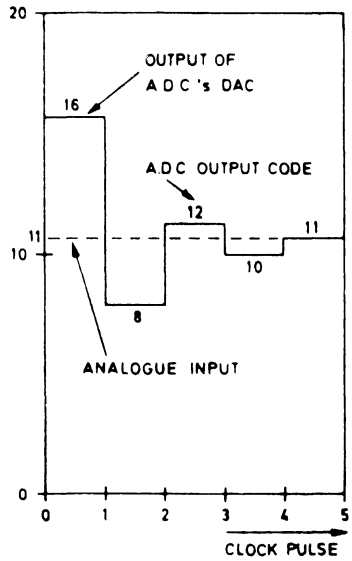


Fig. 15 Operation of a successive approximation ADC

The successive approximation technique is used in most of the Plessey data converters that operate below video speeds.

2.2.5 Dual-slope converters

Dual-slope integration is one of the slowest methods of A-D conversion, but it offers high resolution at a modest cost.

A block diagram of a dual-slope converter is shown in Fig. 16. It operates in the following manner: Switch S1 is closed by the control logic, S4 is opened and the input voltage is integrated for n clock periods, where n is usually the maximum count of the counter. At the end of this time the integrator output voltage, V_O, is $\frac{-V_{in}\, n\, T_c}{RC}$ where T_c is the clock period. This is shown in Fig. 17.

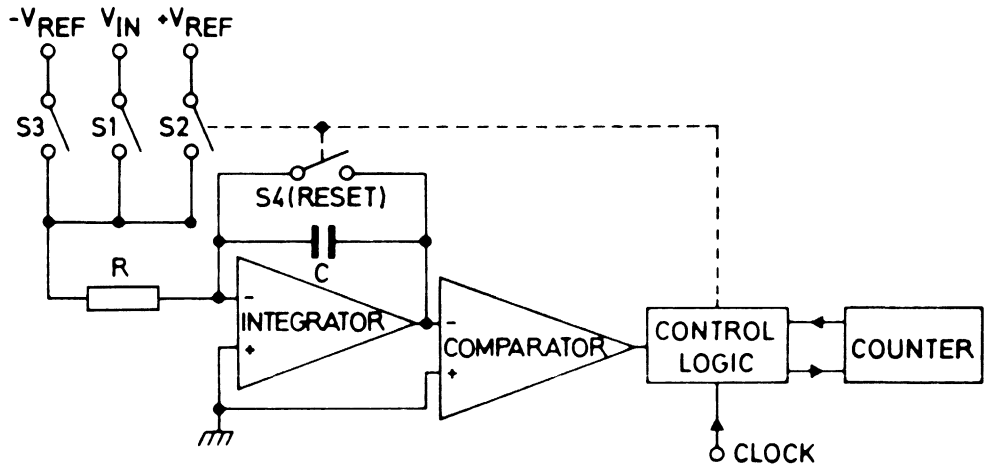


Fig. 16 Dual-slope ADC

During this period the polarity of the input signal is detected by the comparator. At the end of the integration period S1 is opened and, depending on the polarity of V_{in}, either S2 or S3 is closed to connect the integrator to a reference voltage of opposite polarity to V_{in}. The counter is now allowed to count from zero until the integrator output reaches 0V, when the comparator output changes state and the counter is stopped. Since the integration is over the same voltage range (V_O), $V_O = \frac{-V_{REF}\ X\ T_c}{RC}$, where X is the count reached by the time the integrator output

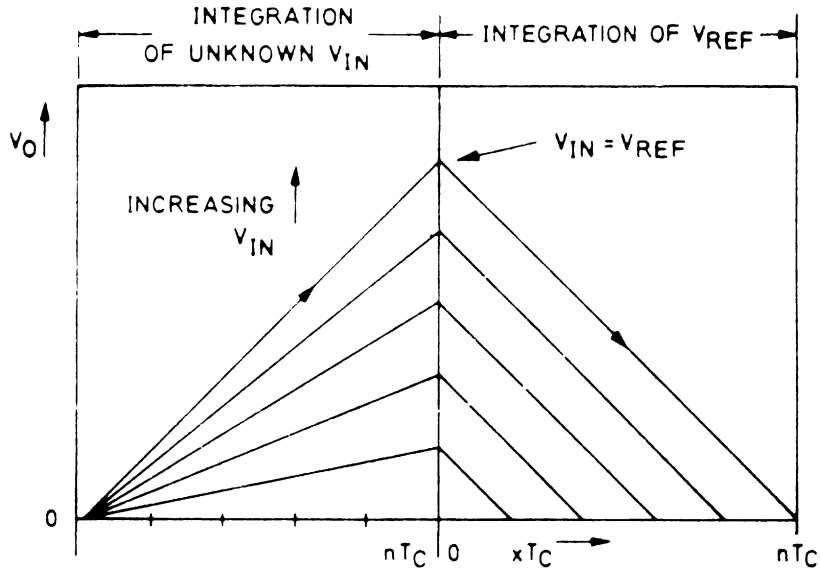


Fig. 17 Operation of dual-slope ADC

crosses zero. Thus

$$\frac{V_{in.}\ n\ T_c}{RC} = \frac{V_{REF}\ X\ T_c}{RC}$$

$$\text{or } X = \frac{V_{in.}\ n}{V_{REF}}$$

Since n and V_{REF} are both fixed the output count is proportional to the input voltage. Since both the first and second integrations occur under identical conditions the converter is unaffected by any long term variations in T_c, R or C, as demonstrated by the disappearance of these terms from the final equation. The only factors affecting the accuracy of the converter are (1) the stability of V_{REF} (2) the stability of the 'on' resistance of S1 to S3 and (3) drift in the integrator and comparator op-amps. These affects can be minimised by careful design.

Dual-slope converters are generally used where high resolution and low cost are more important than speed, for example in digital voltmeters.

The ZNA216 is a DVM logic sub-system containing the clock, counter and all control logic necessary for dual-slope converter or DVM.

2.3 A-D parameters and definitions

2.3.1. A-D converter errors

Like DACs, practical ADCs are subject to a number of error sources, and since most ADCs contain a reference DAC, many of these error sources are the same for both types of converter.

2.3.2 Quantising error (uncertainty)

Quantising error is an ADC specification that has no counterpart in DAC specifications. For each input code of a DAC there is a unique analogue output level, but for any ADC output code there is a 1LSB range of analogue input levels. It is thus not possible to tell from the output code the precise value of the analogue level, there being a quantising error or uncertainty of ± ½LSB. Since all ADCs have this inherent quantising error the parameter is frequently not quoted in specifications.

2.3.3 Missing codes

Missing codes are perhaps best explained by considering the operation of a staircase and compare type 3-bit ADC which has a non-monotonic DAC, as shown in Fig. 18. The reference DAC exhibits non-monotonicity at input code 4, i.e. step 4 of the staircase decreases. There is thus no way in which the counter can be stopped at this code. If the analogue input is less than the DAC output for code 3 then the comparator will stop the counter before 4 is reached. If the analogue input is greater than output 3 it must also be greater than output 4, so the comparator will not change state at code 4.

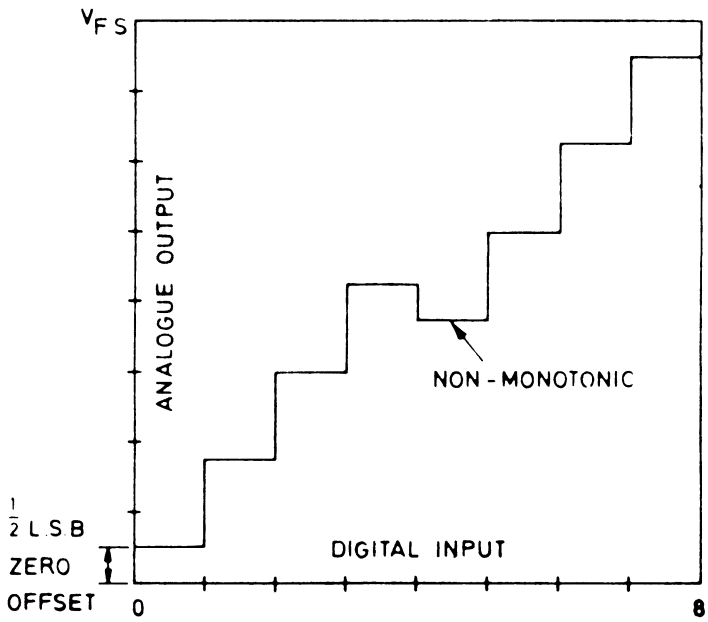


Fig. 18 Non-monotonic DAC used in an ADC

Output code 4 will thus never appear and is known as a 'missing' code. The transfer function of an ADC with a missing code is shown in Fig. 19.

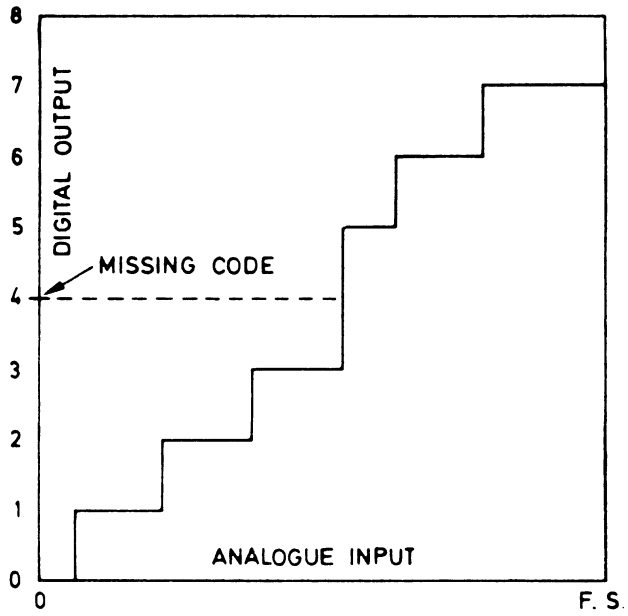


Fig. 19 ADC with missing code

2.3.4 Zero transition

As explained earlier, the zero of an ADC is usually trimmed so that the output transition from 0 to 1 occurs at an input level corresponding to ½LSB, i.e. $\frac{1}{2}\frac{V_{FS}}{2^n}$. However, as supplied the reference DAC of an ADC I.C. will not have the ½LSB offset necessary to achieve this. The zero transition will thus occur at 1LSB plus the DAC zero error, plus the comparator offset voltage. These three parameters are frequently lumped together as the (untrimmed) zero transition of the ADC.

2.3.5 Gain error

This is the difference between the slope of a line drawn between the actual zero and full-scale transition points and that of a line drawn through the ideal transition points.

2.3.6 Non-linearity (linearity error)

Non-linearity is the maximum amount by which any actual transition points deviates from the corresponding ideal transition point. It is specified as a percentage of full-scale or a fraction of an LSB. A linearity error of less than ± ½LBS assures no missing codes.

2.3.7 Differential non-linearity

This is the maximum difference between any 1LSB increment of the analogue input and the ideal size of an LSB increment $\frac{V_{FS}}{2^n}$. Differential non-linearity of less than 1LSB guarantees no missing codes.

2.3.8 Resolution

The resolution of an ADC is simply the number of bit outputs that the converter possesses. As with a DAC, resolution implies nothing about the accuracy of a device.

2.3.9 Useful resolution

Useful resolution is the resolution (number of bits) at which an ADC has no missing codes, which for Ferranti ADCs is guaranteed over the operating temperature range. As with DACs, an n-bit ADC may have a useful resolution less than n bits, for reasons previously explained.

2.3.10 Conversion time

The time taken for an ADC to perform a complete conversion is known as the conversion time. For successive approximation converters conversion time is fixed by the number of bits and the clock frequency. However, for other types, conversion time may vary with input voltage. For example, a ramp and compare ADC requires $2^n - 1$ clock pulses for a full-scale conversion but only one clock pulse for a one bit conversion. It is thus important to check exactly what is being specified.

2.4 Bipolar operation

As with a DAC, an ADC may be used for bipolar operation. Taking the ZN427 as an example the input is offset by $\frac{+V_{REF}}{2}$ so that the input voltage presented to the ADC is always positive, even with negative input voltages down to $\frac{-V_{REF}}{2}$. The principle of offsetting an ADC input is illustrated in Fig. 20, whilst the transfer function of a 3-bit bipolar ADC is shown in Fig. 21. In this case the **output** coding is known as offset binary.

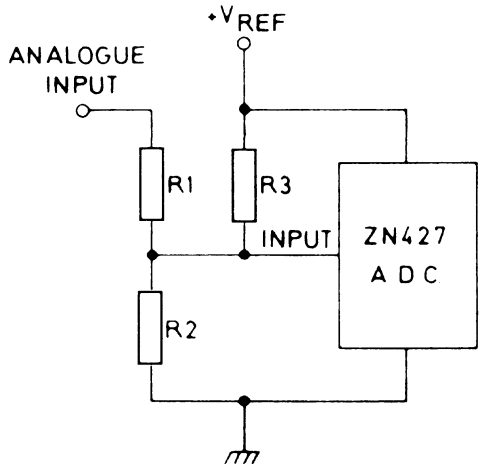


Fig. 20 Bipolar operation of an ADC

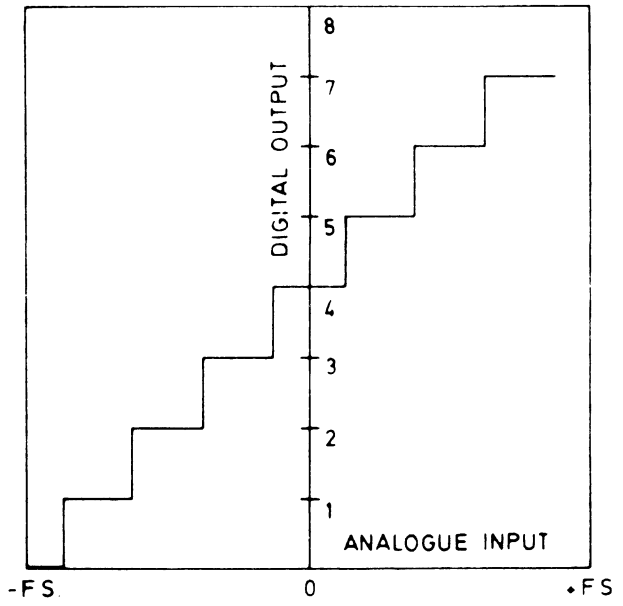


Fig. 21 Bipolar transfer characteristics of an ADC

AP9007 Video ADC Evaluation Board AN52

The Plessey AP9007 evaluation board provides an easy to use demonstration system for the SP94308, 8-bit ADC. The flexibility of the evaluation board allows the SP94308 to be optimised for many different applications, with little effort. The board contains circuitry for generating reference voltages, separating the sync and buffering the clock.

BOARD FEATURES

- 8-Bit 18 MSPS
- On-Board Sync Separator
- On-Board Voltage Reference
- Buffered Clock Output
- Adjustable Reference Chain Voltages
- Adjustable Clamp Level
- TTL or ECL Level Clock Input
- TTL Level Outputs

INPUT CONDITIONS

- +5V and -5.2V Power Supplies
- TTL or ECL Clock (AC Coupled On Board)
- Active Low Clamp Pulse (see Sync Separator)

APPLICATIONS

- Evaluation of the SP94308 A/D Converter
- System Prototyping Aid
- Test Fixture

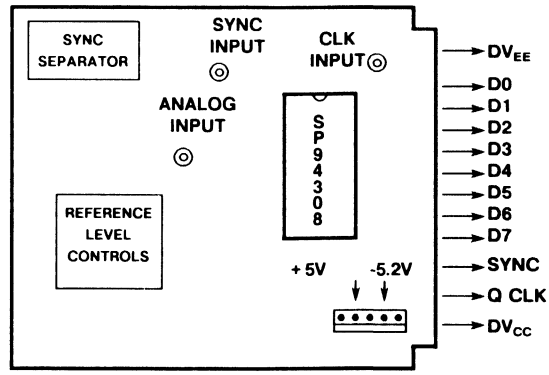


Fig.1 AP9007 simplified board layout

SP94308 FEATURES

High Accuracy

An accuracy of $\pm\frac{3}{4}$ LSB to 8 bits enables high quality TV pictures to be digitised without noticeable contouring.

High Speed

The high sampling rate of the device facilitates digitisation of wide bandwidth video. Clocking at high speeds (4x colour subcarrier) also permits easier anti-aliasing filtering, when required.

High Analog Bandwidth

Wide band video can be digitised with no loss of picture information.

No Sample and Hold Required

The low aperture jitter and low hold time of the device allow high frequency analog signals to be digitised, without the need of an external sample and hold circuit.

Internal Clock Buffer

A low level AC coupled signal can be used to clock the device therefore minimising clock breakthrough to other parts of the circuit.

Internal Sync Clamp

Unlike other video ADCs, the SP94308 accepts AC coupled video signals directly. There is no need for a preceding black level clamp circuit.

Internal Output Latch

An output latch ensures that the data is available for 90% or more of the clock cycle, therefore no external latching is required.

INTRODUCTION

A block diagram of the SP94308 is shown in Fig.2. The design of the SP94308 incorporates many of the external support components required by conventional ADCs, when used in video applications. To demonstrate the versatility of the SP94308, two evaluation boards are available.

The AP9007 board described in this application note is designed to allow the device to be interfaced into almost any video system. With this board a wide range of input options are available by merely changing link positions or altering potentiometers. An on-board sync separator is avalable should an external sync pulse by unobtainable. All outputs, buffered clock and sync signals are available at the edge connector.

GENERAL INFORMATION

The AP9007 evaluation board is designed to demonstrate the flexibility and the many features of the SP94308 Video ADC. The external components and adjustments on this application board allow the device to be interfaced into almost any video system with minimal effort. It also allows experiments to be performed for interfacing with the more unusual systems.

Unlike most video ADCs, especially subranging systems, the SP94308 does not require any preceding sample and hold circuit or buffer amplifier.

To use the full applications board simply connect the supplies to $\pm$5V and apply a standard 1V p-p video signal to the input. Any 15MHz oscillator can be used to clock the device. The level of the clock input should be set to 0.8V p-p (ECL can be used directly, one link change for TTL). The board has been prealigned and will produce a TTL/CMOS digitised output of the active video and sync information. The evaluation board requires no DC clamping, video buffer, sample and hold, sync pulse, clock buffer or output latch.

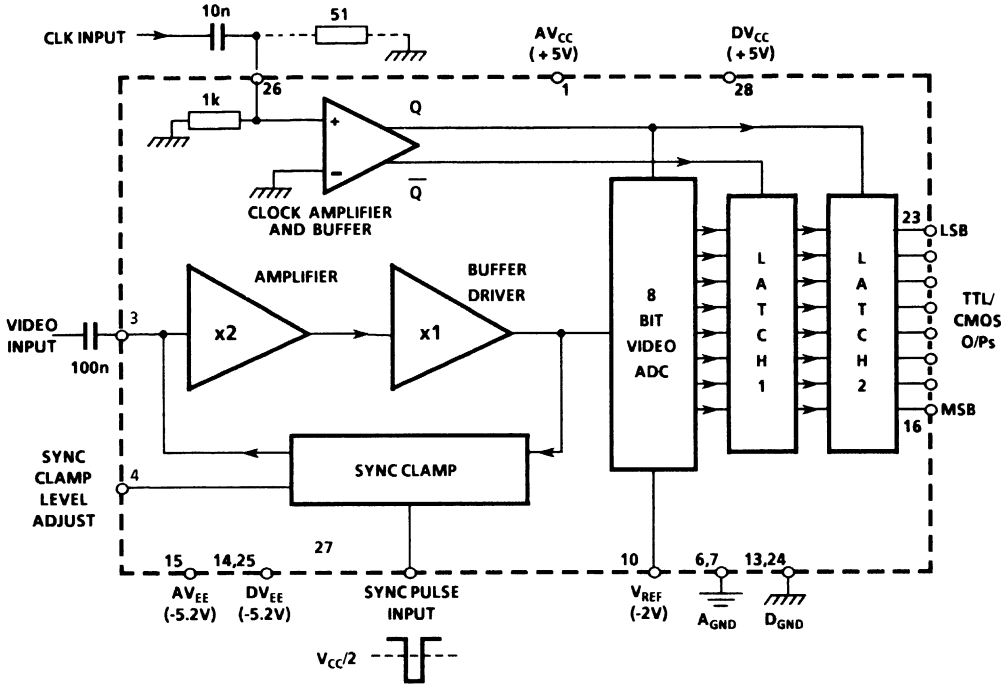


Fig.2 Block diagram of SP94308

Board Supplies

The board is powered from ±5V. The +5V supply requires 70mA and the -5V supply requires 150mA. These are typical figures. All supplies are fed via the power supply connector to the edge connector.

The Clock Signal (Low Level)

The board is designed to cope with a wide range of clock inputs. The SP94308 includes an internal clock amplifier which enables the clock to be driven from low level AC coupled signals. As the signals are Ac coupled either sine or square waves can be used. The board is configured for 800mV p-p clock inputs at frequencies from 10MHz to 20MHz.

A transistor has been included to buffer the clock signal to the edge connector. This also provides some reverse isolation from reflections or loads on the clock lines etc.

TTL Clock

Link L4 has been provided to enable direct connection of TTL CLOCK to the board (see Table 2). With this link positioned for TTL, 0.2 of the TTL amplitude will be AC coupled and fed to the device.

Analog Input

This should be a conventional 1V p-p syncs down composite video signal and can be either NTSC, PAL or SECAM. Please note that if the board is reconfigured for clamping with a burst gate pulse then, for optimum performance the burst should be removed from the analog input.

With any high analog bandwidth ADC, analog inputs that are above the NYQUIST frequency (½fc) will be reflected by the clock (aliases) into the normal signal bandwidth. The patterning caused by this can be removed from the picture by providing an adequate anti-aliasing filter before the ADC input.

On-Board Clamp Gate

The SP94308 contains an input clamp circuit. This enables the video input to be AC coupled and allows automatic DC alignment of the video within the ADC.

One mode of operation is to clamp on the sync tips of the input video. This requires a clamp gate pulse which is coincidental with the sync tip. The pulse can be generated by the on board sync separator circuitry (see Fig.5 in the data sheet).

External Clamp Gate

Link L2 provides external clamp gate operation and R13 terminates the clamp gate pulse. The clamp gate input should be normally high, switching down below the device clamp gate input threshold of Vcc/2 during the selected clamp time. See the data sheet for details and information regarding burst gate/black level clamping.

Reference Voltages

The Plessey TAB1042 is a Quad Operational Amplifier. It is used with a voltage reference to provide full adjustment of all the device reference chain voltages. Please note that this would not be required in a practical minimum component

solution as fixed resistors, potentiometers or zener diodes could be used.

The 10 turn potentiometers RV1 and RV3 allow both the top and bottom of the reference chain to be adjusted. Link L1 allows the REF + ve to be connected to GND.

The preset RV3 is prealigned for -2V. It can, however, be adjusted to suit different levels of input. Also it can be used to reduce the reference chain voltage for applications that require digitisation of the video without digitising the sync.

Clamp Level Adjust

Link L3 is provided to allow the device to be programmed for sync level clamping or black level clamping. When open circuit this pin will automatically self bias (-1.4V) for applications that require black level clamping. If pin 4 is connected to REF -ve then the device will be configured for applications using sync level clamping.

Link L3 also allows pin 4 of the device to be adjusted using preset RV2. This preset effectively moves the video across the reference resistor chain and can be used to align the device for various digital video standards. See link position, Table 2.

Digitisation of Active Video Only

Pin 4 of the SP94308 can be programmed for different DC offsets on the input video. This can be used in applications that require digitisation of the active video only. RV3 can be adjusted to reduce the reference voltage, effectively increasing the gain of the device. This allows digitisation of the active video from a standard 1V p-p input. For this applications, RV2 should be adjusted so that the video black level corresponds to the all zeros code.

Linearity Adjust

This adjustment is again for experimental purposes only and can be replaced with an external resistor as shown in the data sheet, Fig.3. The effect of this adjustment is to fine tune the differential linearity at 15 critical codes. This adjustment is best performed with a video ramp input applied to the board while the reconstructed output is viewed on an oscilloscope.

TOP VIEW
OF UNDERSIDE PINS

ALL TOP PINS = GND

Pin No.	Function
1	NC
2	NC
3	NC
4	NC
5	NC
6	NC
7	NC
8	-5.2V
9	-5.2V
10	A0 LSB
11	A1
12	A2
13	A3
14	A4
15	A5
16	A6
17	A7 MSB
18	NC
19	NC
20	NC
21	NC
22	SYNC OUT
23	NC
24	NC
25	Q CLOCK
26	NC
27	+5V
28	NC
29	NC
30	NC

Table 1 Edge connections

NOTE: Q CLOCK: This is a buffered version of the clock input, with a 0.7V drop due to the emitter follower.

Name	Position	Description
L1	Next to pin 1 on SP94308 made	This link determines whether the REF +ve pin (pin 2) is held to GND or variable. If then REF +ve is tied to GND If then the REF +ve adjust pot is active
L2	Just right of the sync input	This link selects the internal/external sync option. If the external sync must be provided If the internal sync separator is selected.
L3	Left of pins 5,6 on SP94308	This link selects the voltage on the sync level adjust input (pin 4) If sync level adjust = REF -ve, -2V (Sync level clamping) If sync level adjust is variable by the Sync pot If sync level adjust is open circuit (black level clamping)
L4	Right of SP94308	This link selects full clock or attenuated clock input If full amplitude clock signal goes to device If 0.2 x clock signal amplitude goes to device
L5	Left of pins 12,13 on SP94308	This link when open circuit leaves pin 18 (-250mV adjust) open circuit but decoupled. If the link is present then the Lin Adj pot is operational.

Table 2 Link positions

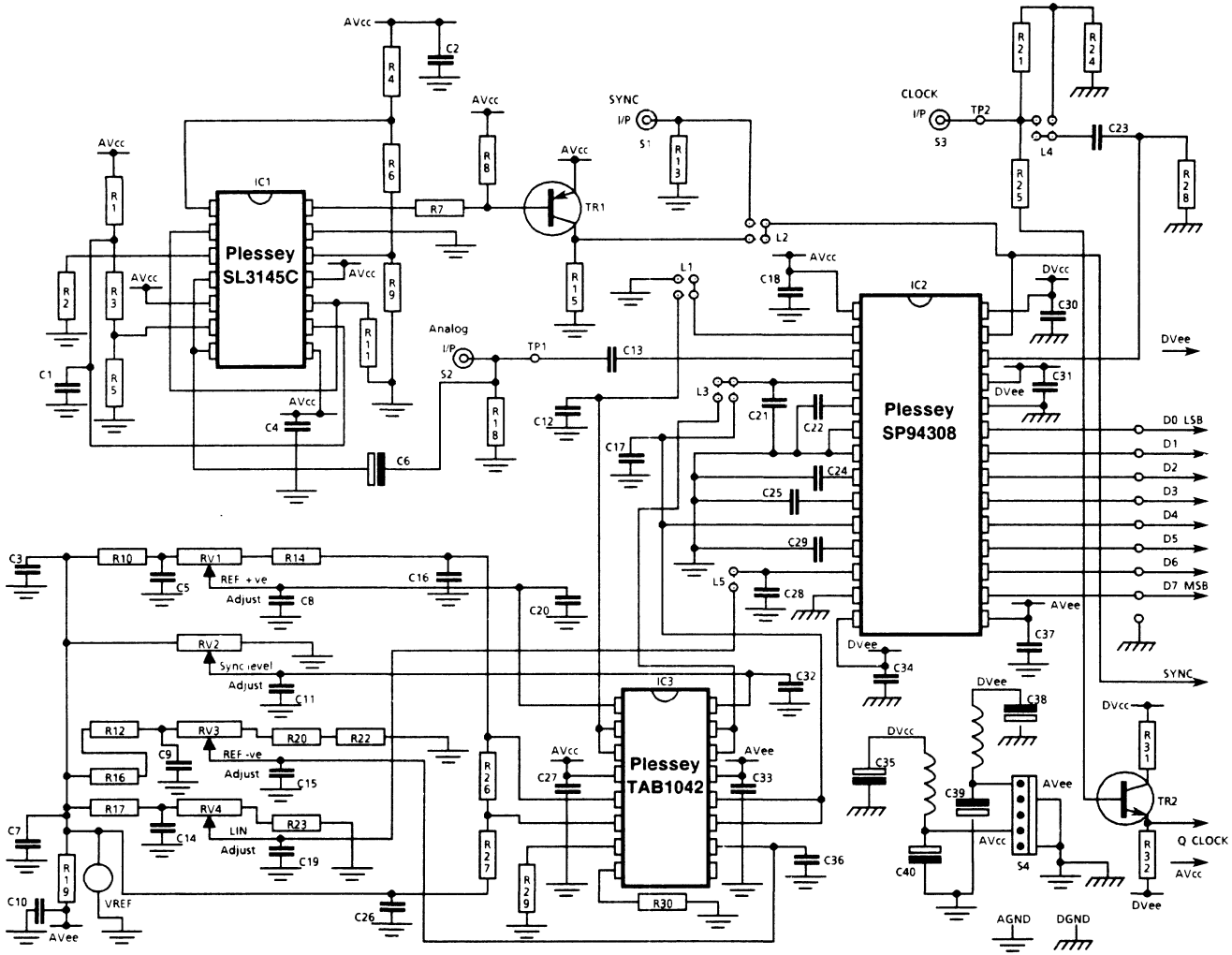


Fig.3 SP94308 test/evaluation board

RESISTORS			
R1	10k	R17	1kΩ
R2	560Ω	R18	75Ω 1/8W
R3	390Ω	R19	330Ω
R4	10k	R20	1.2k
R5	10k	R21	39Ω
R6	10k	R22	47Ω
R7	2.2k	R23	39Ω
R8	560Ω	R24	10Ω
R9	10k	R25	10Ω
R10	10k	R26	1k
R11	1k	R27	1k
R12	220Ω	R28	1k
R13	47Ω 1/8W	R29	1k
R14	10k	R30	220k
R15	2.2k	R31	100Ω
R16	33Ω	R32	270Ω
CAPACITORS			
C1	1μF	C21	100nF
C2	10nF	C22	27pF
C3	10nF	C23	100nF
C4	10nF	C24	100nF
C5	10nF	C25	100nF
C6	47μF (Electrolytic)	C26	10nF
C7	10nF	C27	10nF
C8	10nF	C28	100nF
C9	10nF	C29	100nF
C10	10nF	C30	10nF
C11	10nF	C31	10nF
C12	10nF	C32	10nF
C13	100nF	C33	10nF
C14	10nF	C34	10nF
C15	10nF	C35	47μF (Electrolytic)
C16	10nF	C36	10nF
C17	0.47μF	C37	10nF
C18	10nF	C38	47μF (Electrolytic)
C19	10nF	C39	47μF (Electrolytic)
C20	10nF	C40	47μF (Electrolytic)
POTENTIOMETERS			
RV1	1k (Multiturn Cermet)	RV3	1k (Multiturn Cermet)
RV2	1k (Multiturn Cermet)	RV4	100Ω (Multiturn Cermet)
SEMICONDUCTORS			
IC1	SL3145C	TR1	2N3906
IC2	SP94308	TR2	2N3904
IC3	TAB1042	V_{REF}	ZNREF025
MISCELLANEOUS			
S1 - S3	Sub-Vis Sockets	5 off	Micro Shunts
S4	KK Molex Socket	4 off	Rubber Feet
L1 - L4	4-way Unshrouded Header	11 off	Veropins
L5	2-way Unshrouded Header		

Table 3 Component list for SP94308 test/evaluation board

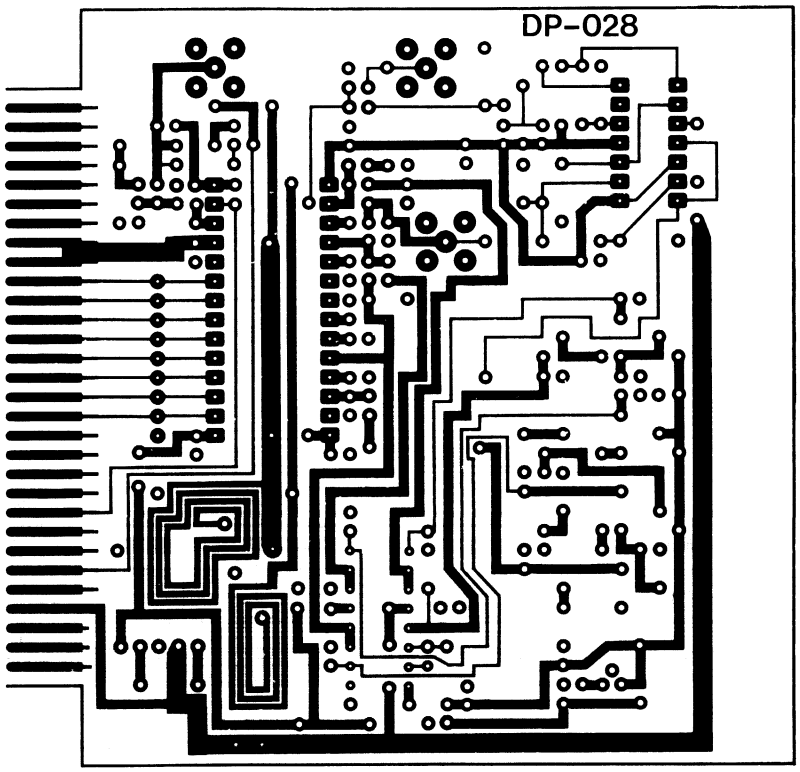


Fig.4(a) AP9007 PCB copper track (1:1)

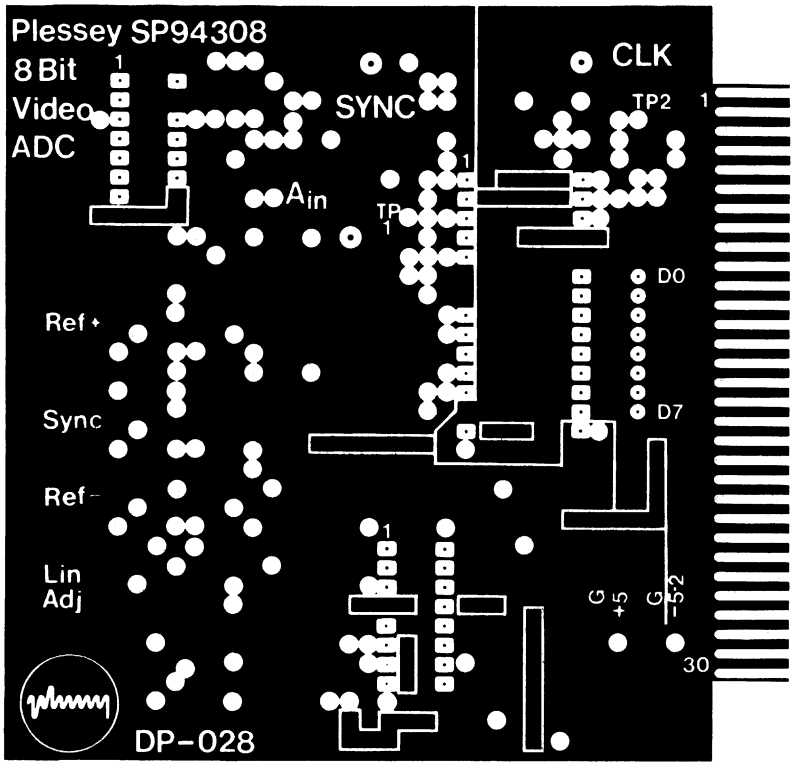


Fig.4(b) AP9007 PCB ground plane and component side (1:1)

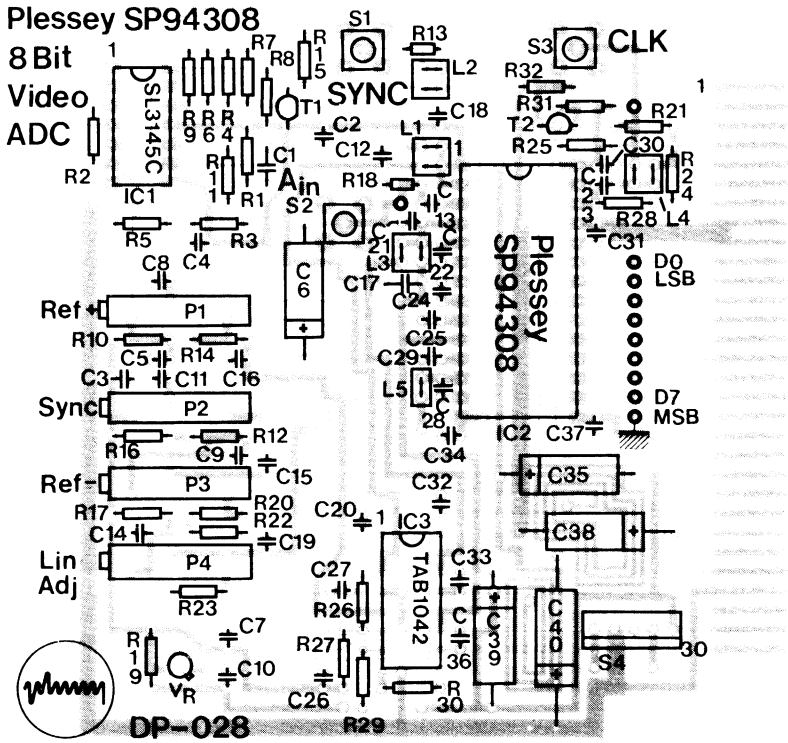


Fig.4(c) AP9007 component layout (1:1)

AP9008 Low Cost Video ADC Evaluation Board AN57

The Plessey AP9008 evaluation board provides a practical, low cost, video application circuit for the SP94308, 8-bit ADC. The features included within the SP94308 reduce the number of external support circuits and components required to produce a complete ADC system.

The AP9008 minimum component application board is designed to demonstrate the flexibility of the SP94308, whilst maintaining a low component count. Although the board can be used in a standalone manner, in a real system a number of components can be omitted e.g. termination resistors, power supply decoupling capacitors etc.

The SP94308 is designed to eliminate the need for the sample and hold circuit and buffer amplifier usually required by video ADC systems.

BOARD FEATURES

- 8-Bit 18 MSPS
- Low Component Count
- Sync and Clock available at Edge Connector
- Only one External Reference Required
- Optional Clamp Level Input
- ECL Level Clock Input
- TTL Level Outputs

INPUT CONDITIONS

- +5V and -5.2V Power Supplies
- Clock Input 800mV p-p, AC Coupled On Board
- Active Low Clamp Pulse (see Data Sheet)
- Negative Reference Voltage (normally -2V)
- Clamp Level Input (Optional)

APPLICATIONS

- Evaluation of the SP94308 A/D Converter
- System Prototyping Aid
- Test Fixture

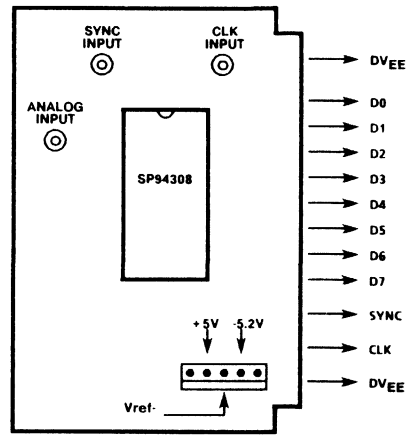


Fig.1 AP9008 simplified board layout

APPLICATION INFORMATION

Power Supplies

Power supplies for the board are fed via the Molex connector S4. The voltages and currents required are, +5V at 40mA and -5.2V at 110mA. A negative reference voltage is required by the device and this can be applied to the middle pin of the power supply connector. This reference takes approximately 6mA at -2V.

Both the +5V and -5.2V power rails are available at the edge connector, pins 27 and 8 to 9 respectively.

Clock Input

Clock input is via the SMC socket S3 and is brought out to the edge connector pin 25. The device is designed to accept low level clock signals. This reduces the possibility of clock pick-up by other parts of the TV or system. On-board AC coupling removes any DC offset. This allows the device to be driven from ECL levels or any 50Ω generator that can produce up to 800mV.

The board can be driven from sine or square wave signals. However, if sine waves are used the maximum recommended amplitude signal is 800mV. This produces the fastest edge speeds at the clock input and will reduce aperture uncertainty caused by clock noise or jitter.

Analog Input

The analog input is fed to the board via SMC socket S1 and is terminated by a 75Ω resistor (video standard termination).

The SP94308 can accept a conventional 1V p-p syncs down composite video signal which can be either NTSC, PAL or SECAM. Note that if the board is reconfigured for clamping with a burst gate pulse then, for optimum performance, the burst should be removed from the analog input. For applications requiring black level clamping or other video levels please refer to Digitisation of Active Video below.

With any high analog bandwidth ADC, analog inputs that are above the Nyquist frequency (½fc) will be reflected by the clock (aliases) into the normal signal bandwidth. The patterning caused by this can be removed from the picture by providing an adequate anti-aliasing filter before the ADC input.

Clamp Gate Input

The clamp gate signal should be fed to the board via SMC connector S2 and is terminated by a 50Ω resistor. The clamp gate input is also taken to the edge connector, pin 22.

For normal sync level clamping, the clamp gate input should be normally high, switching down thorugh the device input threshold (Vcc/2) during the sync period. Details of black level clamping are given in the data sheet and in Digitisation of active Video.

Reference

The negative reference for the SP94308 can be provided in a number of ways. In applications where accurate reference control is required, the voltage may be applied via the middle pin of the power supply connector S4. For less stringent systems R4 or D1 may be added to generate the reference from the -5.2V supply. If -2V is required R4 should be approximately 560Ω. Digitisation of Active Video details other possible voltages for the reference level.

Clamp Level : Link 1

If a standard 1V p-p video signal is to be digitised, then link 1 should be used to connect the negative reference to the clamp level adjust. Link 1 can be left open circuit in which case the clamp level adjust input will float to -1.4V for applications requiring black level clamping. To align the device to other digital standards it may be necessary to take the clamp level adjust to different voltage levels. In this case, feed the required voltage into the upper side of link 1.

Digitisation of Active Video

In the previous sections digitisation of 1V p-p video plus sync has been considered, using the sync tip as the clamping level. The versatility of the SP94308 allows effective alteration of the gain and offset of the device, so enabling specific sections of the video waveform to be digitised. For example, Fig.2 shows a luma signal in which only the active video is to be digitised. The SP94308 has an internal buffer with a gain of 2, giving the internal voltages shown in parentheses. When the sync pulse input is taken low, the internal clamp circuit offsets the waveform to the voltage applied on the sync level adjust pin. Fig.3 shows the result of sync level clamping to -2V, before and after the internal buffer. As only the active video is to be digitised, i.e. the section from 0 to -1.4V in Fig.3(b), then the voltage applied to pin 10 (REF -ve) should now be -1.4V. Reducing the voltage on the reference chain of the ADC can be compared to increasing the gain of the system. However, care should be taken when using this approach as a slight reduction in linearity will occur.

If black level clamping is required then setting the sync level adjust to -1.4V (Note: sync level adjust will float to 0.7 x REF -ve) and REF -ve to -1.4V will achieve the same results as in Fig.3, see Fig.4.

TOP VIEW
OF UNDERSIDE PINS

ALL TOP PINS = GND

Pin No.	Function
1	NC
2	NC
3	NC
4	NC
5	NC
6	NC
7	NC
8	-5.2V
9	-5.2V
10	A0 LSB
11	A1
12	A2
13	A3
14	A4
15	A5
16	A6
17	A7 MSB
18	NC
19	NC
20	NC
21	NC
22	SYNC OUT
23	NC
24	NC
25	CLOCK O/P
26	NC
27	+5V
28	NC
29	NC
30	NC

Table 1 Edge connections

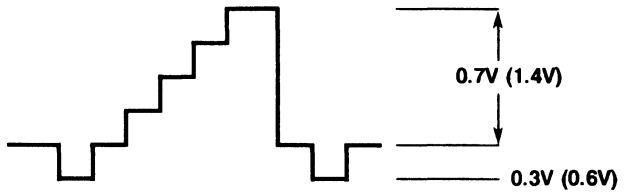


Fig.2 Luma signal

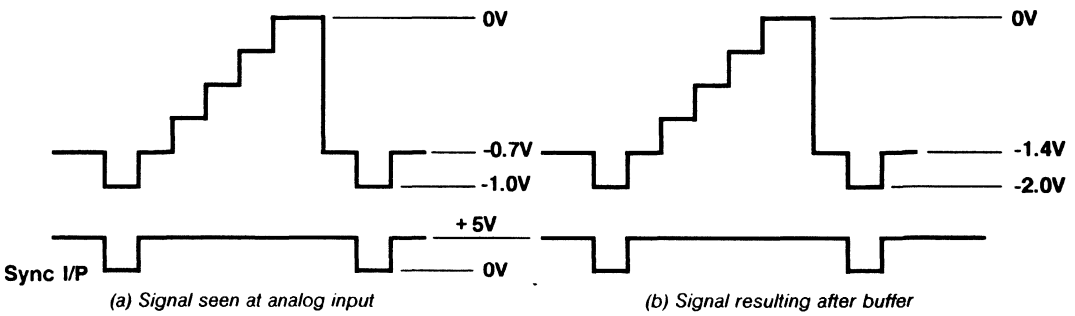


Fig.3 Luma signal after sync level clamping, sync level adjust = -2V

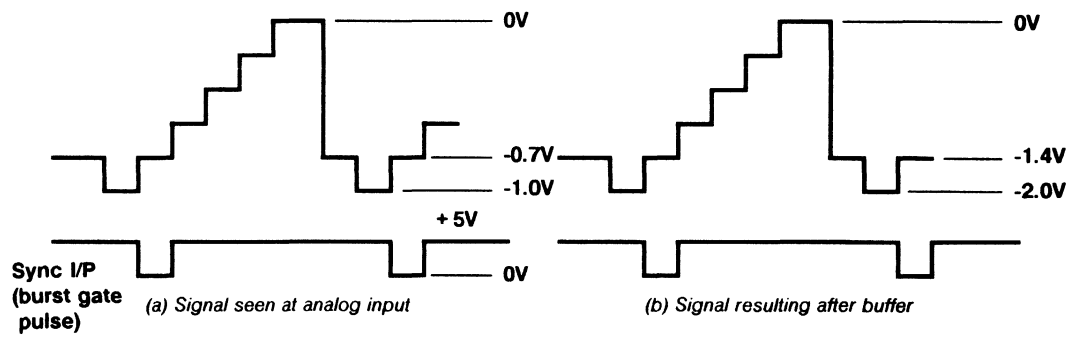


Fig.4 Luma signal after black level clamping, sync level adjust = -1.4V

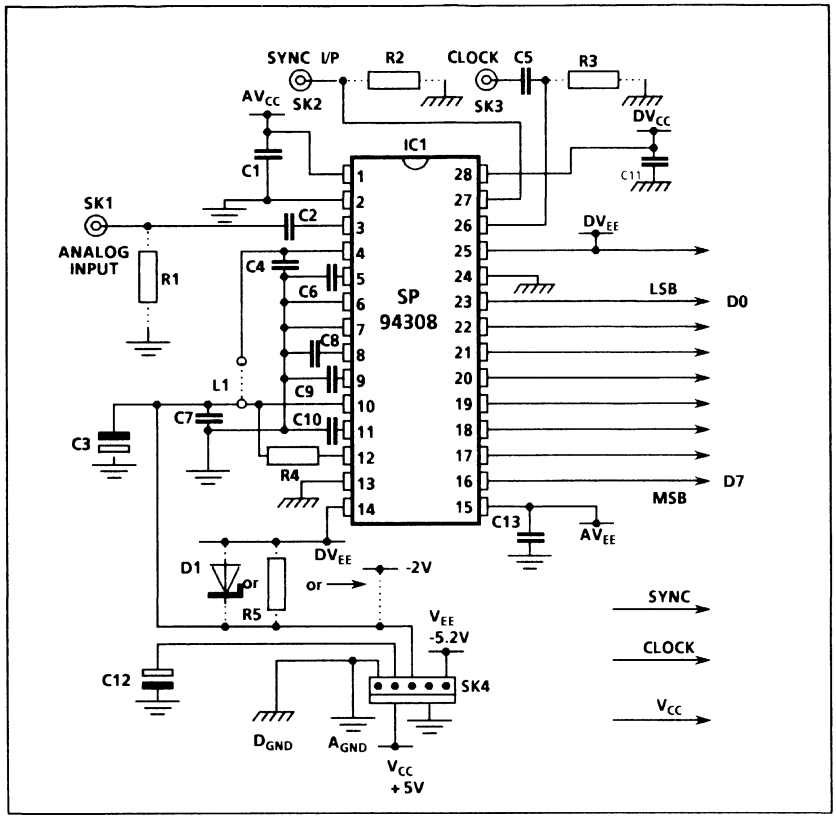


Fig.5 AP9008 circuit diagram

RESISTORS		CAPACITORS for ADC, Clamp, Bias etc.	
R1	75Ω (Optional Termination)	C1	100nF (Optional Decoupling)
R2	47Ω (Optional Termination)	C2	100nF (Input Coupling & Line Clamp)
R3	47Ω (Optional Termination)	C3	47μF (Electrolytic Decoupling)
R4	Approx.560Ω (Optional Low Cost -2V)	C4	100nF (Optional Decoupling)
		C5	100nF (Coupling)
SEMICONDUCTORS		C6	27pF at 20MHz or 47pF at 10MHz Clock
IC1	SP94308	C7	100nF (Decoupling)
D1	BZX79C3V0 (Optional Low Cost -2V	C8	100nF (Decoupling)
		C9	100nF (Decoupling)
SOCKETS		C10	100nF (Decoupling)
S1 - S3	Sub Vis Sockets (Optional)	C11	100nF (Optional Decoupling)
S4	KK Molex Socket (Optional)	C12	47μF (Electrolytic Decoupling)
		C13	100nF (Optional Decoupling)

Table 3 Component list and function

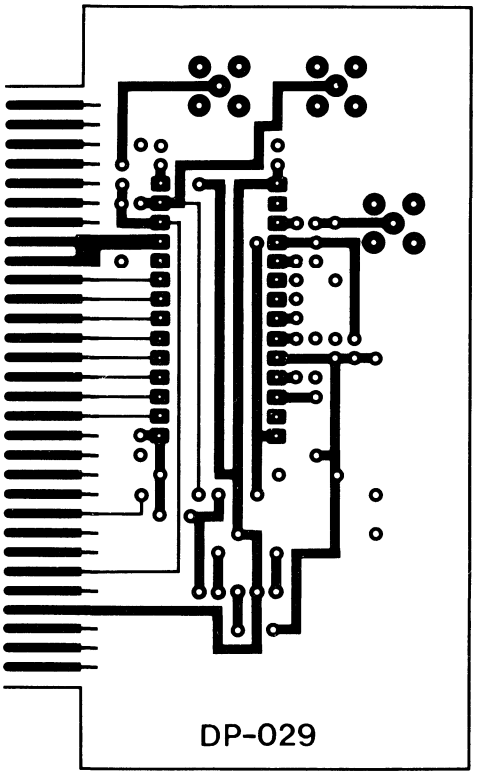


Fig.6(a) AP9008 PCB copper track (1:1)

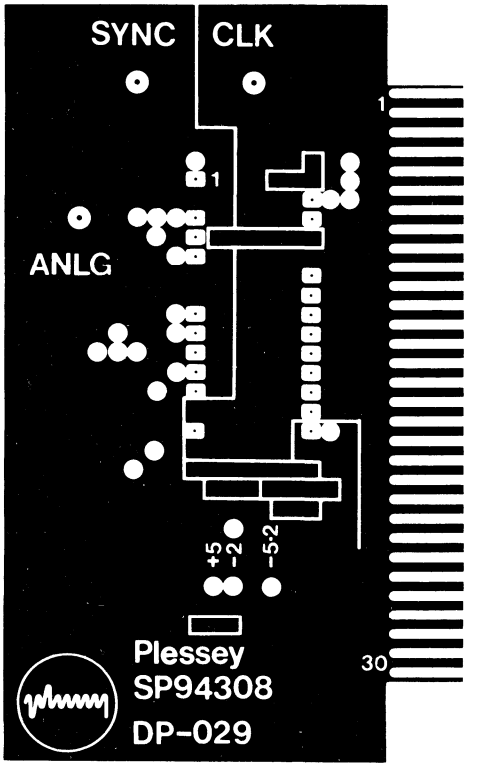


Fig.6(b) AP9008 PCB ground plane and component side (1:1)

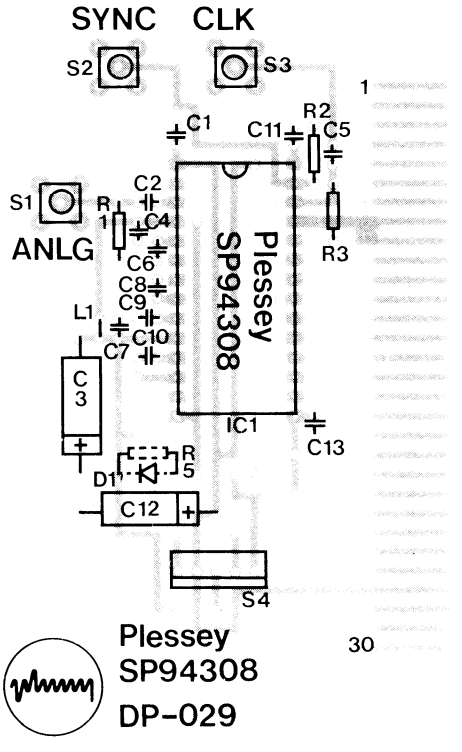


Fig.6(c) AP9008 component layout (1:1)

Evaluation and Comparison of High Speed ADCs

High speed ADCs are used in many varieties of applications; each application may require special consideration of one or more particular parameters. For example, designers of video (radar or TV) would pay particular attention to differential linearity, whereas designers using the ADC for measurement systems would need to pay attention to integral linearity. Other systems may need accurate information on analog power bandwidth or bit error rate.

Specification requirements therefore differ from application to application, and this can make comparisons of ADCs difficult. Outlined below are important tests and evaluation methods, starting with the most simple and progressing to the more sophisticated.

ADC evaluation falls into two main groups: the first group utilises high speed digital-to-analog converters to reconstruct the digital output into an analog form that can then be displayed on an oscilloscope. The second group of methods looks directly at the digital data. This requires a high speed logic analyser and usually a GPIB-compatible desk-top computer

The following discusses these evaluation methods using the Plessey SP97508 110MHz 8-bit ADC in the evaluation system (AP9006) described later.

TESTS USING DAC RECONSTRUCTION

Method 1. Low Speed Ramp (Fig.1)

This test is very simple. A linear full scale triangular wave (or ramp) is applied to the ADC input, at a frequency that is less than $f_{clock}/(2 \times 2^N)$, where N = number of bits. This ensures that all the timing intervals are displayed. The output from the ADC is then reconstructed with a DAC which should have a greater resolution than the ADC to ensure that all output codes are displayed. The results can then be viewed on a good high resolution oscilloscope.

The resultant staircase has vertical voltages that are due to the DAC and horizontal time intervals that are due to the ADC. Therefore any vertical errors can be ignored as they are due to the DAC alone. The horizontal time intervals can be viewed in more detail by using the oscilloscope to invert and add the input signal. The remainder will be the quantisation noise. The error will be 1 LSB high $\pm\frac{1}{2}$ an LSB. Beware of 'scope input overload and the delay between the two signals when using this method.

A major point of interest on this reconstructed ramp is the mid-step or zero crossing where a large differential error or high speed group of glitches can occur. This is a common problem with many ADCs as the digital section of the ADC is changing from 10000000 to 01111111. All the binary outputs are changing at once and hence large current spikes can result.

Another cause of zero crossing error is four-stage design. Within most 8-bit flash ADCs the reference chain and/or the comparators are split into four ranks. The device can then behave as four 6-bit devices. This can give poor differential steps at seven critical codes along this ramp.

Reference Voltage Considerations

The overall accuracy of the staircase will be mostly proportional to the reference voltage. This is because the internal comparator offsets will remain constant while the bit size will vary proportionally to the external reference voltage. Therefore it is important to consider the reference voltage before making comparisons between ADC linearity figures. Disadvantages of the ramp method are (a) it is difficult to obtain numerical results - although this can be achieved using a Tektronix 7854 scope - and (b) this test does not reflect the accuracy at speed.

Method 2. Near Nyquist Beat (Fig.2)

The Nyquist frequency is exactly one half the clock frequency. If a sinewave analog input is set close to this frequency in an unfiltered system, a beat will result. The beat frequency will be

$$f_B = \left|\frac{f_C}{2} - f_{in}\right| \text{ (3MHz in Fig.2)}$$

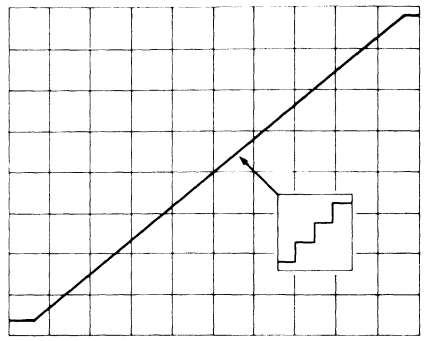


Fig.1 ADC linearity. 1kHz ramp input sampled at 100MHz (2V I/P to ADC)

This test is primarily for evaluation of analog bandwidth. The comparators acquire the input voltages at each end of the input dynamic range on successive samples. An ADC that can slew both positively and negatively fast enough to produce an undistorted sinewave beat contains an extremely fast comparator section. Disadvantages of this method are (a) again it is difficult to produce a numerical value of merit, (b) scope triggering is delicate and (c) DAC overshoot can cloud the results.

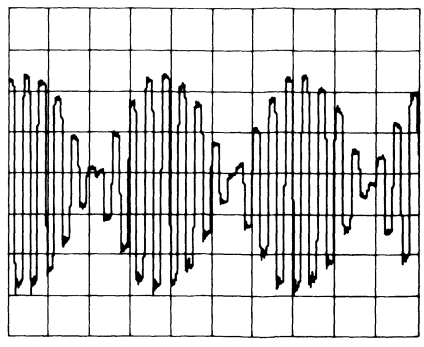


Fig.2 ADC near Nyquist beat. 47MHz input sampled at 100MHz, 2V I/P to ADC

TESTS USING DIRECT DIGITAL ANALYSIS

This group of tests is performed by acquiring the digital data directly from the ADC. The data is usually acquired by a high speed logic analyser and then transferred to a desk-top computer for analysis. The ADC is usually driven with a sinewave of full amplitude. The following gives the more popular methods of analysing and plotting the data. It is essential with all the following methods that the input is set to precisely full scale.

Most of the methods below benefit from phase-locked sampling (stationary sampling). In most cases this enables the number of samples taken to be greatly reduced, therefore improving test/evaluation times.

Method 1. Histogram Test (Fig.3)

This test plots the output code against occupancy of the code. A histogram is produced that should theoretically form a sinewave cusp. Deviations from this cusp will represent differential and integral linearity errors. A differential error would weight the probability of a code being occupied, either more or less than it should be over a large number of samples. This distorts the cusp in a positive or negative direction at the code in question. The advantage of this test is that it will indicate the dynamic accuracy of the ADC, i.e. the accuracy to input frequencies up to Nyquist. This is of course not practical using a DAC and oscilloscope. The disadvantages of this method are that (a) it requires a large number of samples and (b) as a cusp is formed, direct reading of linearity from the curve is difficult.

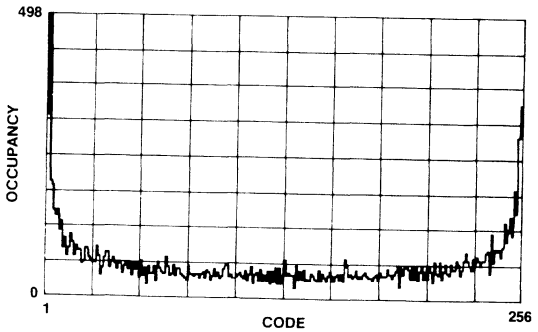


Fig.3 Histogram test at 30MHz input

Method 2.Non-linearity in LSB (Fig.4)

This test is almost identical to the histogram method. The same data can be used within the desk-top computer. Again a large number of samples are taken and again the occupancy of each code is plotted. The subtle difference is that a $\sin^{-1}$ weighting is applied to the results which removes the cusp. The linearity is then plotted :

$$\left[1 - \frac{(Actual\ Probability)}{(\sin^{-1}\ Weighted\ Probability)}\right]$$

As the cusp has been removed, the resulting graph shows at a glance differential non-linearity in terms of LSB. This test can also be performed up to Nyquist limits. Disadvantages are that random errors are averaged out.

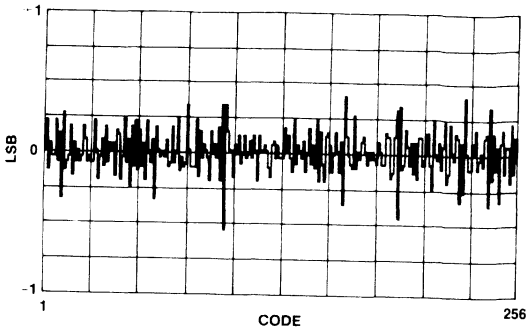


Fig.4 Differential non-linearity in LSB

Method 3. Accumulation Error (Fig.5)

Again, this test can be performed from the initial data. The data is processed to give a graph of integral linearity which can be expressed in two main ways - 'end point' or 'best fit'. The 'best fit' method allows the points to be compared with a line drawn through the average of the results. The 'end point' method is more severe as the line is defined by the end points of the results. From Fig.5 we could quote an integral linearity of ±0.5 LSB for 'best fit', but only ±0.75 LSB for 'end point'. Therefore it is very important to know which method has been used before comparing integral linearity figures.

To form the graph a statistical method is used with many samples taken. The results are corrected for the sinewave cusp and a graph plotted of levels against deviation from the previously defined straight line. This method can also be performed at frequencies up to Nyquist. Fig. 6 shows a plot of end point integral linearity at near Nyquist frequencies for the SP97508. As this test represents the total deviation from a theoretically perfect ADC it is a very useful measurement. It also gives a clear representation of distortion caused by the quantising system.

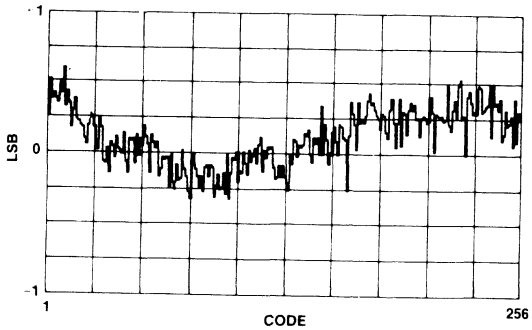


Fig.5 Accumulation error (integral)

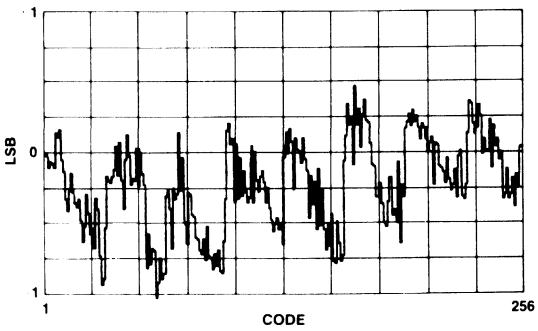


Fig.6 Accumulation error at 30MHz

Method 4. Sinewave Curve Fit

This test is similar again in that the data acquired by a logic analyser is processed by a desk-top computer. The computer generates theoretically perfect sinewave data, from which the actual ADC information, contained in the logic analyser, is subtracted. The data for the perfect ADC is produced by curve fitting: the Least Squares method is usually used to minimise the error between the actual and theoretical data. A theoretically perfect digitised sinewave which has exactly the same amplitude, frequency and phase as the actual data is required. The remaining difference between these groups of data now represents not only differential and integral linearity but also noise and aperture uncertainty effects. The disadvantages of the method are that (a) the programming must be very precise, (b) DC offset errors are ignored.

Method 5. Fast Fourier Transform

The fast Fourier transform (FFT) is simply a numerical method for conversion from the time domain to frequency domain. The method is based on the fact that any waveform can be constructed from a number of discrete pure sinewaves of different frequencies and amplitudes. These frequencies can then be plotted to give the spectrum of the signal.

Two methods are used for acquiring the data. The first and most popular, as in the previous methods uses a logic analyser, which transfers the data to a desk-top computer for FFT calculations. The second method (usually using a waveform analyser) uses a DAC to reconstruct the data which is digitised and sent to the computer for FFT. The spectral information from this method contains DAC distortions within the results. This can be an advantage if a complete system is to be analysed.

The FFT contains not only linearity information but also other errors that deteriorate the signal-to-noise ratio. Linearity errors cause sidebands to be produced in the frequency domain and so measurement and analysis of the system can be performed in great detail.

The disadvantages of the FFT method are (a) it is important to choose the input frequency to avoid coincidence between the fundamental and harmonics reflected back into the baseband by the sampling technique, (b) the input signal has to be exceptionally pure with very low harmonic content.

Choice of Tests

To form a good general assessment of a high speed ADC it is necessary to perform the DAC reconstruction tests as they not only show any gross problems with minimal effort, but also give a clear picture of any gross problems with the analog bandwidth and slewing performance of the ADC.

For an evaluation and experimentation system the accumulation methods give a clear picture of performance but for a test system the sinewave curve fit or FFT methods test a wider range of parameters.

OTHER TESTS AND CONSIDERATIONS

Aperture Uncertainty

Aperture uncertainty refers to the amount of jitter at the instant the sample is taken. In other words the time taken between one sample point and the next may not be exactly the same on the following cycle. This uncertainty is usually in the order of picoseconds and so measurement is incredibly difficult. Aperture uncertainty is also found within the comparator section of the ADC. The aperture uncertainty will be increased if the comparators take slightly differing times to respond to the sample request. The results from techniques using stationary sampling are probably more than 20% inaccurate at high frequency. The effects of aperture uncertainty can also be masked by the phase jitter on the clock signal used for the ADC.

Metastable States

This exotic term is used when discussing missing or random data errors. There is a finite probability that when a comparator is latched it is at balance. This in fact would be a very rare event, as noise and hysteresis would tend to trip the comparator within the time it is being latched. Nevertheless figures as high as 1 missing sample in 10^9 have been quoted.

A balanced comparator would in fact cause an error within the decode ROM and in many ADCs that causes an all '0's output code for that sample.

Mountain Climb Effect

The 'mountains' here are in fact the spikes produced by the fast edges of the clock. If they are not adequately removed from the reference chain and analog input an interesting effect occurs: as the clock edge speed is increased the reconstructed output will show a DC shift, sometimes above one LSB. This is due to the sample being taken at exactly the same time as the sample edge disturbs the input signal. The result is a 'DC' shift because they will always remain in phase. Good layout using split grounds and good decoupling will minimise this problem.

Data Valid Time

This is an important and frequently ignored parameter. It is simply the proportion of time that the output data is valid, expressed as a percentage of the minimum clock period. If the ADC has a maximum frequency of 100MHz i.e. a minimum period of 10ns, a 70% data valid time indicates that the data would be valid for 7ns and could be acquired at any time within this period. This is important as the shorter the time, the harder it is to design the system. High cost can result if extra latches and delay lines are needed to collect the data consistently over the specified temperature range.

AP9006 100MHz 8-Bit A/D-D/A Evaluation System

The Plessey AP9006 evaluation system is a complete 8-bit 100MHz analog to digital conversion system. The system comprises an 8-bit ADC with supporting circuitry, a connecting loom and an 8-bit DAC board. This DAC board allows the ADC outputs to be reconstructed and viewed on an oscilloscope.

Each individual application of the ADC may require different optimisation of parameters; this board has been designed to meet general requirements but little else should be required to meet even the most precise 100MHz system.

THE EVALUATION SYSTEM - AP9006

Included in the evaluation system are the SP97508 ADC board AP9004 (Fig.7), a length of 100Ω twisted pair and the SP97618 DAC applications board AP9005 (Fig.10). The D-A evaluation board provides a simple method of evaluating the all-important analog bandwidth of the ADC.It is suggested that, near Nyquist is viewed at 100MHz sampling to demonstrate the wide analog bandwidth of the SP97508 (see Figs.2, 3 and 4).

The ADC board (AP9004) comprises one SP97508 (8-bit ADC), one TAB1042 (quad op-amp), one SP9687 (dual comparator) one SP9210, one SP1662, one SL9999 and one RS7805 5V regulator.

Evaluation Boards

In general, the performance of a high speed ADC can be greatly affected by the circuit board ground plane layout and associated component placements. Plessey Semiconductors therefore make available for purchase completed ADC and DAC boards with connecting loom.

The items listed in Table 1 can be ordered from our Customer Service department: Tel: UK (0793) 726666.

Item	Description
AP9004	CompleteADC board and data
AP9005	Complete DAC board and data
AP9006	Complete ADC, DAC and connecting loom with data (recommended system)

Table 1 Evaluation systems available from Plessey Semiconductors

Power Supplies

The evaluation system requires external -5.2V and +12V supplies. A +5V supply is also required but this is provided from the +12V supply by an RS7805 regulator on the board. For convenience all power supplies have been taken through the edge connector to supply the DAC evaluation board.

Supply	AP9004 ADC Board only	AP9006 ADC & DAC System
-5.2V	700mA	1050mA
+12V	110mA	110mA

Table 2 Power supply currents

The current taken from the -5.2V supply increases to 1050mA when the DAC board is connected, due to the extra current taken by the line termination and device supplies.

ADC BOARD AP9004

The AP9004 applications board has been designed to allow adjustments to be made to all the important parameters that effect the performance of the SP97508 110MHz ADC. RV2, which adjusts the DC input offset, allows a wide range of input signals to be applied.

A wide range of clock signals can also be applied to the board as the PlesseySP9687 and SP1662 devices form a complext clock conditioning circuit for the ADC.

To enable the board to drive lines of 50Ω or 100Ω directly, the Plessey SP9210 high speed latch has been used. Technical data on this and the other devices mentioned can be found in the Plessey High Speed Data Products handbook.

The Plessey TAB1042 (TAB1043 recommended for new designs) quad operational amplifier has been used to provide the adjustable DC voltages which supply the reference chain of the ADC. The bottom of the reference chain V_{RB} can be adjusted using RV3 and the mid reference voltage can be adjusted using RV1.

Analog Input to the Board

The analog input is fed to the SL9999 and is terminated by 56Ω (R7). An offset can be applied by varying RV2 (see Fig.8).

The SL9999 is a fast ADC driver capable of driving the input capacitance of the SP97508 at over 50MHz and ×4 gain. Hence the peak-peak input voltage to the board is 0.5V.

The SL9999 ADC Driver

For a full evaluation of the SP97508 the input signal from the signal source should be coupled via R21 and R29 into the ADC. But in practical systems it can be difficult to drive the input capacitance of the ADC. This is due to the combination of high frequency, high capacitance and large voltage swings needed, whilst maintaining good linearity. In addition, the ADC input capacitance changes dynamically with input voltage. These factors led to the development of the SP9999 ADC driver.

The SP9999, unlike other ADC driving circuits can be used to provide gain as well as satisfying the above requirements. Also the separate buffer in the SP9999 can be used to aid in setting reference voltages for low DC drift applications.

As the SL9999 is an op-amp, the gain of the driver circuit is simply defined by the two resistors R18 and R11; the DC offset is controlled by RV2.

It is important to minimise strays around this ultra fast op-amp. Care should be taken in the choice of components, component placement and track layout. Eighth watt carbon resistors have been used to minimise stray inductance and capacitance and Rf has been positioned directly from pin 3 to pin 13 of the device, to reduce lead length and strays.

Note the SP9999 is useful for many other difficult applications such as line driving etc., and makes a useful lab stock device.

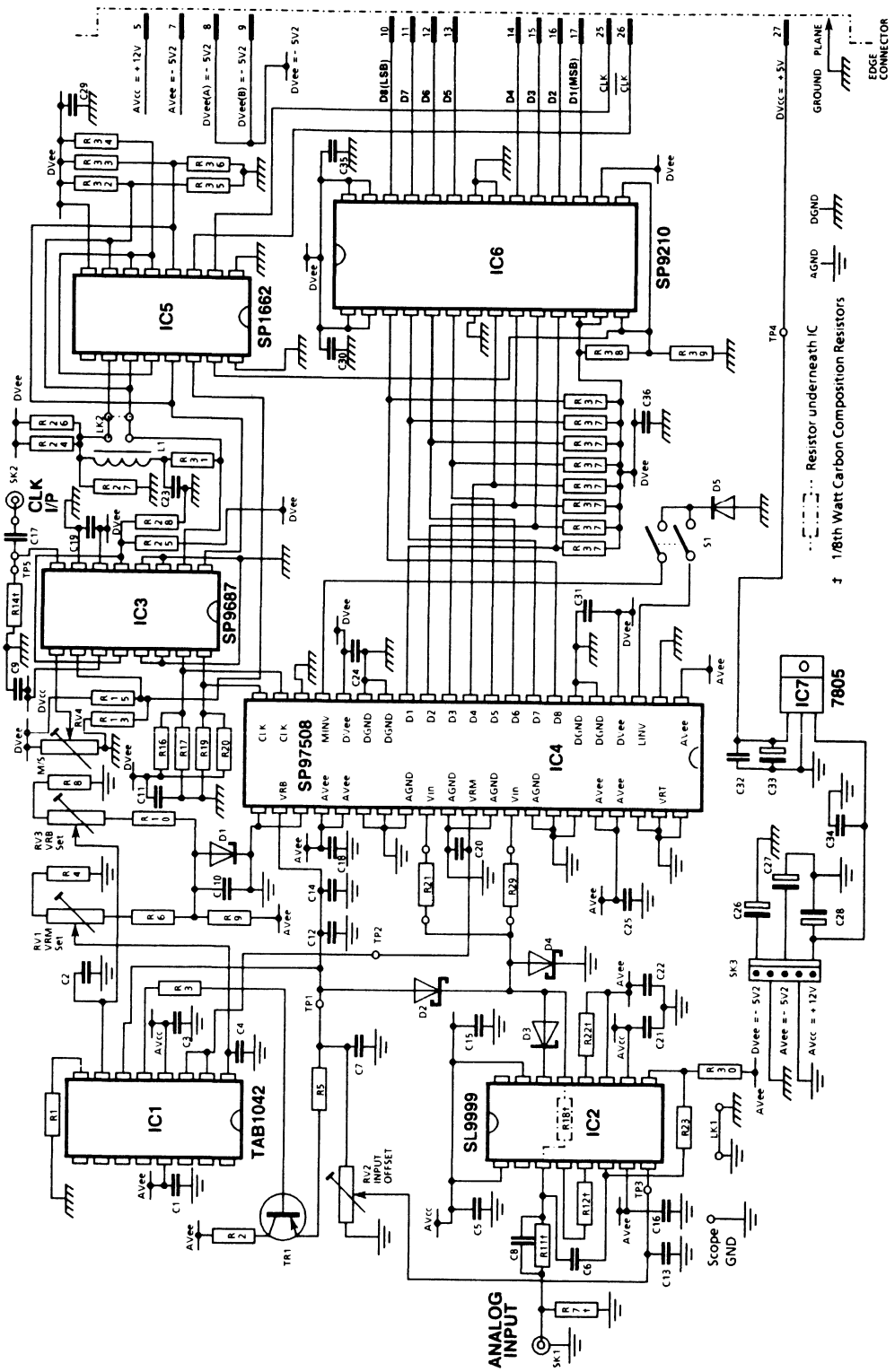


Fig.7 SP97508 ADC evaluation board AP9004

The Clock Conditioning Circuit

Unlike many other 8-bit ADCs the SP97508 can be clocked from a unity mark/space ratio clock, up to its maximum clock frequency (110MHz). This is due to the exceptionally wide bandwidth comparators and latches used in the device design.

As metastable states are of great concern in some communications applications, and the occurrence of these infrequent errors is affected by the mark/space ratio of the clock (in any flash ADC) we have provided a method on the board that can be used to select the clock mark/space ratio. We believe the optimum mark/space ratio for minimum errors is 3 to 1 (see data sheet).

The Plessey SP9687 dual comparator has been used to receive the incoming clock from either a sinewave oscillator or a pulse generator. Link LK2 can be positioned to select either unity or 3:1 mark/space ratio clock.

Component List for the AP9004 Board

RESISTORS

All ¼W unless otherwise stated

R1	220kΩ	R21	2.7Ω (optional)
R2	47Ω	R22	18Ω 1·8W
R3	10Ω	R23	470Ω
R4	2.2k	R24	1.2k
R5	10Ω	R25	3.9k
R6	3.3k	R26	4.7k
R7	56Ω 1/8W	R27	270Ω
R8	3.9k	R28	1k
R9	560Ω	R29	2.7Ω (optional)
R10	560Ω	R30	270Ω
R11	560Ω 1/8W	R31	220Ω
R12	220Ω 1/8W	R32	270Ω
R13	150Ω	R33	270Ω
R14	47Ω 1/8W	R34	1k
R15	270Ω	R35	150Ω
R16	270Ω	R36	150Ω
R17	150Ω	R37	1kΩ 8-way SIL
R18	2.2k 1/8W	R38	270Ω
R19	150Ω	R39	150Ω
R20	270Ω		

CAPACITORS

All encapsulated chip unless otherwise stated

C1-C5	10nF	C24,C25	10nF
C6	3.9pF	C26-C28	47µF 16V Electrolytic
C7	10nF	C29-C31	10nF
C8	Optional	C32	1µF
C9-C11	10nF	C33	47µF 16V Electrolytic
C12	10nF	C34	220nF
C13-C22	10nF	C35,C36	10nF
C23	6.8pF		

SEMICONDUCTORS

IC1	TAB 1042* (Plessey)	D1	ZN REF 025 (2.5V ref.)
IC2	SL9999 (Plessey)	D2	BAT 83
IC3	SP9687 (Plessey)	D3	BZX 5V6
IC4	SP97508 (Plessey)	D4	BAT 83
IC5	SP1662 (Plessey)	D5	IN 4148
IC6	SP9210 (Plessey)		
IC7	7805	TR1	2N3906 (PNP)

*NOTE:The TAB1042 will soon be discontinued. The TAB1043 can be used as a replacement, with a small mask change; please contact the Applications Laboratory if this causes concern.

SOCKETS

SK1,SK2,	PCB Mounting SUB-VIS or SMC
SK3	5-pin KK MOLEX

POTENTIOMETERS

RV1-RV4	1K Multiturn

MISCELLANEOUS

6-off	Veropins
S1	2-way SPST DIL Switch
1	Microshunt
4-off	Rubber Feet
1	4-way Header
1	16 pin Turned Pin IC Socket
1	Wire Link (24 Gauge Wire)
L1	220nH Inductor

EDGE CONNECTORS (Top View)

ADC BOARD		DAC BOARD	
Pin No.	**Function**	**Pin No.**	**Function**
1	N/C	1	N/C
2	N/C	2	N/C
3	N/C	3	N/C
4	N/C	4	N/C
5	AV_{CC} OUT	5	N/C
6	N/C	6	N/C
7	AV_{EE} OUT	7	N/C
8	DV_{EE}(A) OUT	8	DV_{EE}(A) IN
9	DV_{EE}(B) OUT	9	DV_{EE}(B) IN
10	D8 LSB	10	D8 LSB
11	D7	11	D7
12	D6	12	D6
13	D5	13	D5
14	D4	14	D4
15	D3	15	D3
16	D2	16	D2
17	D1 MSB	17	D1 MSB
18	N/C	18	N/C
19	N/C	19	N/C
20	N/C	20	N/C
21	N/C	21	N/C
22	N/C	22	N/C
23	N/C	23	N/C
24	N/C	24	N/C
25	$\overline{CLK}$	25	$\overline{CLK}$
26	CLK	26	CLK
27	DV_{CC} OUT	27	DV_{CC} IN
28	N/C	28	N/C
29	N/C	29	N/C
30	N/C	30	N/C

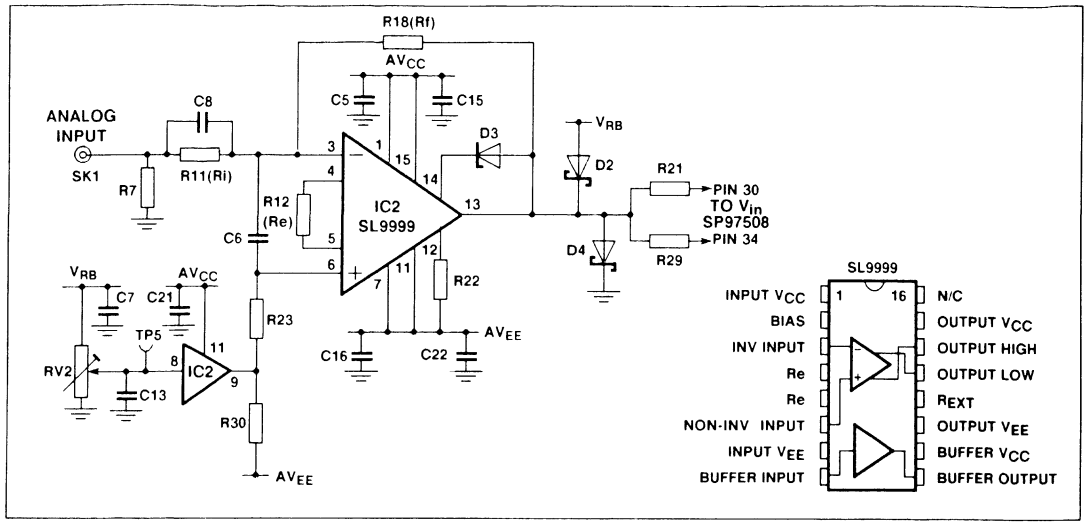


Fig. 8 Analog input driver for AP9004 ADC board

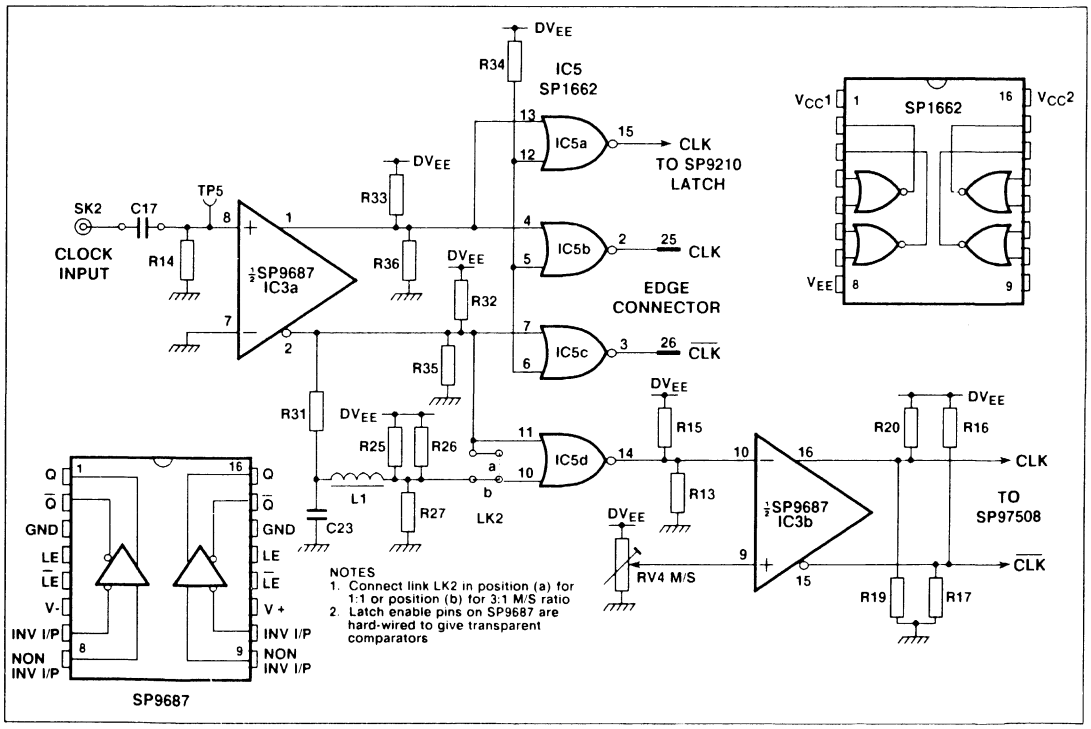


Fig.9 Clock system for AP9004 board

DAC BOARD AP9005

The following information describes the SP97618 250MHz graphics DAC applications board AP9005.

This board is capable of acquiring the 8-Bit 100MHz data from the ADC board in a fast retaining latch. It then converts this data into an analog signal that can be displayed on a fast oscilloscope.

The Plessey SP97618 DAC used on this board is a complete graphics DAC with video control inputs and is ideal for high resolution video signals

The switch S1 can be used to select individual data bits and switch S2 can be used to demonstrate the graphics facilities of the device (FT,FH,BLANK,BRIGHT and SYNC)

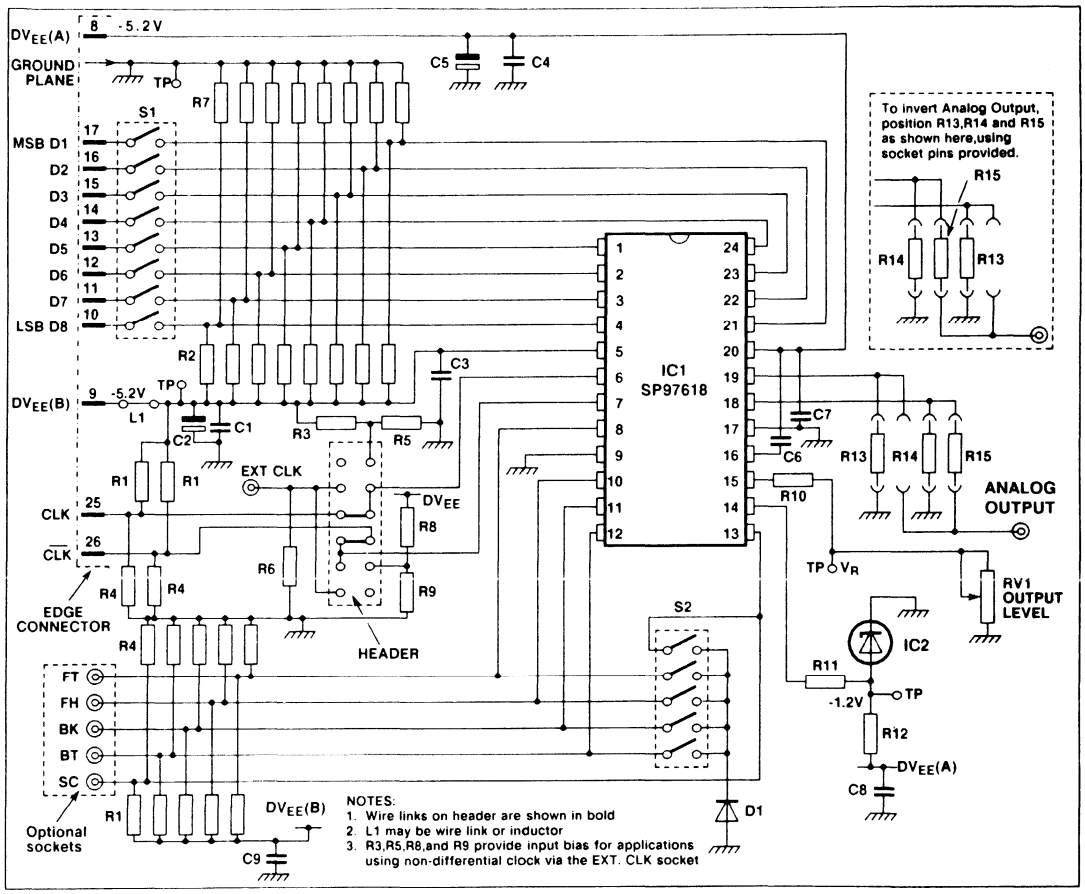


Fig. 10 SP97618 DAC applications board AP9005

RESISTORS

R1	8 x 270Ω SIL RS Part No. 140-237
R2	8 x 270Ω SIL RS Part No. 140-237
R3	270Ω
R4	8 x 150Ω SIL RS Part No. 140-215
R5	150Ω
R6	47Ω 1/8 watt
R7	8 x 150R SIL RS Part No. 140-215
R8	270Ω
R9	150Ω
R10	470Ω
R11	1K
R12	2K
R13	39Ω
R14	75Ω
R15	24Ω

RV1 1K CERMET 20 TURN

CAPACITORS

C1	0.1µF Encapsulated Chip
C2	47µF 16v Electrolytic
C3	10nF Encapsulated Chip
C4	10nF Encapsulated Chip
C5	47µF 16v Electrolytic
C6	10nF Encapsulated Chip
C7	0.1µF Encapsulated Chip
C8	10nF Encapsulated Chip
C9	10nF Encapsulated Chip

SEMICONDUCTORS

IC1	SP97618(Plessey)
IC2	LM113 or LM313
D1	1N4148 or similar

MISCELLANEOUS

S1	8-way SPST DIL Switch
S2	6-way SPST DIL Switch
1-off	12-way Unshrouded Header
2-off	Sub-Vis Connectors
4-off	Vero Pins
2-off	Micro Shunts
4-off	Rubber Feet

RELATED DOCUMENTS

Low Cost Video Speed A-D/D-A (Publication No.P.S. 1993) (Plessey Semiconductors)
High Speed Data Products Integrated Circuits Handbook (Publication No.P.S. 1989) (Plessey Semiconductors)
A Complete 100MHz 8-Bit ADC/DAC Evaluation System (Publication No.P.S.2048)

ACKNOWLEDGEMENTS

DM/DP-87
Plessey Design UK
Plessey Applications UK
Plessey Applications California USA

REFERENCES

Dynamic Performance Testing of A to D Converters - Hewlett Packard Product Note 5180A-2.

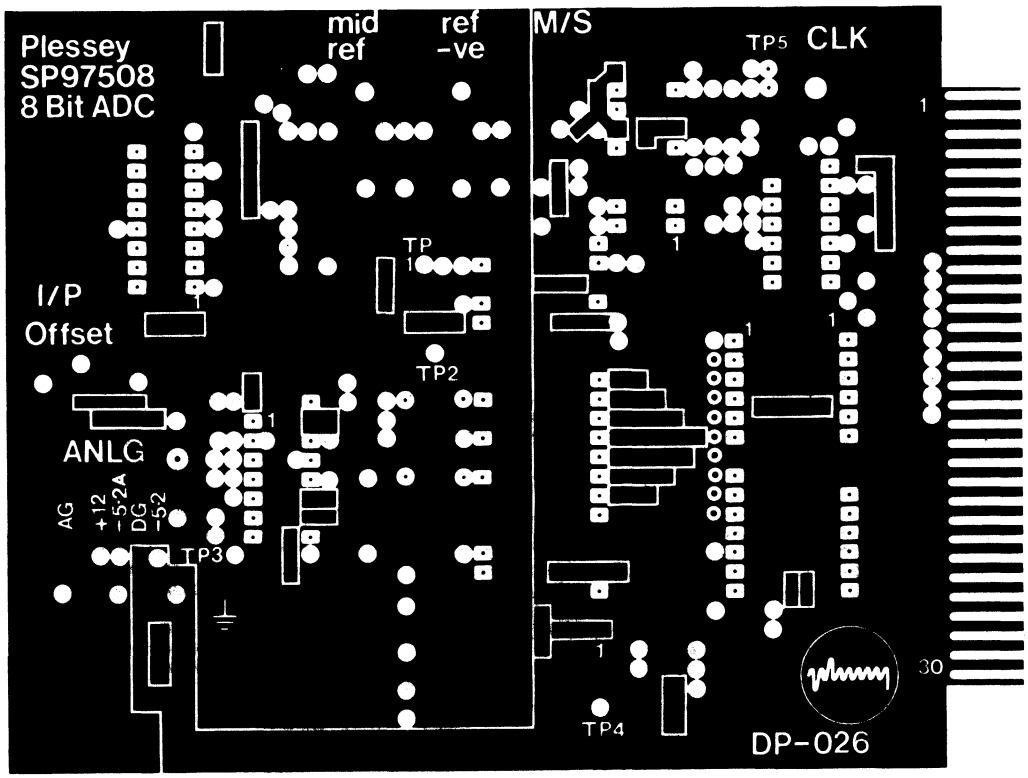


Fig.11(a) AP9004 ADC board, ground plane

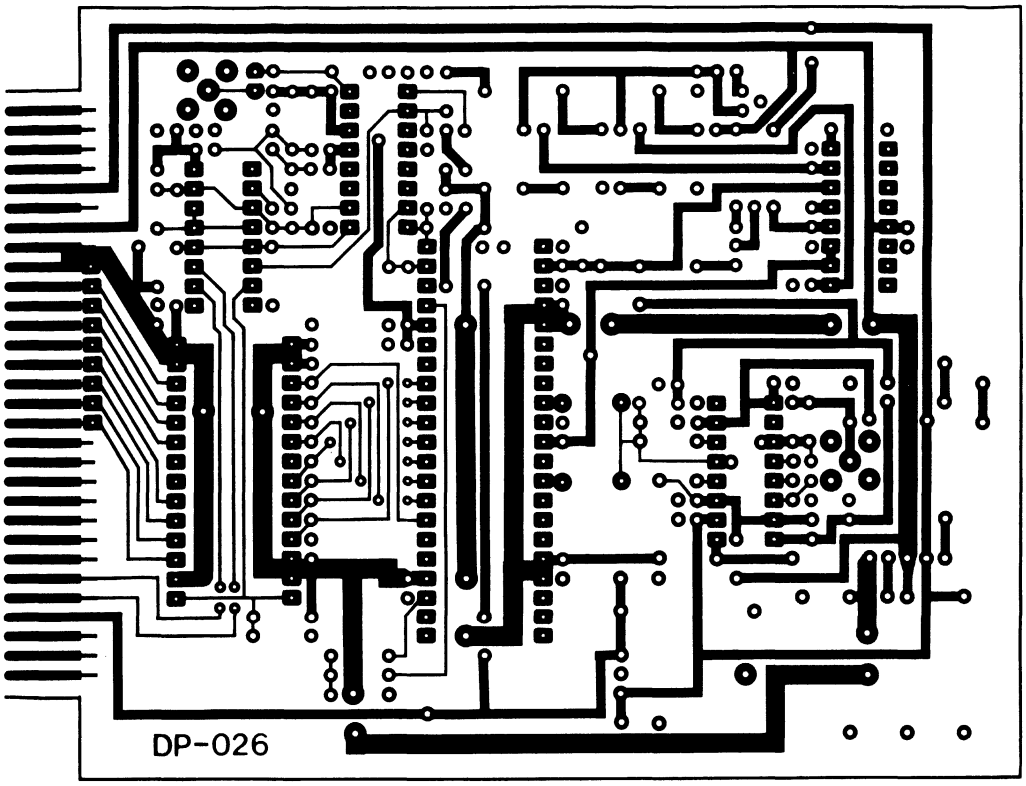


Fig.11(b) AP9004 ADC board, track side

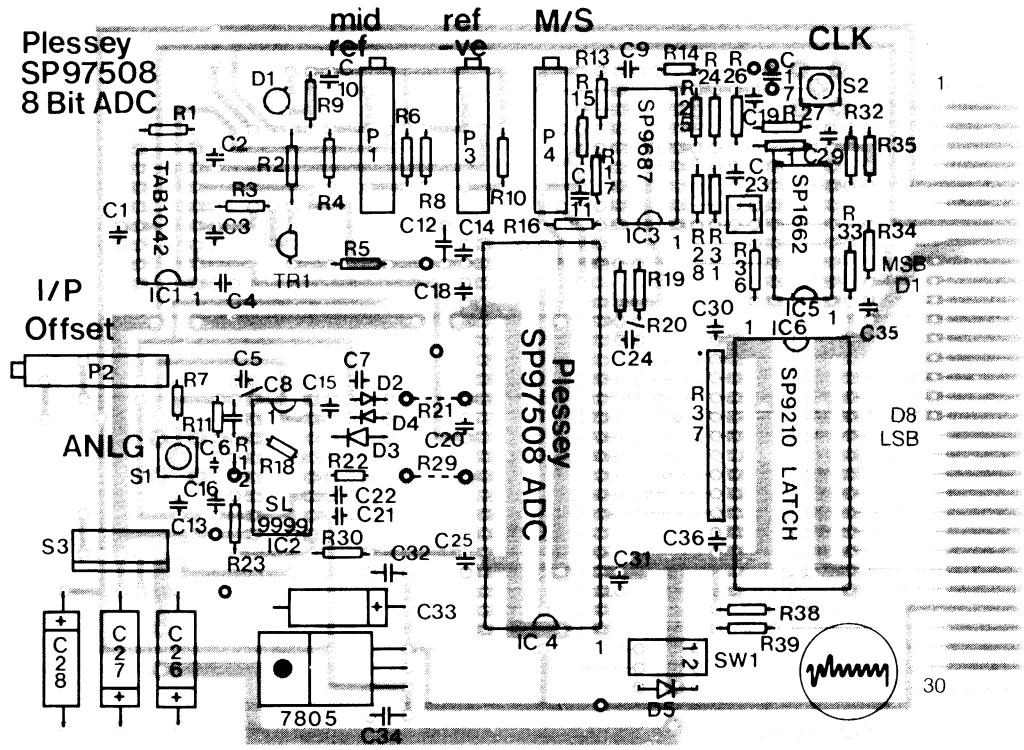


Fig.11(c) AP9004 ADC board, component layout

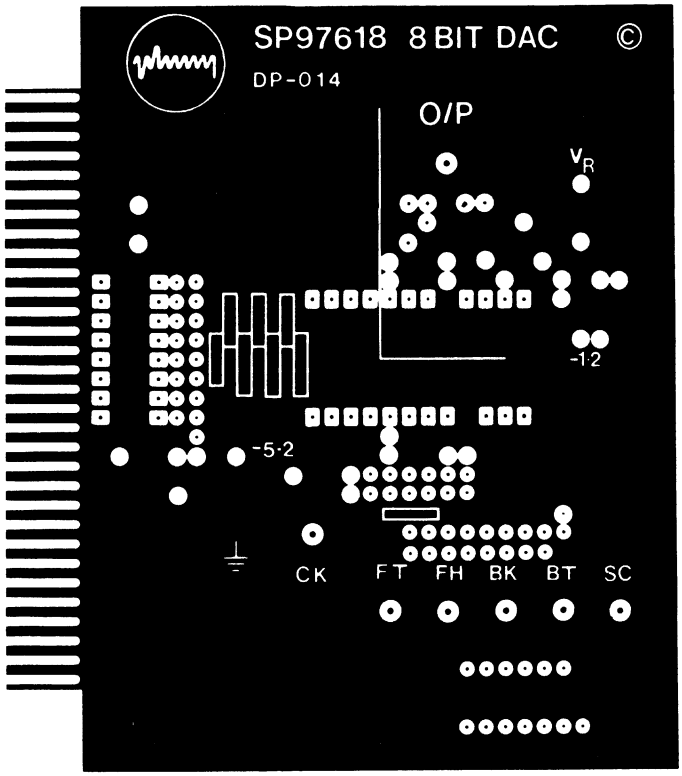


Fig.12(a) AP9005 DAC board, ground plane

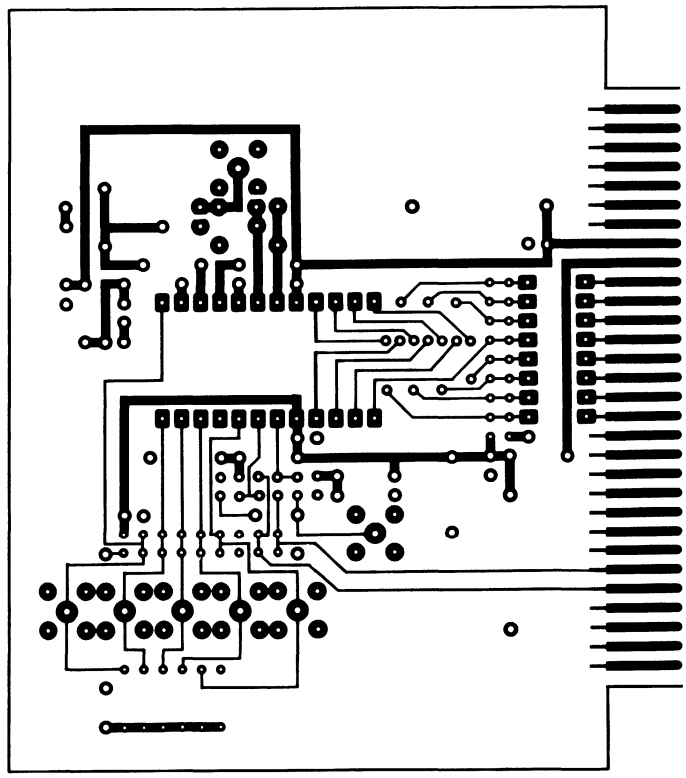


Fig 12(b) AP9005 DAC board, track side

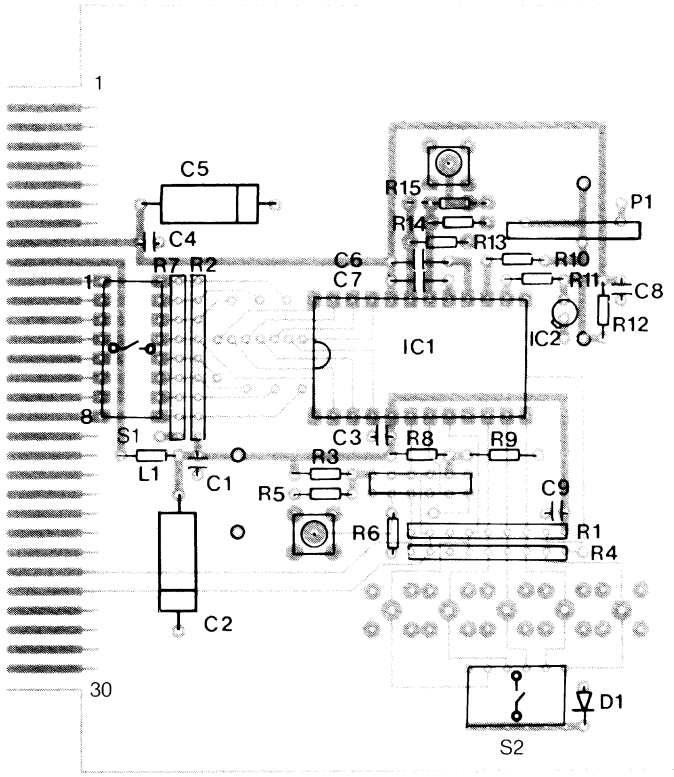


Fig.12(c) AP9005 DAC board, component layout

High Speed ADC Bit Error Rate Measurement AN65

This application note describes a measurement system which can be used to measure the number of bit errors per second produced by a high speed ADC. The technique can be used at low frequency or with full amplitude near Nyquist input conditions (50MHz).

This application note should be read in conjunction with '100MHz ADC/DAC evaluation system for the SP97508 ADC and SP97618 DAC'.

INTRODUCTION

It has been generally assumed that the only way to make accurate ADC bit error rate measurements was to use a very large high speed memory to capture vast amounts of data. Then a computer would be needed to sift through this data, to find and count the number of bit errors. This method becomes impractical at very high data rates with today's ADCs, as the size of high speed memory required to capture the data becomes too large and costly.

The measurement technique described here, needs neither the computer or memory, yet it gives a readout of errors per second *in real time*. This is achieved using standard lab equipment and the Plessey application board AP9004 (SP97508 ADC) plus two AP9005s (SP97618 DAC).

BASIC THEORY OF THE TECHNIQUE

Before examining this system at near Nyquist input frequency the explanation can be simplified by first describing a low input frequency system. Then it can be shown how this simple system can be modified to measure bit errors with a full amplitude near Nyquist input.

Low Speed System

If the slew rate of the input signal to the ADC under test is set to a very low frequency (say, f') it is certain that at a clock frequency of f_c at least one sample would be taken between each of the comparators within the flash ADC. The resulting reconstructed DAC output would then show all 2^N levels.

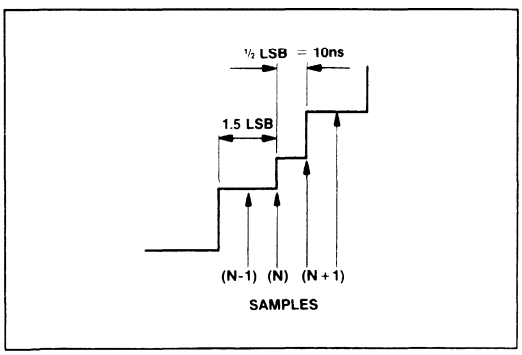


Fig.1

If f' is calculated for a specific f_c and N (number of bits) it can be ensured that the data from the ADC will never change by more than one LSB between any two successive samples. See Fig.1.

Therefore, at the output of the ADC, (DATA N) - (DATA (N-1)) $\leq$ 1 LSB.

This rule will only break down if a code error or a bit error occurs. It will be discussed later how to count the resulting error codes, but first to set up this system the value of f' must be calculated.

Calculation of f'

From Fig.1 a general formula can be derived for f' in terms of N, f_c and the minimum differential linearity error (e_{min}).

To do this must first be calculated the maximum rate of change of voltage which gives one LSB change at the output of the ADC, each time we take a sample.

$$\text{The rate of change of the input is } \frac{\Delta V}{\Delta t}$$

The voltage at the input for a 1 LSB change at the output is:

$$\Delta V = V\,p\text{-}p\ \frac{1}{2^N - 1}\quad N = \text{number of bits}$$

Now to take into account the minimum differential linearity:

$$\Delta V = \frac{V\,p\text{-}p}{2^N - 1}\ (e_{min})$$

Δt is simply $\frac{1}{f_c}$ ie, one clock cycle

$$\text{Therefore } \frac{\Delta V}{\Delta t} = \frac{\frac{V\,p\text{-}p}{2^N - 1}\ (e_{min})}{\frac{1}{f_c}} = \frac{V\,p\text{-}p\ f_c\ (e_{min})}{2^N - 1} \quad \ldots (1)$$

It is now possible to calculate the sinusoidal input frequency f' which gives this maximum rate of change of input voltage.

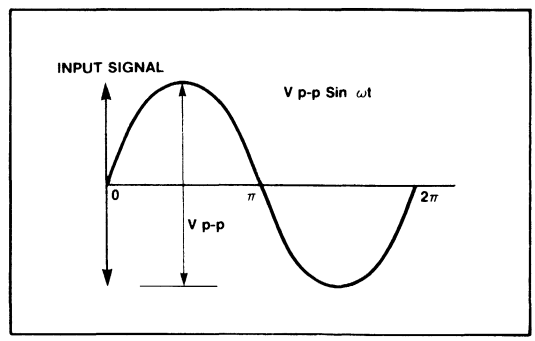


Fig.2

The maximum rate of change of a sinewave is when $\omega t = 0$, π or 2π.

$$\text{ie. when } \frac{dV}{dt}(V\,p\text{-}p\ \sin\ \omega t) = 0, \pi \text{ or } 2\pi$$

$$\text{Now } \frac{dV}{dt} V\,p\text{-}p\ \sin\ \omega t = V\,p\text{-}p\ \omega \cos\ \omega t$$

Therefore as $|\cos\ \omega t| = 1$ for $\omega t = 0, \pi$ or 2π, the maximum rate of change must be given by:

$$V\,p\text{-}p\ \omega \times 1$$

$$\text{Therefore } \frac{dV}{dt} \text{ max } = V\,p\text{-}p\ 2\pi f' \qquad \ldots (2)$$

$$\text{Hence, when } \frac{dV}{dt} \text{ max } = \frac{\Delta V}{\Delta t}$$

The required conditions are satisified. ie. when equation (1) = equation (2).

$$\frac{V\,p\text{-}p\ f_c\ (e_{min})}{2^N - 1} \quad V\,p\text{-}p\ 2\pi f'$$

Cancelling V p-p and rearranging for f' gives:

$$f' = \frac{f_c\ (e_{min})}{2\pi\ (2^N - 1)} \qquad \ldots (3)$$

As we now have a general formula for the maximum input frequency at which the ADC outputs only change by 1 LSB, we can calculate f' for our 100MHz 8-bit device (SP97508) (e_{min}) = ½ LSB.

$$f' = \frac{100MHz\ 0.5\ LSB}{2\pi\ (2^8 - 1)}$$

$$\text{Therefore } f' = \frac{100MHz\ 0.5}{1602}$$

$$f' = 31.2kHz$$

The analog input must therefore be set to less than 31.2kHz to ensure that the output code only changes by 1 LSB or less between each sample. A safety factor can be applied to this frequency but we must not go too low as we need to measure errors on as many levels as possible within each second (20kHz is a suitable low frequency).

COUNTING THE BIT ERRORS

Before proceeding with any bit error measurement we must first make sure that the device is not producing code errors.

This is easily done by viewing the reconstructed 20kHz sinewave output on a scope. As code errors occur on every cycle they are easily visible on an 8-bit device.

As stated previously, a bit error has occurred if the difference between any two adjacent codes is greater than I LSB. We can therefore detect the occurence of any bit error by subtracting data (N-1) from data N and then looking for a result greater than one.

This system delays the 8 bits output by one clock cycle and then sums this with the complement of the original data, thus producing the difference between data N and data N-1. If the LSB is ignored the resulting 7 bits should remain at zero unless a bit error occurs. Bit errors are detected by the OR gate. These pulses can then be counted using a frequency counter yielding a result in errors per second.

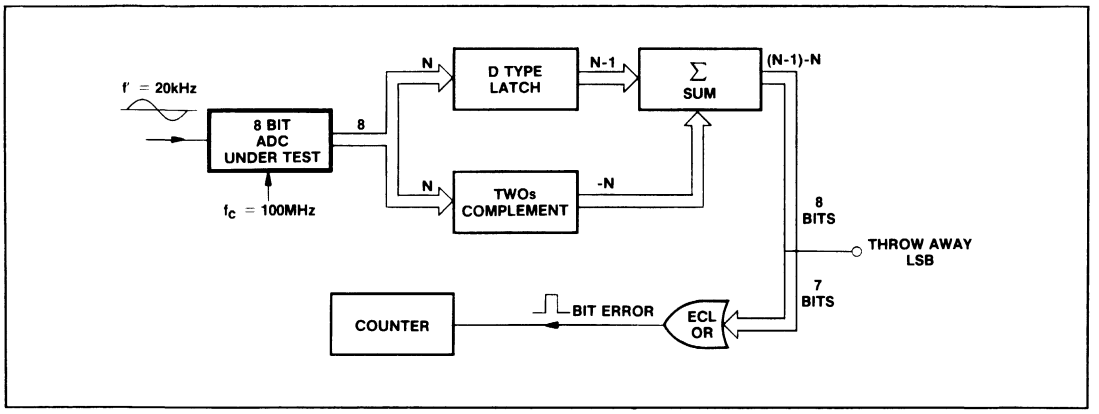


Fig.3

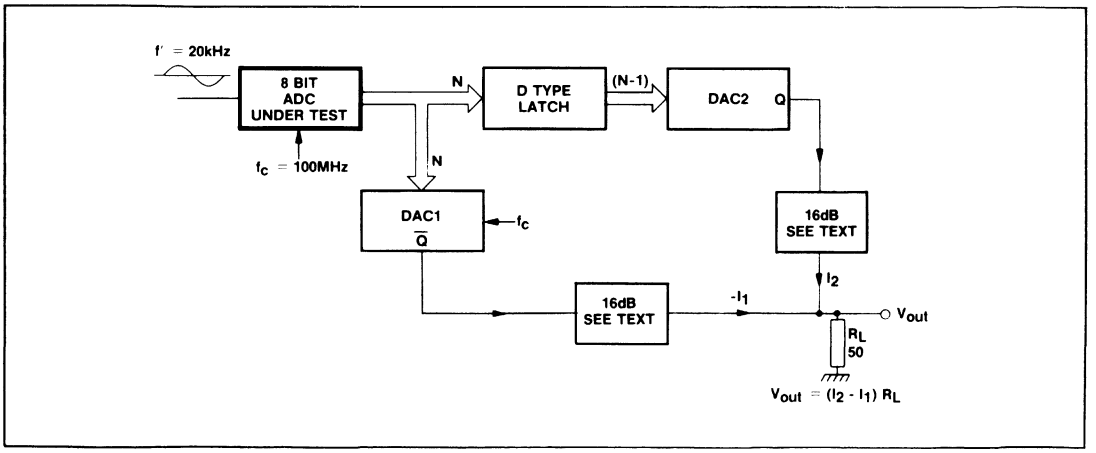
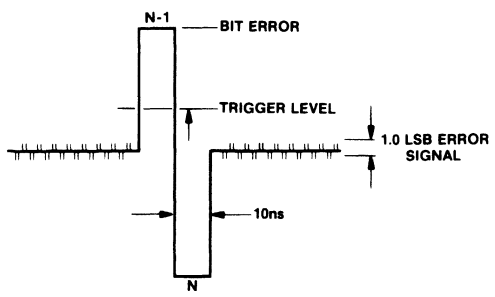


Fig.4

Analog Technique

This analog technique is an alternative to the digital subtraction method. Digital subtraction can be very difficult at 100MHz and above. (However it can be ideally suited to production testing.) The analog technique now described takes advantage of the very high speed latched DACs now available (SP97618 or SP98608). These 200MHz or 400MHz DACs can be used to reconstruct the data. The subtraction can then be performed very simply by summing the true and inverse analog DAC output currents into a 50Ω load (Fig.4).

V_{out} will be a small error voltage signal 1 LSB high, unless of course a bit error occurs, in which case a pulse is produced with an amplitude proportional to the erroneous code the error has caused. The pulse will also be seen on the next cycle of the clock, due to the one cycle delay in the latch. On this second cycle a negative going voltage will be seen.



NOTE: This waveform can only be seen with full intensity on the scope and a very bad ADC in circuit, as it may only trigger the scope 1-200 times per second.

Fig.5

Counting these bit errors is very simple as most scopes produce a trigger output signal from the rear panel. This can be connected directly to a counter. The scope trigger level can then be adjusted so that the normal 1 LSB error is ignored. The scope trigger must be set to DC and normal with the timebase at about 100ns/div.

The system can be calibrated to look for bit errors greater than a chosen number of bits. This is done by switching off the LSBs of DAC1 to produce the error amplitude above which bit errors are to be counted. The scope trigger is then set so that triggering is just lost. The LSBs can then be reintroduced into DAC1 and the errors counted on the counter as above. This technique is most useful when small code errors are present as these need to be ignored to measure the remaining bit errors.

Attenuators

These are placed in the path of the current flowing to the summation resistor, and provide a cleaner signal on the scope. This is due to the fact that most current output DACs are very capacitance sensitive. The attenuators reduce the amount of scope input capacitance seen by the DAC outputs. The settling times of the DACs are therefore much improved.

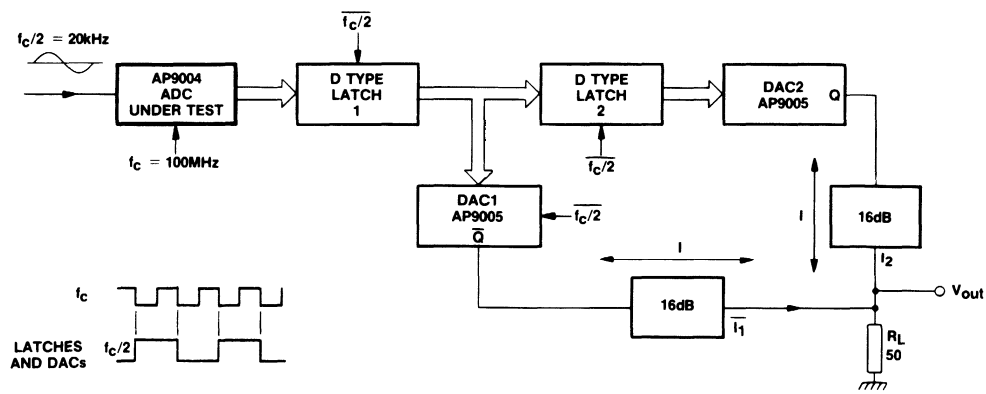
HIGH SPEED INPUT BIT ERROR MEASUREMENTS

Measurement of Bit Errors with Full Amplitude near Nyquist Input Signals

The bit error rate of an ADC is not only dependent on the clock mark-to-space ratio and temperature, but also on the frequency of the anlog inmput, and of course the input amplitude.

The definitive test for bit errors within an ADC would therefore be with a full ampltiude near Nyquist input signal at maximum ambient temperature and 1:1 clock mark-to-space ratio.

This measurement can be achieved by adding a simple D type latch (clocked at $f_c/2$) to the output of the ADC and again we can follow the previous analog measurement technique to measure the bit error rate, under high frequency input conditions.



The length of cable from each DAC to the load should be adjusted for minimum glitches on V_{out}.

Fig.6

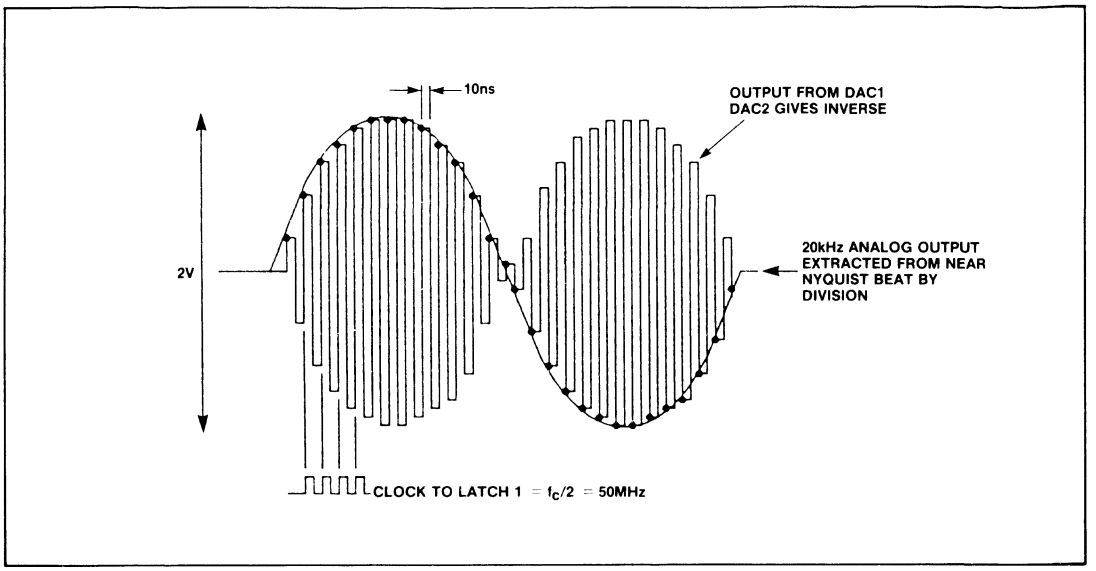


Fig.7

D type latch 1 will now divide the output data. This means that every other data word is discarded. The reason for doing what seems to be a waste of good output information is to extract the envelope from the Nyquist beat pattern (see Fig.7).

If the analog input to this system is set correctly (f'a) we can again be confident that even though the input frequency is at near Nyquist, there will be only one LSB change at the output of the ADC, but this time on every other clock cycle.

The analog input frequency must be within f' of Nyquist:

$$f'a = \frac{f_c}{2} \pm f'$$

In general the lower of the two resulting frequencies is chosen.

$$f'a = \frac{f_c}{2} - f'$$

The general expression for the near Nyquist input frequency that will produce only one LSB change every other clock cycle is:

$$f'a = \frac{f_c}{2} - f'$$

$$f'a = \frac{f_c}{2} - \frac{f_c\,(e_{min})}{2\pi\,(2^N - 1)}$$

$$\text{Therefore } f'a = \frac{f_c}{2}\left(1 - \frac{(e_{min})}{\pi\,(2^N - 1)}\right) \quad \ldots (4)$$

Where: f_c = clock frequency
N = number of bits
$f'a$ = analog input frequency
(e_{min}) = minimum differential error

We can now determine this input frequency for the 100MHz 8-bit device.

$$f'a = \frac{100MHz}{2}\left(1 - \frac{0.5}{\pi\,(2^8 - 1)}\right) = 49.9687MHz$$

The two analog waveforms from each DAC are summed in R_L to produce the small 1 LSB error signal as before. The only difference between this and the low speed test is that due to the fact that the ADC output was divided by 2. The displayed error count must now be multiplied by 2.

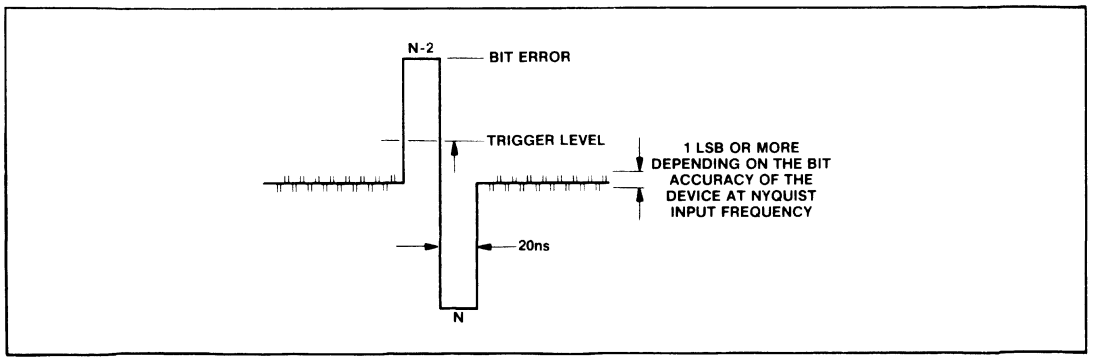


Fig.8

It is wise to add a small safety margin to this input frequency, as some competitors products will show significant deterioration of accuracy with input frequency. A frequency of 49.98MHz was chosen as a standard input frequency for tests on the Plessey SP97508.

The results from the counter (connected to the trigger outputs of scope) will be in counts per second. As the total number of operations per second is 10^8 (f_C = 100MHz) a result of 4 counts per second would be equal to 4 x 2 in 10^8 ie. 8 in 10^8 bit errors.

It is possible when using the high speed technique to simply switch the analog input from 49.98MHz to 20kHz to find the low frequency error rate (do not forget to multiply the result by x2 if the division is not removed).

The system timing allows both the data capture time and mark space ratio to be adjusted without affecting the measurement technique. These adjustments can be made to the system by connecting the HP8640 (used as a master oscillator) to a HP8082 pulse generator. The HP8640 also drives the SP9131 divide by 2 circuit. The pulse generator (HP8082) drives the clock of the ADC via a SP8687 comparator which is already present on the AP9004 applications board.

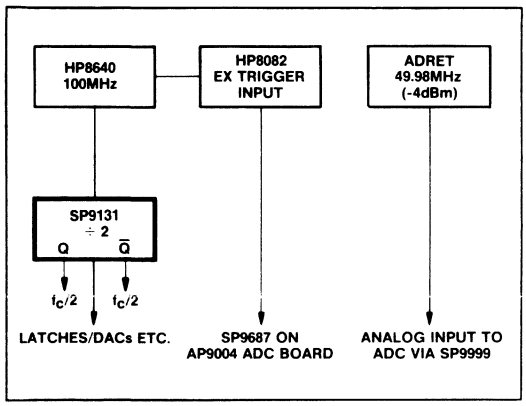


Fig.9

EQUIPMENT AND SETTINGS FOR FULL NYQUIST BEAT BIT ERROR RATE TEST

HP8640 or equalivent (master system clock)
+10dBm, 100.000MHz, AM = off, FM = off, RF = on.

HP8082 (clock conditioning for ADC, driven from 8640)

Ext trig, slope/polarity = pos, rate = 100m 10m ⟲ ← knob position.

Pulse delay = 2n-5n ⟲, Pulse width = 5n-50n ⟲

Trans time = 1n-5n ⟲ ⟲, Amplitude (into 50Ω) = 1.0-2.0 both, vernier = ⟲, offset = on ⟲, $\overline{\text{use output}}$ (right), neg pos = pos, normal compl = compl.

ADRET or equivalent (analog input to ADC. Another HP8640 could be used). 49.98MHz, -4.98MHz, -4dBm (adjust to full amplitude reconstructed output).

Counter (to count triggers ie. bit errors from external trigger out of scope). Philips M6671 was used with all buttons out apart from power.

Measuring time = 1 second, hold off = 0, set to freq A, use A input, trigger (⟲ Pushed in).

Scope (any 300MHz scope with trigger out), 5mV/DIV. AC coupled (full BW), trig = normal DC -ve slope time base 100ns/div.

Power Supplies

+5V at 220mA, -5.2V at 1.52A, +12V at 108mA.

Attenuator

Two 50Ω attenuators set to 16dB.

CONCLUDING REMARKS

We have shown that an accurate and consistent measurement of bit errors can be achieved using general lab equipment, combined with standard Plessey applications boards, two latches and a little ingenuity. This technique can be used even when the ADC is performing under the most severe input and clock conditions.

The major advantage of this method is that the result from the counter is in real time. Therefore it is much easier to see the effects of small parametric changes to the setup of the ADC on the bit error rate result. This allows easy optimisation of all the critical factors which effect the bit error rate within a system.

Measurements have been made on standard Plessey products versus competitive products. Without exception the Plessey SP97508 has peformed better than the competitive products at high analog input frequency and voltage. Ths is simply due to the higher input analog bandwidth of the Plessey device. This extra speed yields comparators that can regenerate their full output drive quickly. This in turn greatly reduces the probability of metastable states, and therefore reduces the bit error rate, under all conditions. When the mark-to-space ratio is adjusted to give a longer period for the input comparators to regenerate a full output, the bit error rate from the ADC is improved still further, in all devices (Plessey or others) evaluated so far. The optimum mark-to-space ratio for the SP97508 was found to be 7ns - 3ns.

We realise the effects of bit errors on systems such as digitised scopes, multi quadrant transmission systems, radar systems, video printers etc. It is hoped that this applications note will provide a quick and effective method, for the evaluation and comparison of this important device parameter.

An Example of a Subranging ADC System

The product information in this application note should not be used for new designs: it is included in this handbook since the design ideas presented are still valid.

LOW COST HIGH SPEED ADC

This application note outlines the use of the Plessey SP9000 series of high speed ECL circuits in a low cost flexible 8-bit analogue-to-digital converter.

The circuit provides 8 bits with a clock rate in excess of 20MHz and analogue bandwidth from DC to 10MHz.

FEATURES

- ECL
- Analogue Bandwidth DC to 10MHz
- Input Gain and Offset Controls
- Built in Sample and Hold System
- Low Cost
- Latched Outputs
- Low Power Dissipation 12W at ±12V
- Flexible Design can be tailored for Individual System Requirements
- Linearity ±½ LSB

APPLICATIONS

- TV Video Systems
- Computer Interface
- Radar
- Nucleonics
- Educational Experimentation
- Instrumentation

FUNCTIONAL DESCRIPTION (Fig.1)

The subranging, or series-parallel, technique has been known for many years in low speed A-D applications. With the introduction of the Plessey SP9754 100MHz 4-bit ADC, subranging techniques are practical at video speeds and above.

Subranging is a useful technique as it uses less power and components compared with the equivalent flash system. This is due to the economical use of comparators. For example, an all parallel 8-bit flash ADC uses 256 comparators. The subranging ADC described in this application note uses only 32 comparators to provide the same 8-bit parallel output as the flash converter.

The subranging system block diagram is shown in Fig.1. The analogue signal is first processed by the input buffer amplifier, then fed through a simple sample and hold system. This holds the input amplitude at a constant level for 25ns during conversion. The signal is then fed to the first SP9754 which is a latched device and due to this latch, SAH acquisition times can be slow; minimising the need for expensive circuitry.

On the positive edge of the clock the analogue signal is converted to a 4-bit code by the SP9754. This binary code is the most significant 4 bits of the 8-bit code, and is sent directly to the output latch. The least significant 4 bits are produced by first reconstructing the most significant bits into an analogue signal, using the Plessey SP9768 digital to analogue converter. This reconstructed analogue signal is subtracted from the original analogue signal by the SL541B. The result of this subtraction is a signal consisting of the remaining analogue corresponding to the least significant digital information. This is now converted to a 4-bit digital code and sent to the output latch as the least significant bits.

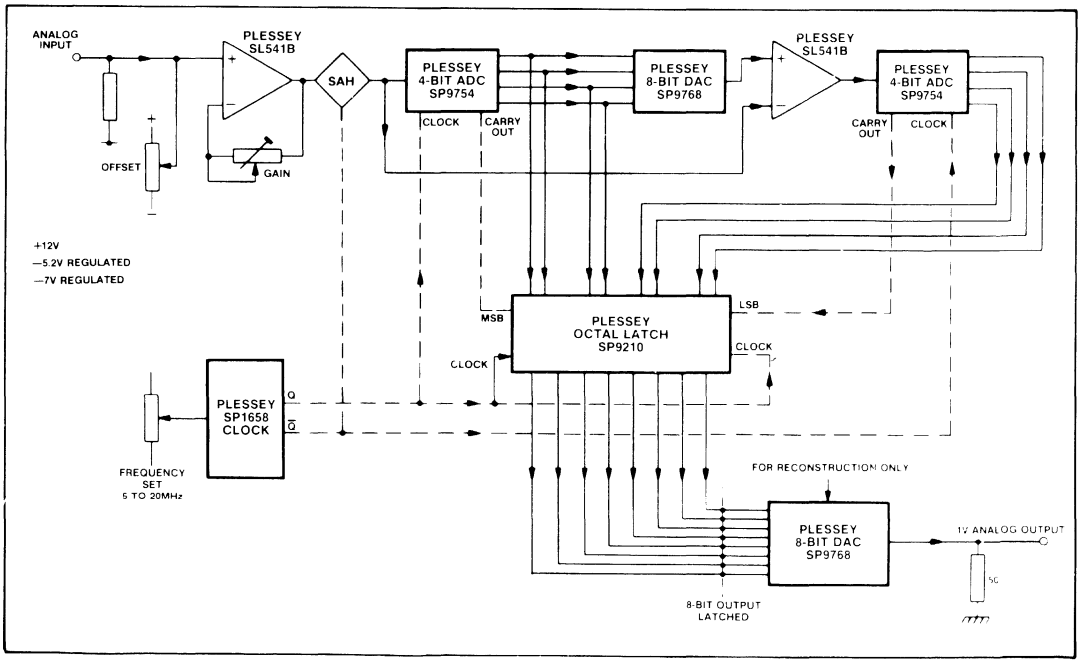


Fig.1 Block diagram of low cost 20MHz 8-bit A-D converter

The information is acquired by the latch at a point in time where the LSB and MSB codes are both valid. The resulting latched 8-bit ECL outputs are capable of driving 50 ohms to -2V and are valid for the complete clock cycle.

SYSTEM (Fig.2)

As with all ADC systems aliasing is evident at higher analogue frequencies. In practical systems this and also sinx/x frequency distortion are problems which can be corrected using anti-aliasing and interpolating filters. Suitable types are available from:

Electronic Techniques (Anglia) Ltd.,
Viking Works, Kirton, Nr. Ipswich,
Suffolk, England. Tel: 03 948 433.

A full system board layout is as shown in Fig.2.

THE TIMING DIAGRAM (Fig.3)

This diagram shows the arrangement of the ECL clock to each part of the circuit. The device chosen to provide the clock signal was the Plessey SP1658 voltage controlled multivibrator. This device gives Q and $\overline{Q}$ outputs which are both needed to drive the subranging A-D converter.

Four equal lengths of 100 ohm twisted pair were used. Two pairs connected to Q and the other two pairs connected to $\overline{Q}$. The Q outputs clock the first SP9754 and the output latches, the $\overline{Q}$ output clocks the second SP9754 and the sample and hold circuit. Fig.21 shows the clock layout.

The sample and hold circuit is used to hold the analogue voltage for 25ns, which is the 'on' time of the clock. This ensures that the LSB SP9754 at point B sees the same analogue voltage as the MSB SP9754 at point A.

This delay between the conversion of LSB's and MSB's is needed to allow for the propagation delays and settling times of the SP9768 D-A converter, the latch to output delay of the MSB SP9754 and also the propagation delay and settling time of the SL541B.

The output latch SP9210 is driven from the Q output and works in master slave fashion. The data is acquired by the latch on the rising edge of the clock point C on the timing diagram. At point C the MSBs are still valid. The output of the latch now gives continually valid information with no timeskew between MSBs and LSBs.

Why 20MHz Clock

Although the SP9754s are capable of conversion at 100MHz, the total system speed is limited by the time taken to convert the MSBs back to an analogue signal, and also the time taken to subtract the original analogue from the reconstructed analogue. The LSB SP9754 cannot convert until these delays and settling times are complete. The measured times are as follows:

Latch to output delays MSB SP9754 = 9ns
Settling time and propagation delay SP9768 D-A = 3.5ns
SL541B Op amp propagation delay and settling time = 7.5ns

Total delay before the LSB SP9754 can convert is therefore 20ns, this gives a maximum clock frequency of 25MHz. Due to component tolerances and possible temperature drifts a safe maximum clock rate of 20MHz is advised for the system described here. It is this high speed and low propagation delays of the Plessey SP9754 and SP9768 that make this technique feasible for video speeds and above.

THE CIRCUIT DIAGRAM (Fig.4)

The Input Op-Amp

This Op-Amp is not part of the ADC itself but provides easy interface for the user. The Plessey SL541B is a high speed low cost device suitable for video signals.

Resistors R1, R2 provide the termination impedance for the analogue signal.

V1 and R4 provide an offset control. This allows the user to interface with signals DC offset positively or negatively. The offset control can be set to higher or lower ranges by re-positioning the range link. This link connects to +5V, 0V or +12V. The +5V position gives a suitable range for most standard video signals.

A gain control is provided by the variable resistor V2 in the feedback loop of the Op-Amp.

The Sample and Hold

Sample and Hold systems can be an expensive problem in A-D conversion due to the high acquisition rates needed. On the other hand with the SP9754 circuit, Sample And Hold can be made at low cost. The reason for this is that the SP9754 works in master slave fashion by latching the comparators when the clock is high. This is in itself a sample and hold system. We still need an external sample and hold due to the time taken to process the LSBs. As the SP9754 latches the input analogue signal at high speed the external sample and hold can have a slow acquisition time and can be driven directly from the clock pulse.

R11 and R12 provide an ECL termination at 100 ohms for the sample and hold clock.

The clock is then AC coupled into the primary of a mini circuits T5-IT impedance matcher. Hand wound transformers can be used here, but beware! The design is very critical. The cost of the mini circuits matcher is about £9.10 for 1 off and £3.80 for 10 to 49 off (24 September 82/UK) and perform very well in sample and hold applications.

The transformer secondary drives a diode ring through a current limiting resistor R10. Good quality signal diodes were first tried for the ring, but the analogue bandwidth was affected, so high speed Schottky diode were used. This gave no apparent degradation in analogue bandwidth.

The clock pulse is amplified by the transformer and switches the diode ring on, this connects the input Op-Amp to the storage capacitor C1 through R7. When the clock changes state the diode ring will go open circuit leaving the analogue level held constant on C1. It is in this steady state condition that the subtraction and LSB acquisition takes place.

The A-D

Transistors TR1 and TR2 provide the current to drive the Plessey SL541B which subtracts the signals. The sample and hold analogue signal is now fed to the MSB SP9754.

TR3 is used to provide the reference voltage for the internal reference chain of the SP9754. This voltage can be adjusted by V3 and should be 1.5V at pin 17 of the SP9754. This reference voltage must be very clean, free from digital and analogue noise. C2, C4 and a 10nF capacitor are used to decouple the reference voltage over a wide frequency range. R16 protects the tantalum from destruction by turn on transience and also generates a time constant with C4. The diode D1 is used to reduce the drift with temperature of the base emitter junction of TR3.

R20 and R21 are used to ECL terminate the clock at 100 ohms and -2V.

The 4-bit code from this device is fed to the SP9768 and the Plessey octal latch SP9210. At the SP9768 the 4-bit code is converted back to an analogue signal at TP2. V5 adjusts the amplitude of this analogue signal and R22 improves the noise immunity of the device by tying unused inputs low.

The analogue signal from this digital to analogue converter and the analogue signal from the sample and hold are subtracted by the SL541B Op-Amp. The external components have been arranged to provide subtraction of the DC and AC signals giving operation down to DC.

V5 is adjusted to give the same amplitude output from the D-A converter as the output from the sample and hold, which is 1.5V pk-pk. V4 will adjust the DC offset at the Op-Amp output and should be adjusted until the output sits from 0 to about 0.5V. This output level is fixed by the gain set resistors R48, R9 and R26.

R23 is the coarse setting resistor for V4. The slew rate of

this Op-Amp is further improved by R25 and C7. R25 reduces the open loop gain enabling C7 to peak the response.

The subtracted analogue signal is now converted to the LSB data by SP9754(No.2). TR4 and surrounding components provide a smoothed adjustable DC reference for pin 17 of SP9754(No.2) in the same manner as TR3 for pin 17 of SP9754(No.1).

R30 to R37 are pull down resistors for the SP9754 outputs. The 8-bit digital information is then fed into a Plessey SP9210 master slave ECL latch. This latch is clocked by a Q phase clock giving valid data for the full clock cycle. Carry pulses from the SP9754s are connected to the output latch to prevent the codes resetting to zero in any overflow condition.

The final 8-bit output from the latch is ECL and must be terminated to -2V with lines terminated with their characteristic impedance.

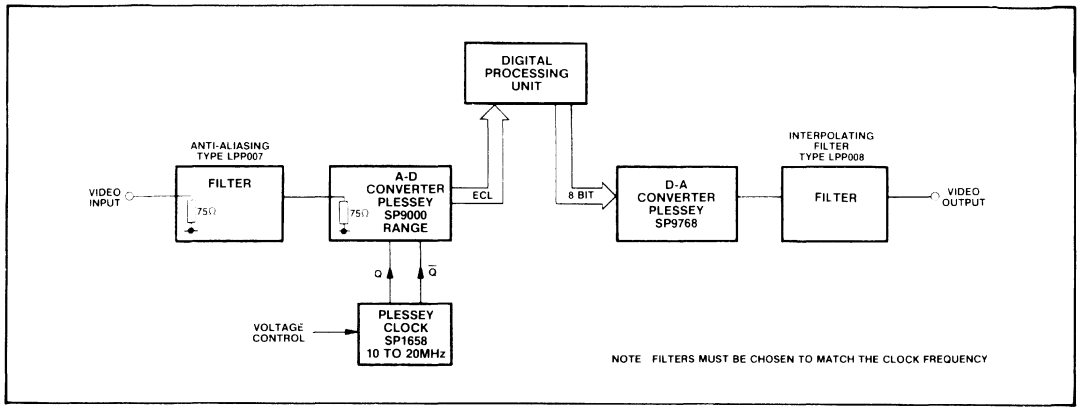


Fig.2 Block diagram of a full system board layout

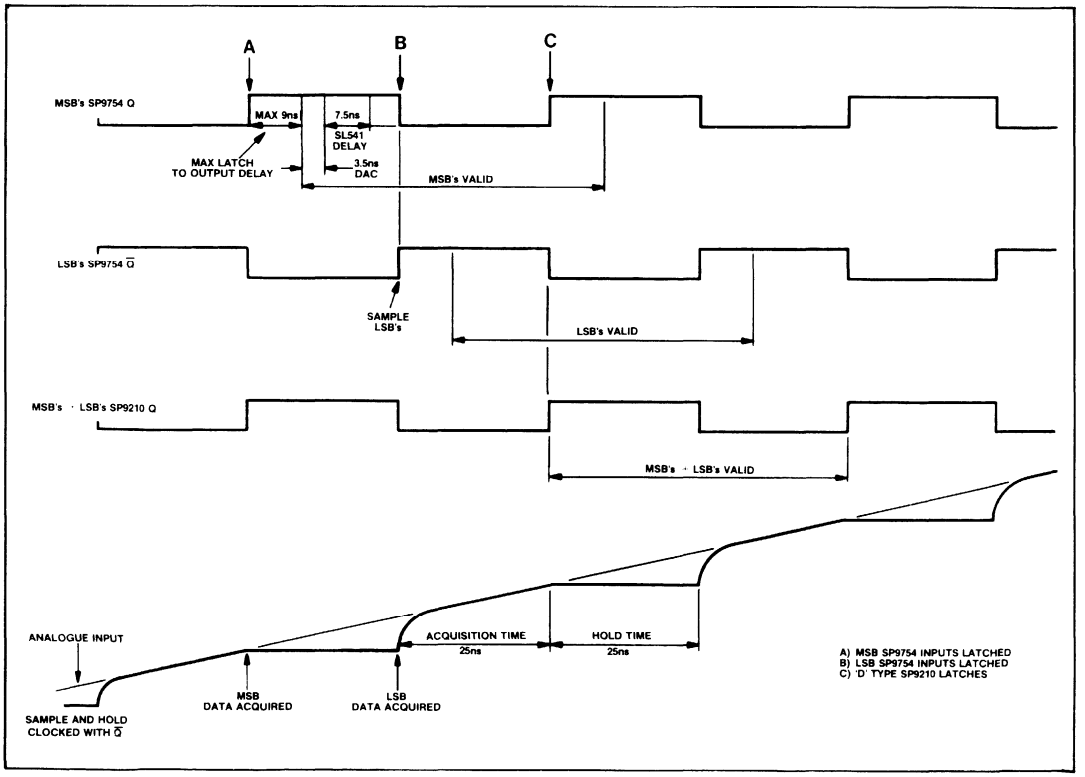


Fig.3 Timing diagram for 20MHz clock

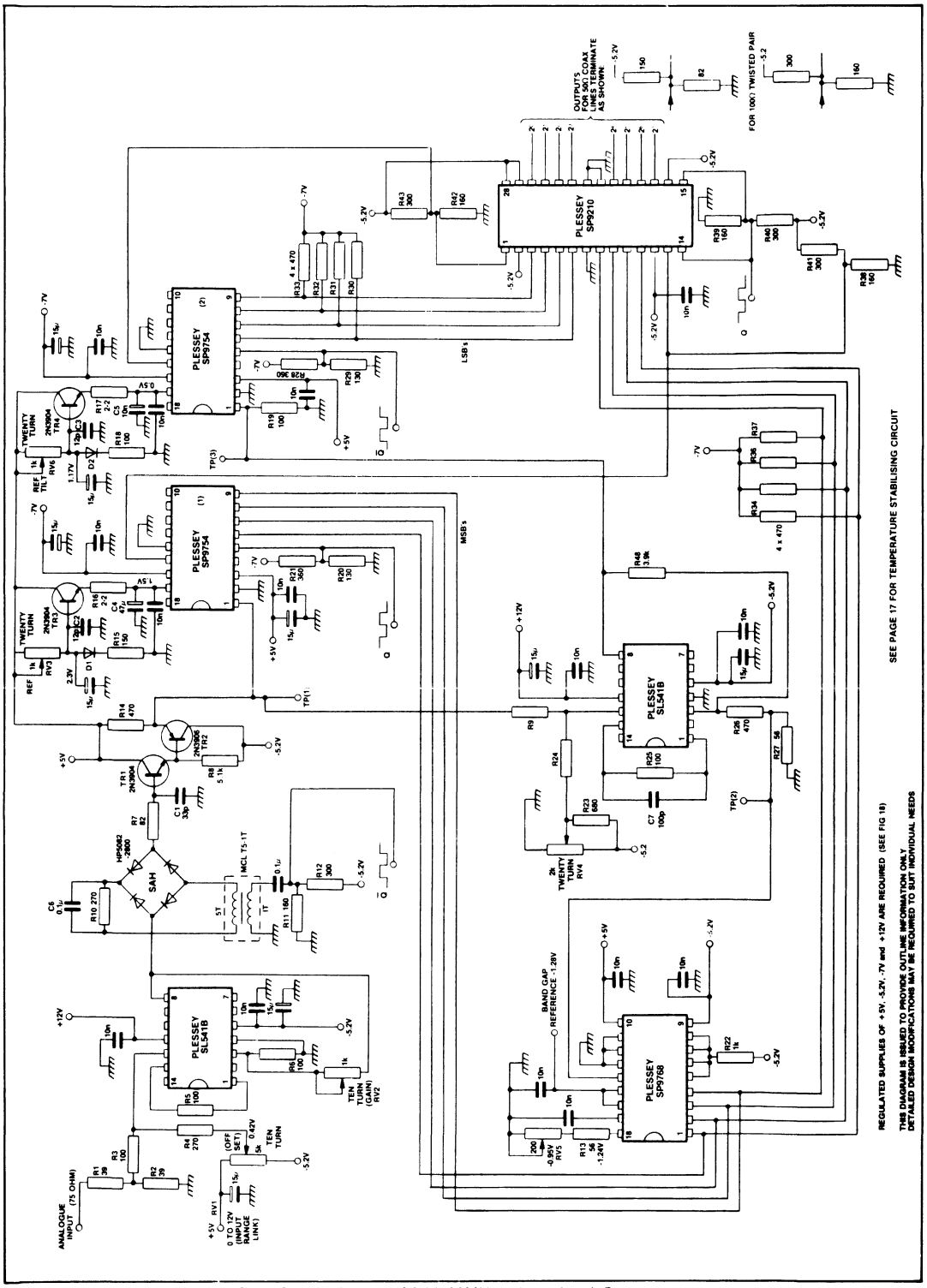


Fig.4 Circuit diagram of 8-bit 20MHz subranging A-D converter

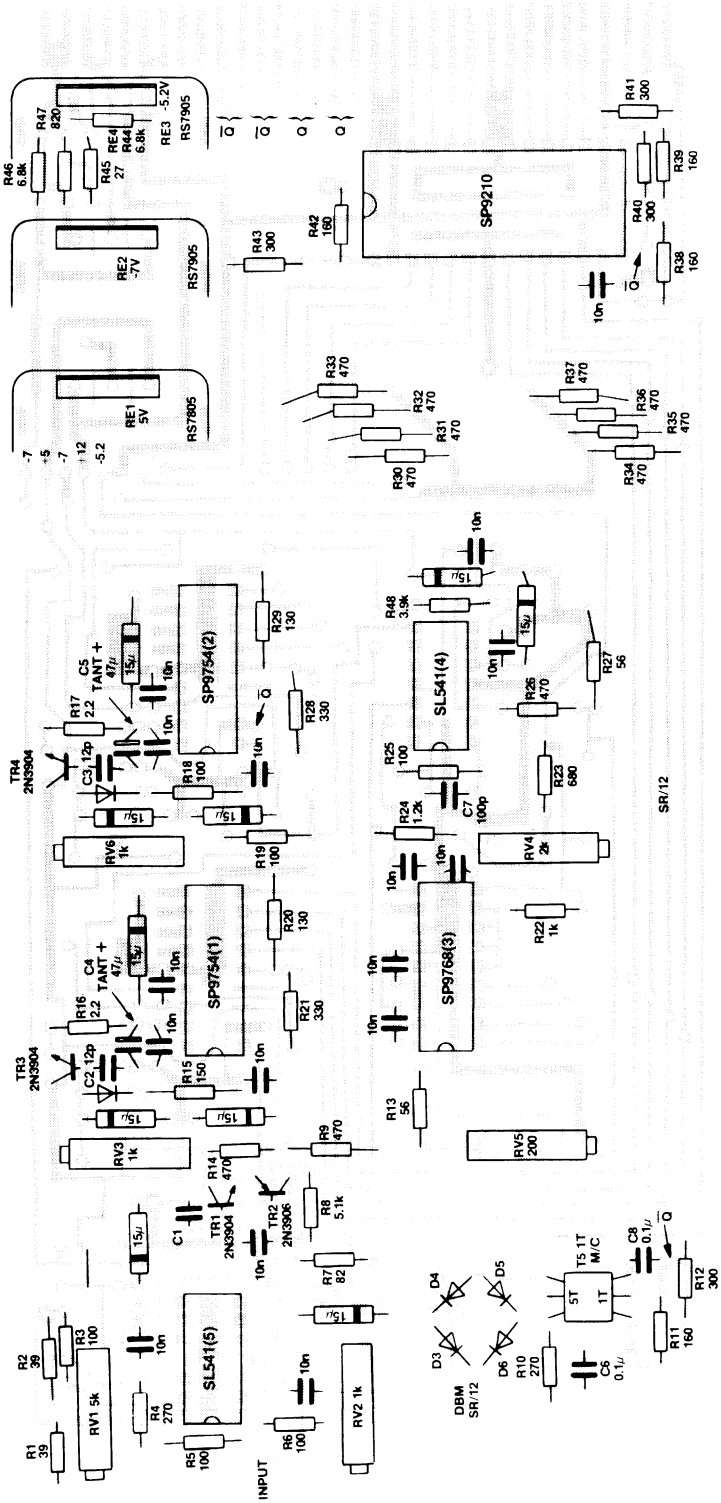


Fig.5 Component layout for A-D converter

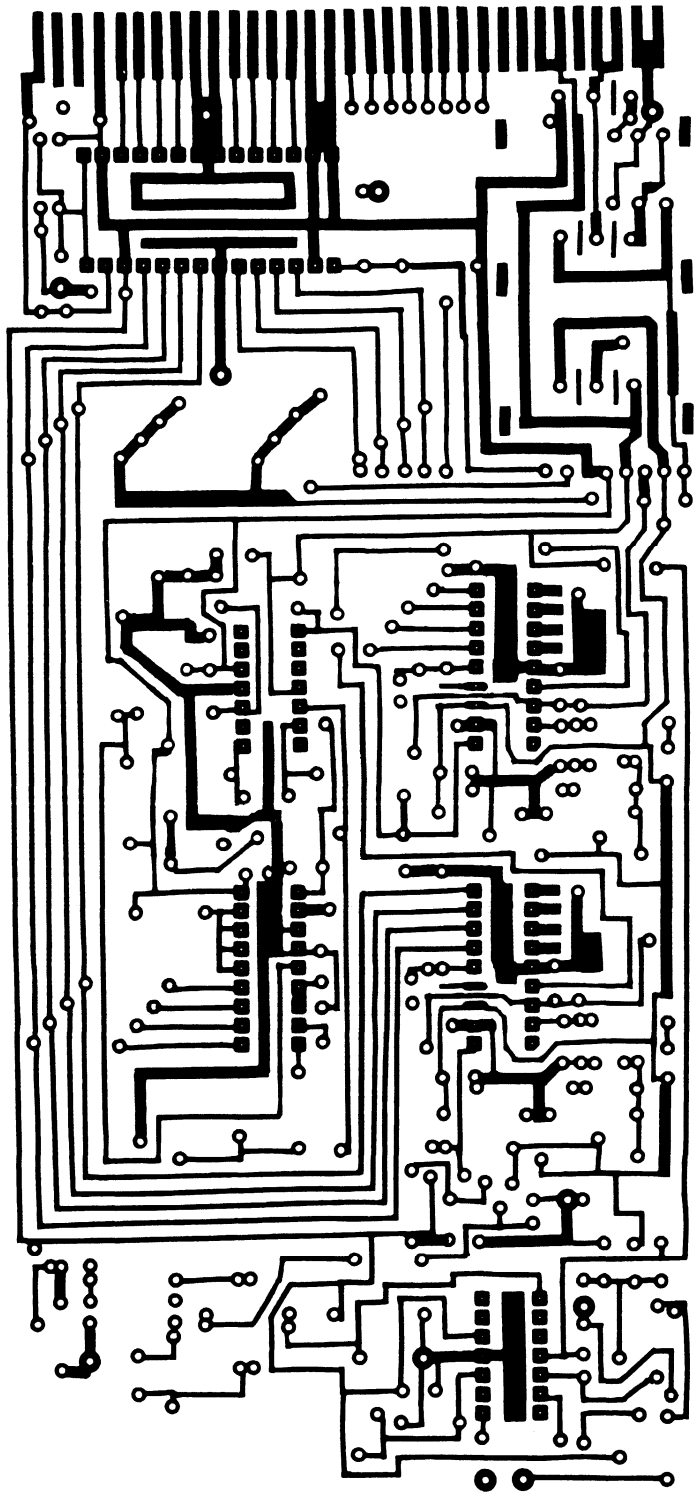


Fig.6 PCB layout of A-D converter

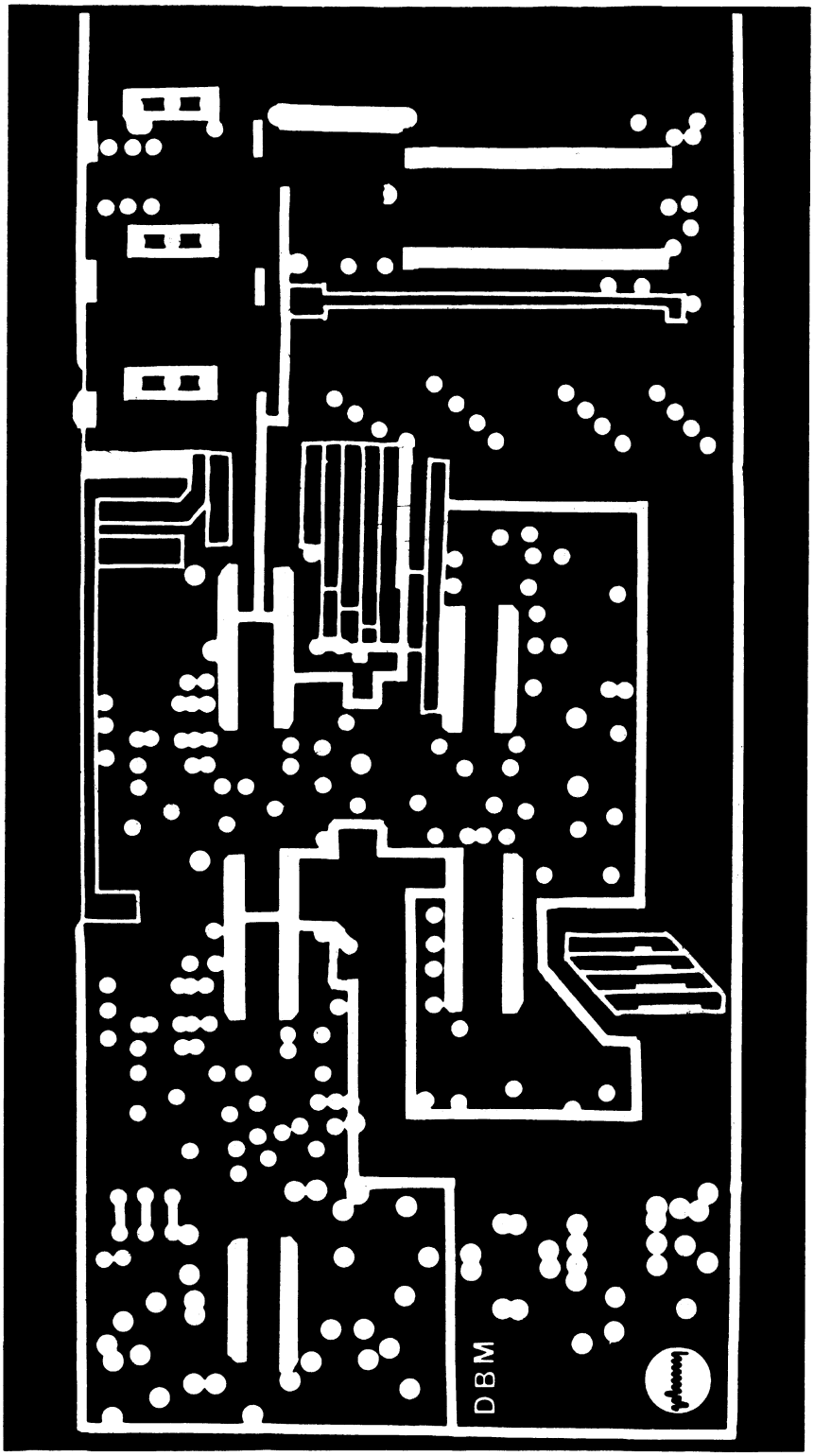


Fig.7 Ground plane for PCB of A-D converter

2 % RESISTORS (Ω)

R1	39
R2	39
R3	100
R4	270
R5	100
R6	100
R7	82
R8	5.1k
R9	470
R10	270
R11	160
R12	300
R13	56
R14	470
R15	150
R16	2.2
R17	2.2
R18	100
R19	100
R20	130
R21	330
R22	1k
R23	680
R24	1.2k
R25	100
R26	470
R27	56
R28	330
R29	130
R30 – R37	470
R38	160
R39	160
R40	300
R41	300
R42	160
R43	300
R44	6.8k POWER SUPPLY
R45	27 POWER SUPPLY
R46	6.8k POWER SUPPLY
R47	820 POWER SUPPLY
R48	3.9k

CAPACITORS

C1	33pF
C2	12pF
C3	12pF
C4	47μF TANT.
C5	47μF TANT.
C6	.1μF
C7	100pF
C8	.1μF
C9 – C25	10nF
C26 – C36	15μF 16V

REGULATORS (IF NECESSARY)

RE1	RS7805
RE2	RS7905
RE3	RS7805

(WITH HEAT SINK KIT RS401-863)

INTEGRATED CIRCUITS PLESSEY

IC1	SP9754DC
IC2	SP9754DC
IC3	SP9768DC
IC4	SL541BDG
IC5	SL541BDG
IC6	SP9210DG

TRANSISTORS

TR1	2N3904
TR2	2N3906
TR3	2N3904
TR4	2N3904

DIODES

D1, D2: CHOOSE FOR GOOD MATCH WITH TR3 AND TR4

D3 – D6: HP5082-2082

IF POSSIBLE MATCHED SCHOTTKY DIODES

TRANSFORMER MINI-CIRCUITS T5 1T

DALE ELECTRONICS LTD.
DALE HOUSE, WHARF ROAD
FRIMLEY GREEN
CAMBERLEY, SURREY
TEL: 02516 5094

CERMET TRIMMER 20 TURN POTS

RV1	5k
RV2	1k
RV3	1k
RV4	2k
RV5	200
RV6	1k

Table 1 Component list for A-D converter

NOTE
The above component list does not include components for the Plessey SP1658 Q-$\bar{Q}$ clock or the other Plessey SP9768 D-A converter used to reconstruct the digital data. See Fig.21 and Fig.22.

RECONSTRUCTION OF THE DIGITAL CODE

In a great number of applications the digital code must be reconstructed into an analogue signal, after transmission or computing has been performed. The digital to analogue converter described earlier in this article is ideally suited to this purpose. A board with adequate termination for 100 ohm twisted pair ribbon cable (Rs 358-D40) is shown in Fig.22.

The final analogue output will be DC biased below ground. The amplitude of the analogue output can be controlled by the current into pin 18 of the SP9768 to a maximum of 1.3 volts. The output can be inverted by exchanging pins 14 and 13.

Setting Up The A-D Converter

1. Before powering up set RV1 to RV6 mid-range.
2. Connect Q and $\bar{Q}$ clock inputs and set to 20MHz.
3. Connect SP9768 8-bit D-A converter.

Coarse Settings

1. Set RV3 for 1.5V at pin 17 of SP9754(1).
2. Set RV6 for 0.5V at pin 17 of SP9754(2).
3. Set RV5 for -1.37V at pin 18 of SP9768(1).
4. Set RV4 for -4.55V at wiper of V4.

Fine Settings

1. Set a triangular wave at the input with a similar amplitude and offset as the analogue signal eventually to be used. Set RV2 (gain) and RV1 (offset) for signal levels as below Fig.8 at TP(1). If this signal level cannot be met, RV1 can be connected to 12V or 0V by changing the link.
2. With scope at TP(3) set RV5 for a flat signal as Fig.9.
3. Adjust RV4 to sit signal at 0V as Fig.9. Note RV5 and RV4 interact and some iteration may be needed.

Reconstructed Signal (Fig.11)

The reconstructed signal should now be expanded to show individual steps. At intervals of 16 steps low energy subranging errors may be seen, adjust RV6 (subranging tilt) and RV4 (subranging offset) for 'Best Fit' at all subranging points.

NOTE: If it is not possible to set good linearity over the full voltage range examine TP(3) for flat waveform, adjusting RV5 if incorrect.

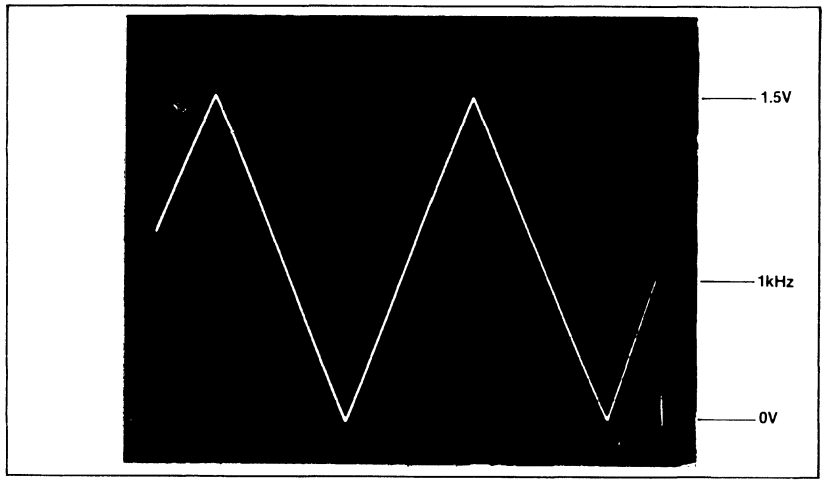


Fig.8 Test waveform at first SP9754 input TP(1)

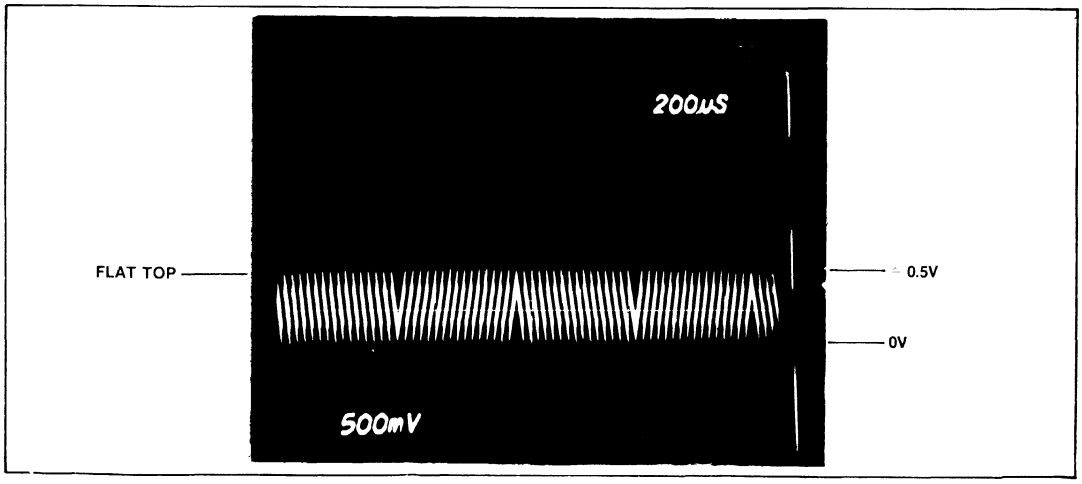


Fig.9 Test waveform at second SP9754 input TP(3)

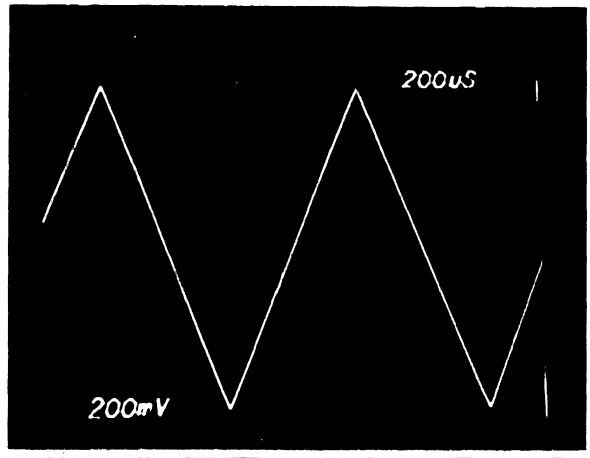


Fig.10 A triangular wave which has been digitised by the subranging method then reconstructed by the SP9768 D-A converter

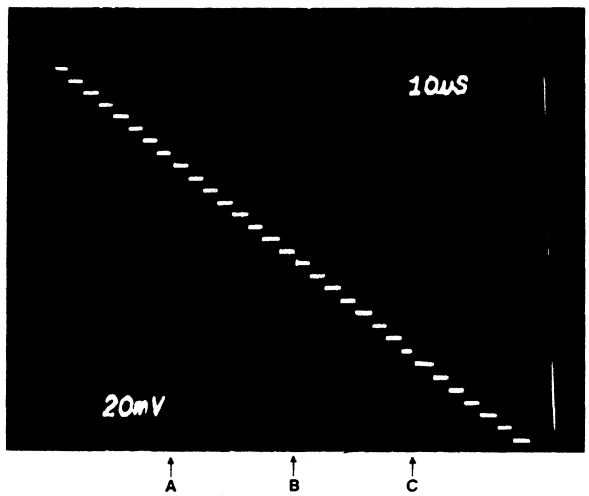


Fig.11 Expanded view at the zero crossing of the triangular waveform. 'B' is the typical error at the zero crossing, 'A' and 'C' are typical errors at the subranging points (no filters in circuit).

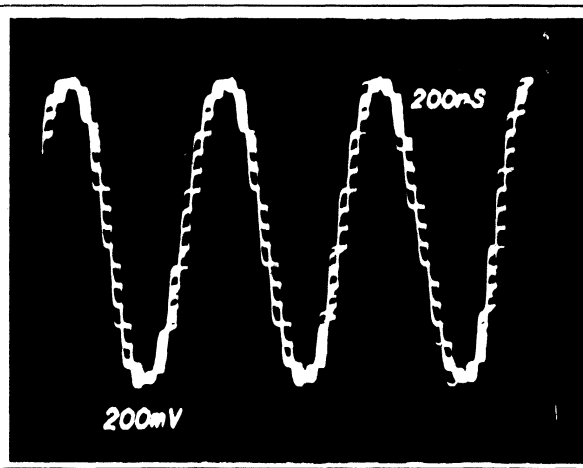


Fig.12 Sinewave at high analogue frequency (no filtering)

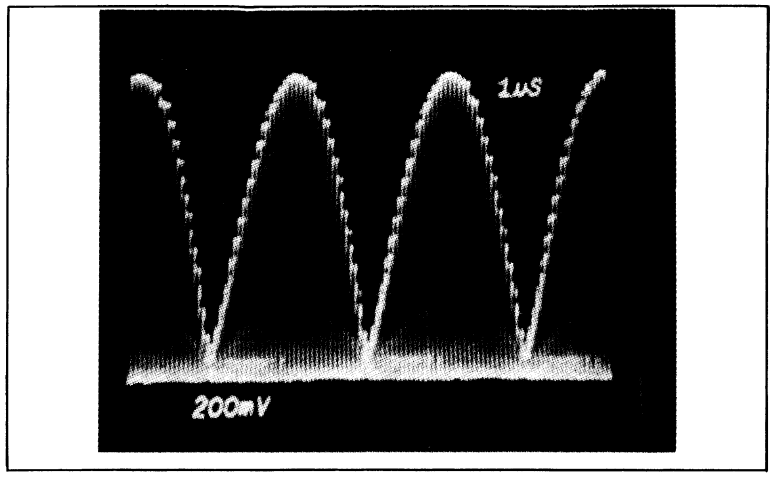


Fig.13 Half sinewave beat at near Nyquist analogue frequency

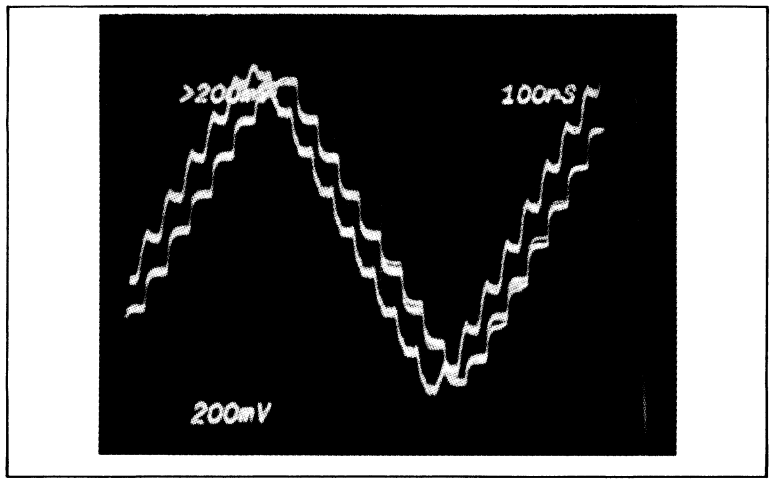


Fig.14 Propagation delay from the output of the sample and hold to the final reconstructed analogue output (53ns)

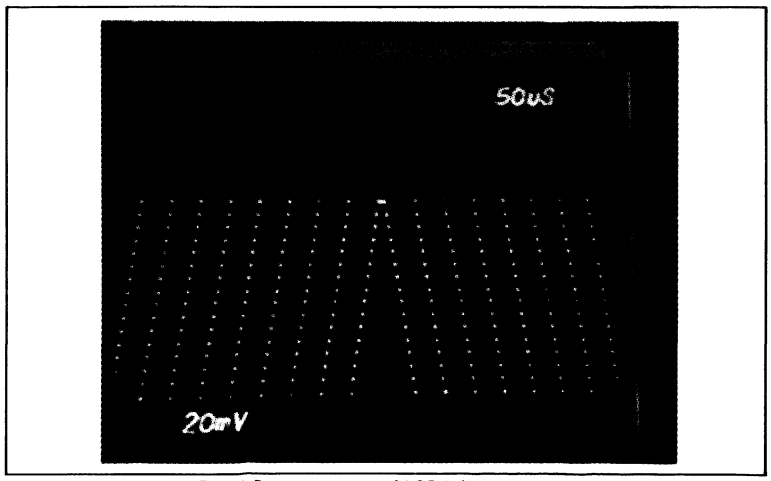


Fig.15 Reconstruction of LSB information only

Fig.16 An off-air TV picture which has been digitised, then reconstructed to 8-bit resolution. A full colour picture with no degradation in picture quality can be seen using a colour monitor.

Fig.17 An off-air TV picture which has been digitised, then reconstructed to 3-bit resolution. The coarse digitisation of the signal produces a recognisable picture but all fine detail is missing.

LOW COST POWER SUPPLIES

Fig.18 shows the power supply circuits to obtain regulated +5V, -5.2V and -7V from ±12V supplies. ±15V can be used if the subranging ADC has been aligned at this supply voltage.

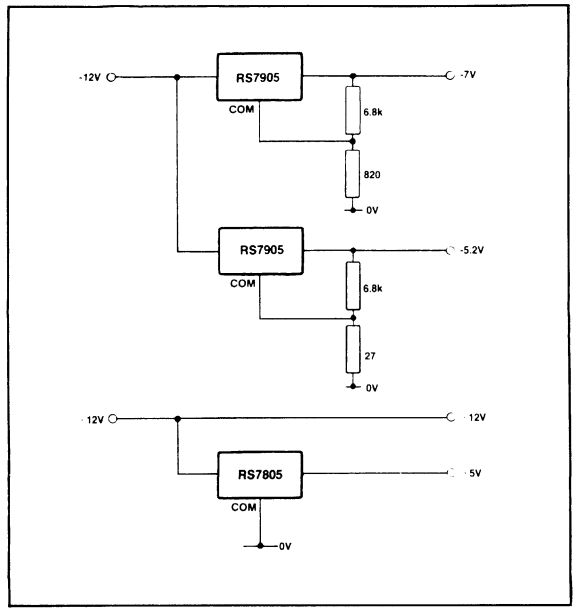


Fig.18 Power supply circuit

SUBRANGING - BOARD CHARACTERISTICS

Characteristic	Typ.Value	Units	Conditions
Power supply	±12	V	With regulators
Number of bits	8		
Supply current	940	mA	
Max. clock frequency	20	MHz	
Analogue bandwidth	DC to 10	MHz	
Input voltage levels	0.5 to 3	V	With input op-amp
Input impedance	75	Ω	With R1 = 39, R2 = 39, R3 = 100
Output voltage	ECL		
Output drive	50	Ω	Minimum (to -2V)
Best fit straight line linearity	±½	LSB	After thermal stability has been reached
Propagation delay	53.5	ns	From SAH output to reconstructed analogue

Table 2 Board characteristics

BOARD CONSTRUCTION

Although the use of a double sided PCB with plated-through holdes would be ideal, a double sided board with through holes is practical where small quantities are involved. Good quality low-profile sockets can be used for all integrated circuits. The layout has been specifically designed to keep analogue and digital ground planes separate at critical points. A 0.1 inch pitch edge connector is used.

ECL CLOCK SP1658

This small ECL clock circuit provides the Q and $\overline{Q}$ outputs necessary to drive the subranging ADC. It should be connected using 100 ohm twisted pair. The clock frequency is voltage controlled by RV1 and can be connected to phase locked loop circuits.

The -5.2V supply can be taken from the subranging ADC board.

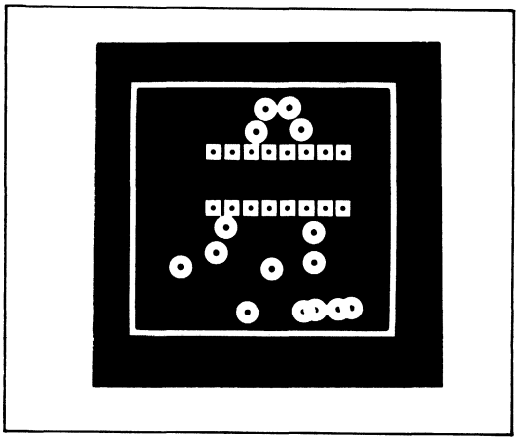


Fig.19 ECL clock PCB ground plane from component side

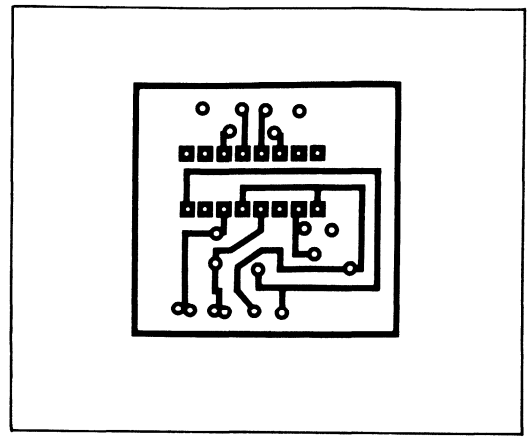
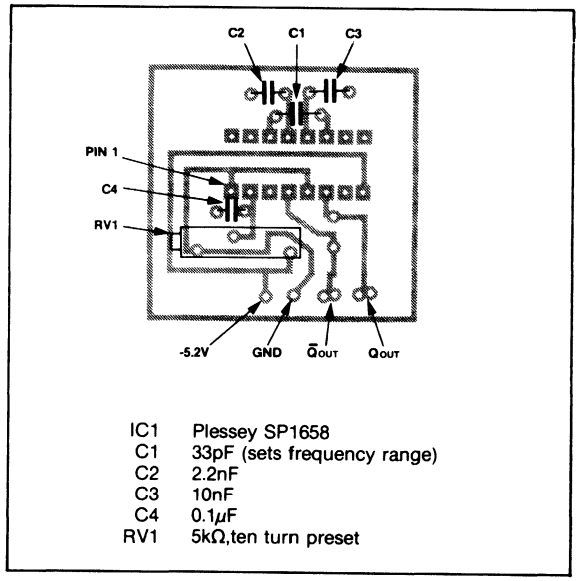
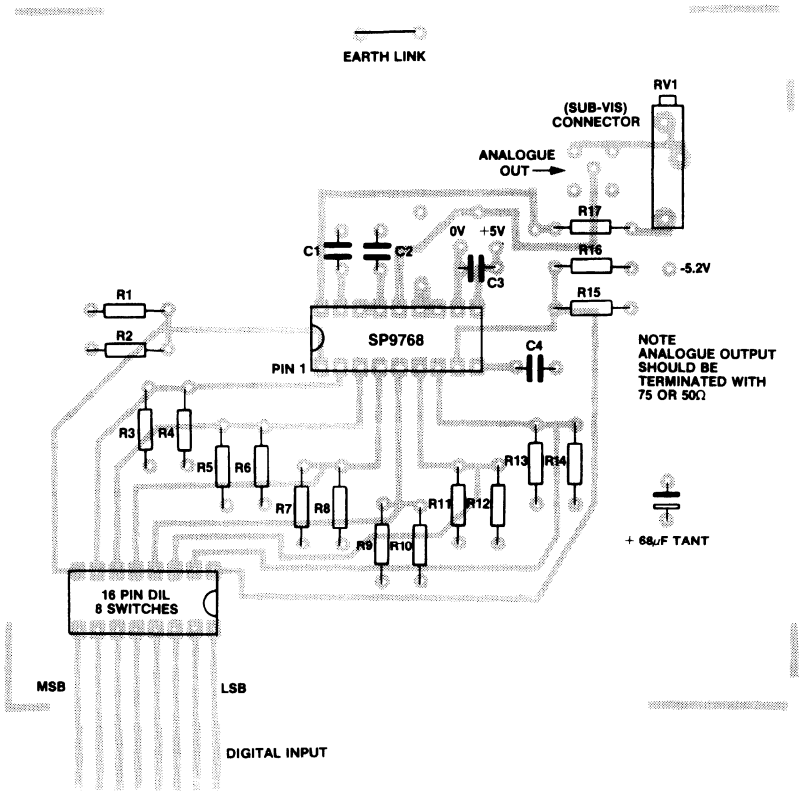


Fig.20 ECL clock PCB track layout from copper side



IC1	Plessey SP1658
C1	33pF (sets frequency range)
C2	2.2nF
C3	10nF
C4	0.1μF
RV1	5kΩ,ten turn preset

Fig.21 ECL clock component layout



R1,R4,R5,R8,R9,R12,R14,R16 160Ω
R2,R3,R6,R7,R10,R11,R13,R15 270Ω
R17 150Ω
RV1 1kΩ
C1,C2,C3,C4 10nF
C6 68μF, tantalum
IC1 SP9768
16-pin DIL 8 SPST switch package
Sub-vis connector
Note: Plated-through holes should be used

Fig.22 SP9768 DAC component layout, 100Ω system

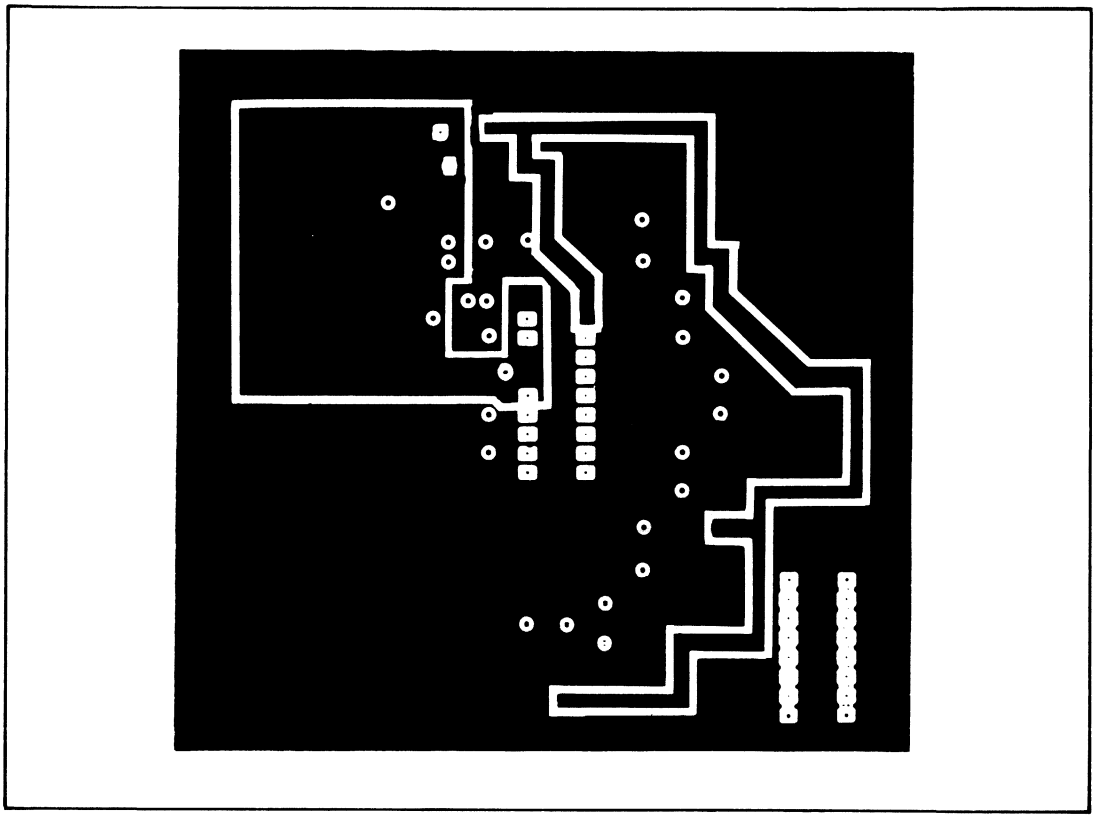


Fig.23 SP9768 DAC ground plane from component side

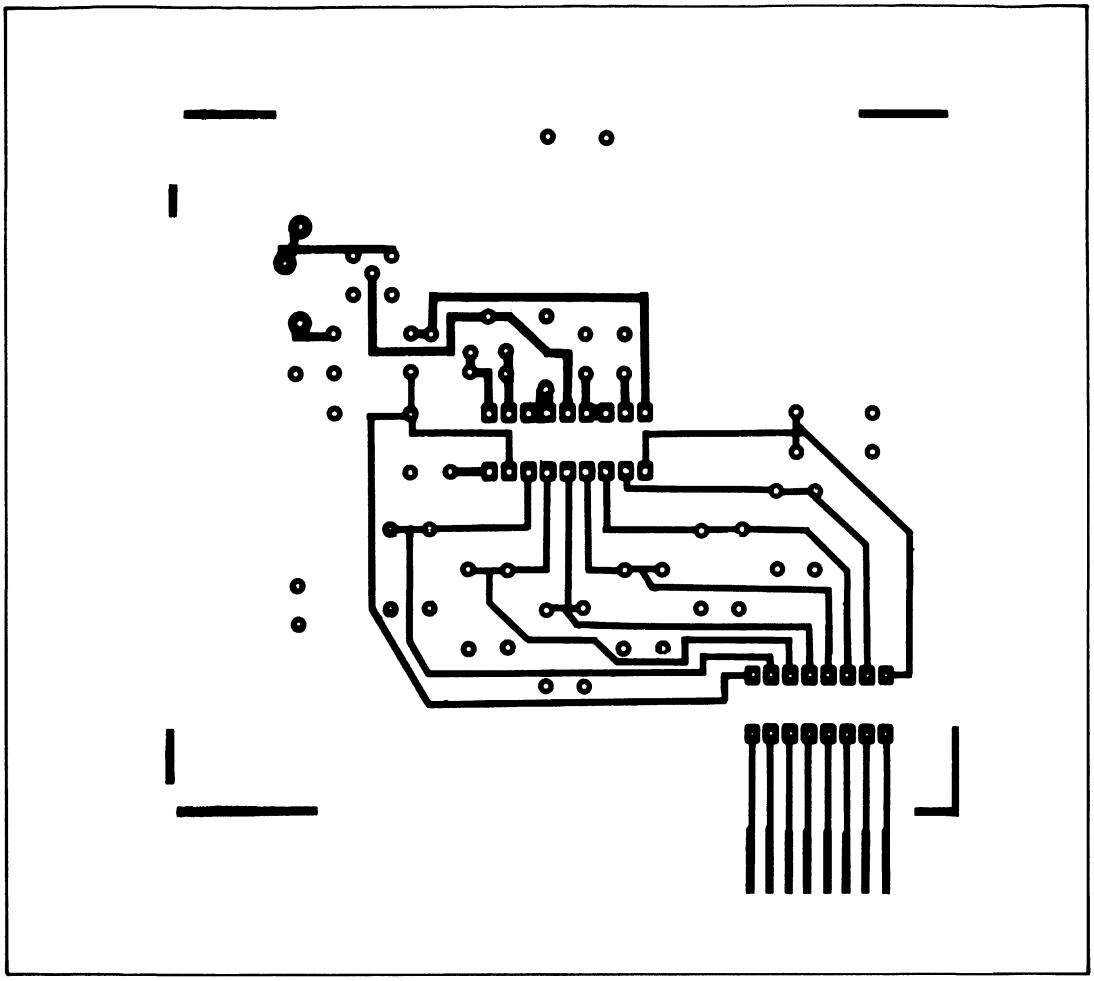


Fig.24 SP9768 DAC PCB track layout from copper side

TAILORING THE SUBRANGING SYSTEM

Thermal Stability

As the Plessey SP9768 has a bandgap reference voltage output, thermal stability can be improved using this reference (-1.28V), and an op-amp to define the reference voltage at pin 17 of the first SP9754 in the system. The second converter can be referenced in the same manner if necessary.

Error Correction

Error correction can be applied to this system by the use of two SP9754s in parallel to provide a 5-bit converter for the LSBs. The fifth bit can then be used to error-correct the MSBs.

Auto Drift Correction

For systems that do not need full operation down to DC, the setting of RV4 can be eliminated and stability improved by detecting the negative peaks of the subtracted analogue signal and applying this signal as feedback to the top of R23.

Analogue Bandwidth

Analogue bandwidth can be improved by using very high speed Schottky dioded in the diode ring of the sample and hold system.

Noise Improvement

The quantisation noise floor of conventional 8-bit systems can be as low as 49.9dBs. Some improvements in quantisation noise performance can be gained by the addition of a high frequency jitter signal to pin 3 of the first SL541 in the system. The improvement is obtained due to the comparators in the ADC being switched regularly at high speed, and so effectively moving some of the quantisation noise out of band. This technique is used by the IBA in some of their digital signal processing systems. In the A-D described in this application note a jitter signal of 10MHz was found to be optimum.

System Speed

Improvements in speed can be made to the subranging technique by removal of the sample and hold and adding delays to accurately 'pipeline' the system. The pipelined system must be very accurately timed as small errors would cause large subranging glitches. System speeds of 60 to 90MHz may be obtained using such techniques.

Glitch Energy

In some subranging systems glitch energy is noticeable at subranging points (every sixteenth step). Improvements can be made by the use of a very high slew-rate op-amp as the subtracting element in the system, unfortunately, such devices are more expensive than the Plessey SL541 used in the system described in this article.

FLASH TECHNIQUE

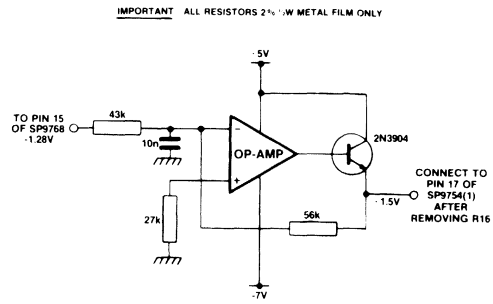
The SP9754 is ideal for stacking in flash format. Using 16 devices and supporting circuits a high performance 80MHz system can be realised.

Other Useful Plessey ECL Components for High Speed Data Processing	
SP9685	Ultra fast comparator (2.2ns)
SP9687	Ultra fast dual comparator with latch (2.2ns)
SP9680	Ultra fast comparator in low cost 8-bit pin package (2.4ns)
SP9131	550MHz dual 'D' type master slave flip flop

ACKNOWLEDGEMENTS
G.M. DRURY AND I. LEVER VIDEO AND COLOUR DEPARTMENT (I.B.A.)
V.DEVEREAUEX RESEARCH DEPARTMENT (B.B.C.)

IMPROVING THERMAL STABILITY

Thermal stability can be improved by the addition of an op-amp to accurately control the reference voltage of the first SP9754 in the system. The accurate reference voltage is provided by the band-gap reference from pin 15 of the SP9768.



A Complete 100MHz A/D-D/A Evaluation System

The Plessey AP9001 evaluation board is a complete 6 bit 100MHz A to D system. The resulting low external component count can be seen easily when comparing the SP9756 with other solutions. The reduction in external component count is possible because the device includes a clock driver stage, band gap reference, output D-type latch and a reference chain.

Each individual application of the ADC may require different optimisation of parameters; this board has been designed in a general manner, yet little else should be required to meet even the most precise 100MHz systems.

The Plessey SP9756 is a 6-bit flash ECL analog-to-digital converter. It incorporates 64 individual comparators, a clock driver circuit, reference chain and a D-type output latch. This flash ADC is capable of sampling in excess of 110MHz, with a wide analog bandwidth and good dynamic performance.

A choice of accuracy is available: the accuracy of the SP9756-8 is typically ±⅛ LSB at 2V input and therefore it is ideally suited for use in systems that incorporate expansion to higher resolutions. Alternatively the SP9756-6 is guaranteed to be accurate to ±½ LSB for inputs between 1V and 2V in cost conscious designs.

An SP9756 data sheet is included at the end of this application note.

THE EVALUATION SYSTEM - AP9003

Included in the evaluation system are:- ADC board (Fig.1), a length of 100Ω twisted pair and the SP9768 DAC applications board (Fig.2). The twisted pair shows the effectiveness of the SP9756 output latch and enables the user to interface easily with other digital circuitry. The D-A evaluation board provides a simple method of evaluating the all-important analog bandwidth performance of the ADC. It is suggested that, near Nyquist - and even near clock - beats are viewed at 100MHz sample to demonstrate the wide analog bandwidth of the SP9756 (see Figs. 14, 15 and 16).

The ADC board (AP9001) comprises one SP9756 (6-bit ADC), one TAB1042 (quad op.amp), one SP9687 (dual comparator) and one RS7805 5V regulator.

Evaluation Boards

In general, the performance of a high speed ADC can be greatly affected by the circuit board ground plane layout and associated component placements. Plessey Semiconductors are therefore prepared to make available for purchase small quantities of completed ADC and DAC boards with connecting loom, for evaluation and educational use. The items listed can be ordered from our customer service department.

Item	Description
AP9001	Complete ADC board and data
AP9002	Complete DAC board and data
AP9003	Complete ADC, DAC and connecting loom with data (recommended system)

Evaluation systems available from Plessey Semiconductors

Power Supplies

The evaluation system requires external -5.2V and ±12V supplies. A +5V supply is also required but this is provided from the +12V by an RS7805 regulator. For convenience all power supplies have been taken through the edge connector to supply the DAC evaluation board.

Supply	AP9001 ADC board	AP9003 ADC & DAC system
-5.2V	240mA	660mA
+12V	90mA	90mA
-12V	90mA	90mA

Table 1 Power supply currents

The current taken from the -5.2V supply increases to 660mA when the DAC board is connected, due to the extra current taken by the line termination and device supplies.

Analog Input to the Board

The analog input is fed directly to the SP9756 and is terminated by R14 = 47Ω. Socket pins are provided for AC or DC coupling. An offset can be applied by varying RV2 (see Fig.3).

The source impedance should be 25Ω, certainly no higher than 50Ω (see Fig.4 for device input impedance).

Ideally the reference should be set to accept an analog input of 2V p-p with its center offset by -1V. The range of this offset is approximately +1V to -1.2V.

Clock Input to the Board (Fig.5)

The SP9756 has an on-chip differential clock driver which allows the device to be driven directly from an ECL source. To aid interfacing to the applications board a comparator has been added. This allows a sinewave oscillator to be used to clock the device. An offset provided by RV4 can be adjusted for AC-coupled inputs or adjusted for an input trip level of -1.28V for ECL signals.

RV4 can also be used with a DC-coupled sinewave input to vary mark/space ratios when experimenting at clock frequencies above 130MHz.

A signal generator with low frequency jitter should be used that is capable of driving the board's 50Ω termination.

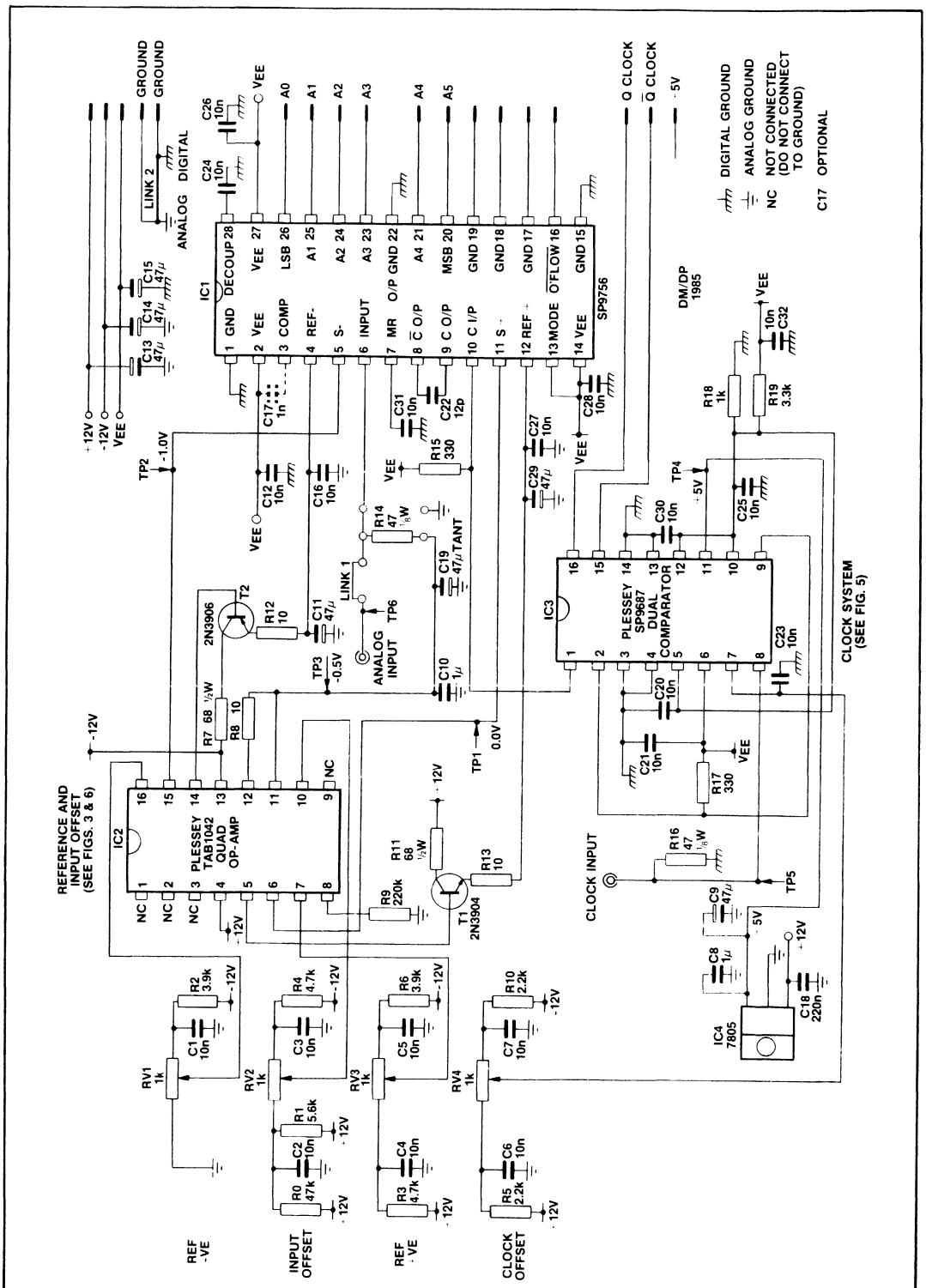


Fig.1 Plessey SP9756 100MHz 6-bit ADC evaluation board - AP9001

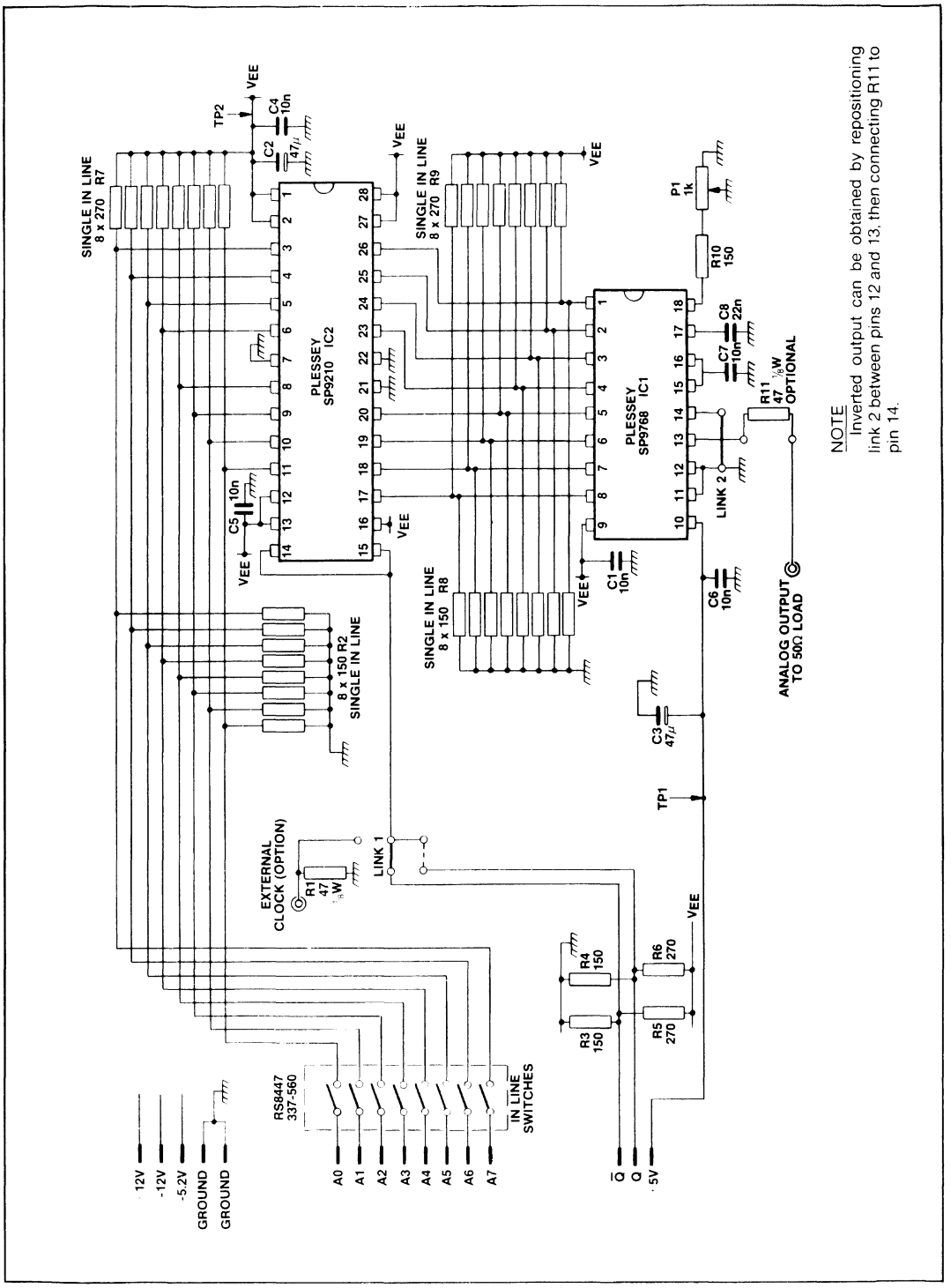


Fig.2 Plessey SP9768 8-bit DAC board - AP9002

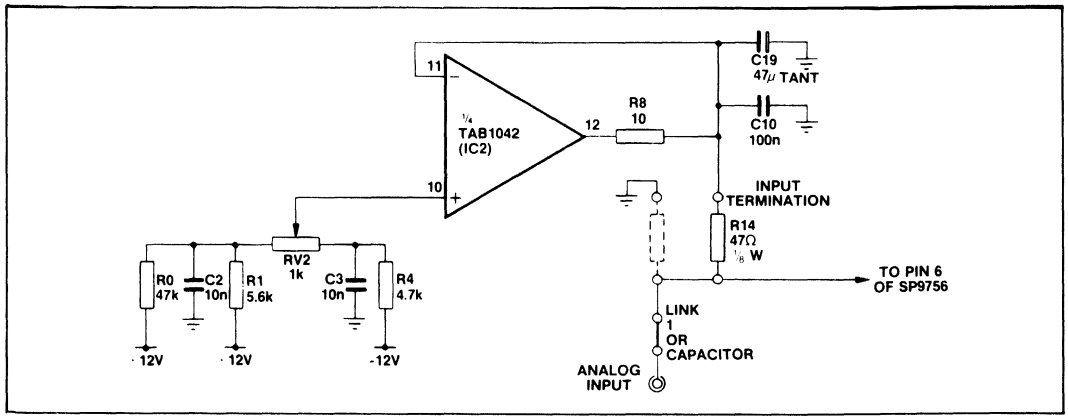


Fig.3 Input offset

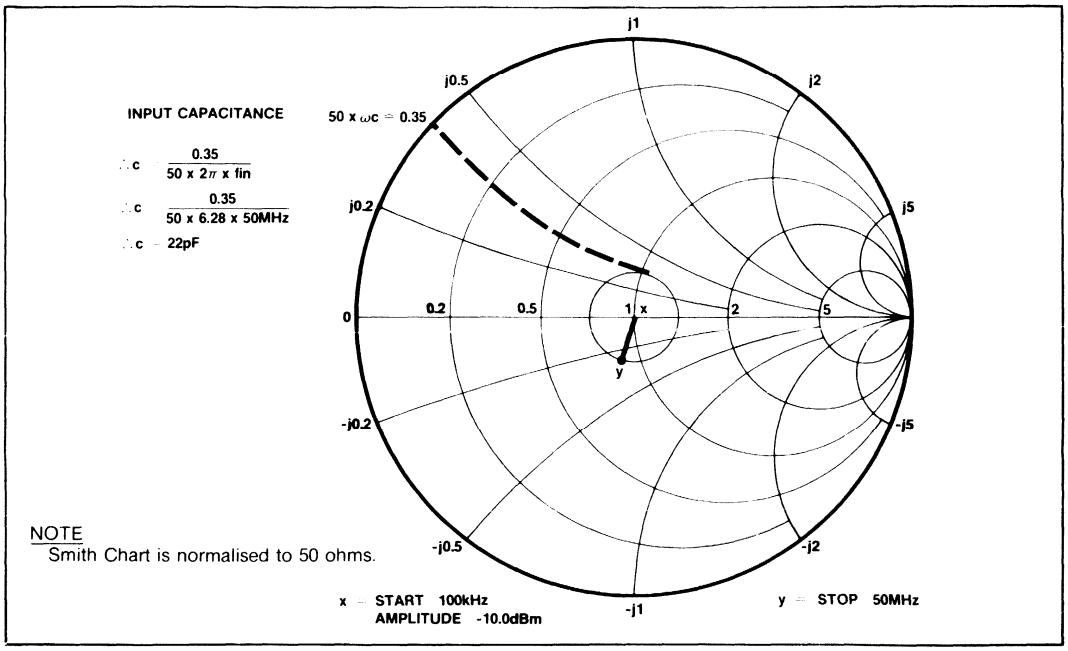


Fig.4 Analog input to board

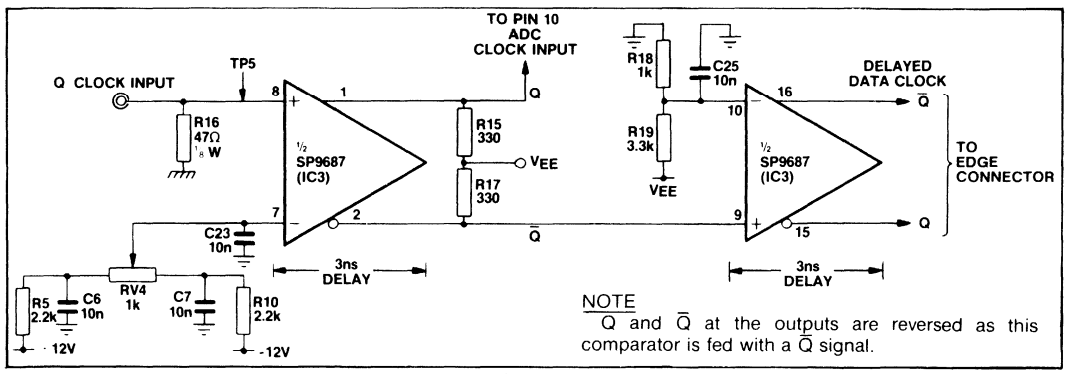


Fig.5 Clock system

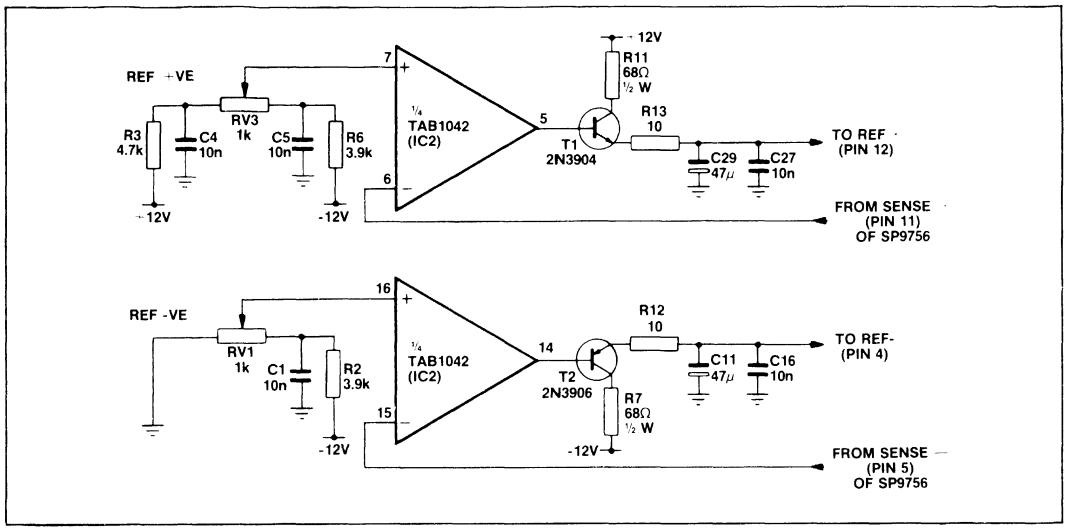


Fig.6 Reference setting

Reference Settings

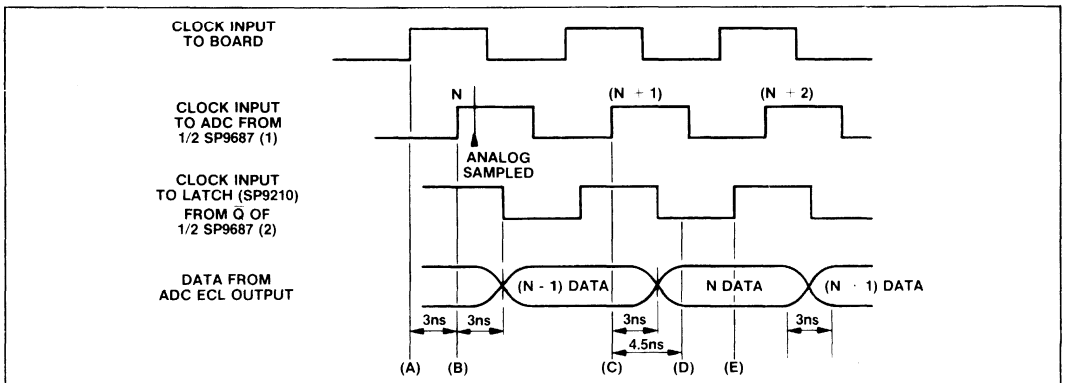
The SP9756 incorporates optional sense outputs (pins 5 and 11) at each end of the reference chain. These allow the reference voltages to be set with precision. The sense outputs permit Kelvin connections to be used to force the precise voltage to the end reference resistors, thus avoiding errors normally caused by bond wire resistances. RV3 is used to set the positive reference voltage via one of the TAB1042 amplifiers. For optimum performance, RV3 should be adjusted until the positive sense voltage (REF +) = 0.0V. This potentiometer will adjust the REF + from +0.6V to -2.2V. RV1 is used to set the negative reference voltage via another amplifier in the TAB1042. For optimum performance RV1 should be adjusted until the sense negative voltage = -2.0V. RV1 will adjust the REF- from 0V to 2.5V. Experiments an be performed on the ADC by adjusting the voltage across the reference chain from 0.5V to 2.0V. Optimum performance will be obtained using a reference voltage of 2.0V.

Digital Outputs

The digital outputs from the SP9756 are brought directly to the edge connector and should be terminated with 100ohm connected to -2V. This termination can be achieved using the Thevenin equivalent circuit, as demonstrated with the DAC application board.

If direct connection to a logic analyser is necessary then the outputs should be terminated on the ADC board using the holes provided.

Other digital signals going to the edge connector are CARRY OUT Q clock and $\overline{Q}$ clock. The clock outputs from the board have been delayed by 3ns using the propagation delay of 1/2 the SP9687 dual comparator.



(A) POINT IN TIME THAT THE BOARD SEES FIRST RISING EDGE
(B) POINT IN TIME THAT THE SP9756 SAMPLES
(C) POINT IN TIME THAT THE NEXT SAMPLE IS TAKEN
(D) POINT IN TIME THAT THE DATA BECOMES VALID
(E) POINT IN TIME THAT THE DATA IS ACQUIRED INTO THE SP9210 LATCH

NOTES
1. The analog input signal is sampled approximately 1.2ns after point (B).
2. As the ribbon cable connecting the two boards will delay the clock and data by the same amount it has been omitted from the diagram.
3. The fact that all intervals are 3ns is mere coincidence.
4. The tolerance on SP9687 propagation delay is ± 1.5ns. The SP9210 setup time is 1.5ns and hold time is 1ns.
5. As 70% of the data is valid no expensive delay line is required.

Fig.7 SP9756 applications board. Clock timing shown at 100MHz

Clock and Data Timing (Fig.7)

The SP9756 accepts standard ECL clock inputs. It then converts them to a differential clock signal used internally. The propagation delay of this internal circuit is approximately 1.2ns, which means that the point that the analog signal is actually sampled is 1.2ns after each rising edge of the clock input to the device.

The clock input to the board is compared to a trip level that can be externally adjusted. This allows an ECL or an AC-coupled signal to be used. The Plessey SP9687 dual high speed comparator is used as it combines low propagation delay (3ns) and complementary ECL outputs. The other half of this dual comparator is connected in series with the first. The reason for this is twofold: first it provides reverse isolation (preventing reflected signals interfering with the clock signal to the SP9756) and secondly it provides the 3ns delay needed to position its rising edge in the centre of the valid data period.

This Q signal from the second half of the SP9687 can therefore be used directly to clock the circuit acquiring the digital information from the ADC board.

For single shot applications it is important to note that the digital word corresponding to any sample will be valid at the output 4.5ns after the second rising edge of the clock input i.e. the data out is valid after the n + 1th sample. This is simply due to the output D-type latch within the SP9756.

This D-type latch provides DATA OUT which is valid for 70% of the clock cycle at 100MHz. This implies that external latch and expensive delay lines can in most applications be omitted.

Evaluation System Construction

Printed circuit board layouts for the ADC and DAC boards are given in Figs. 8 to 13.

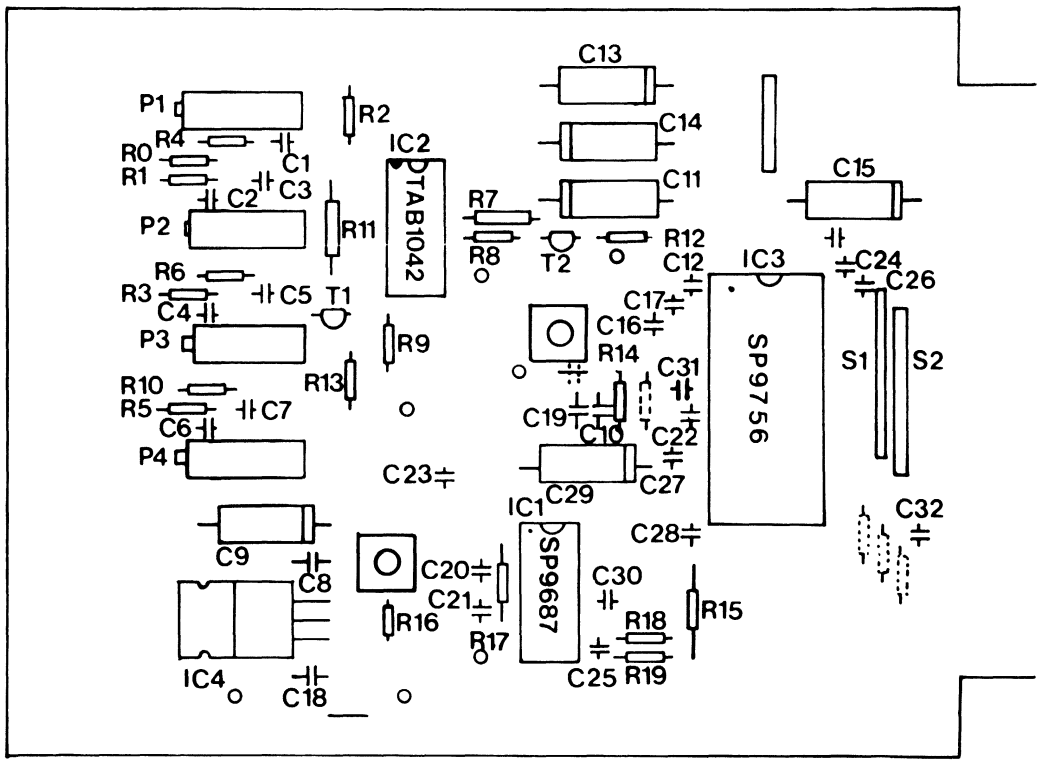


Fig.8 ADC board, component layout - AP9001

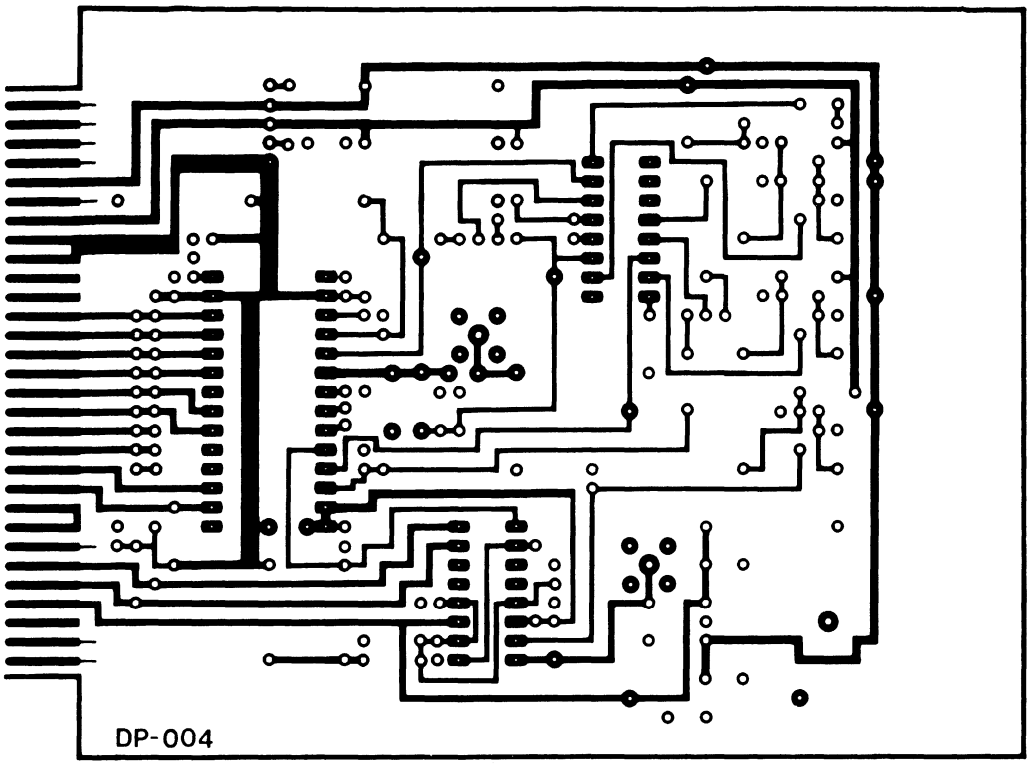


Fig.9 ADC board, underside (black = copper)

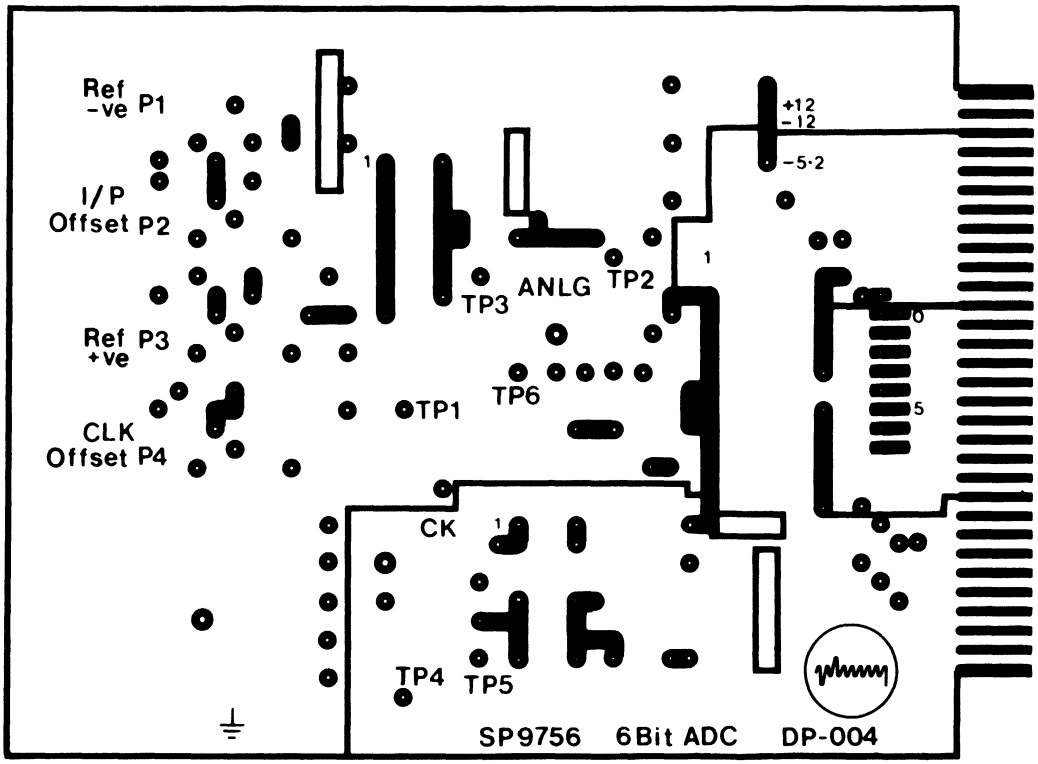


Fig.10 ADC board, component side (white = copper)

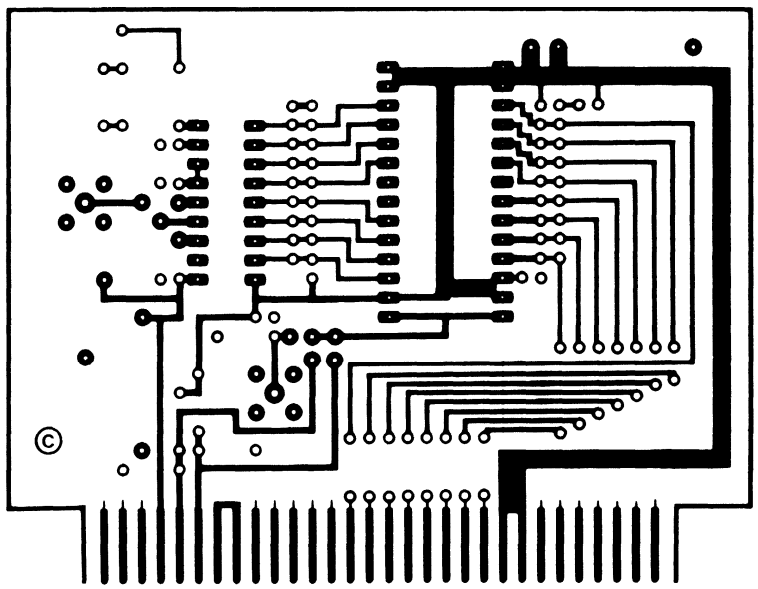


Fig.11 DAC board, underside (black = copper)

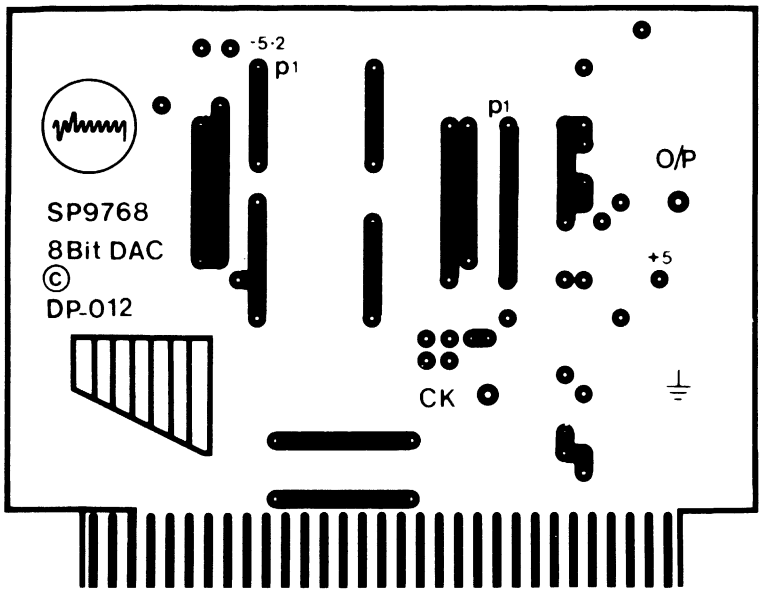


Fig.12 DAC board, component side (white = copper)

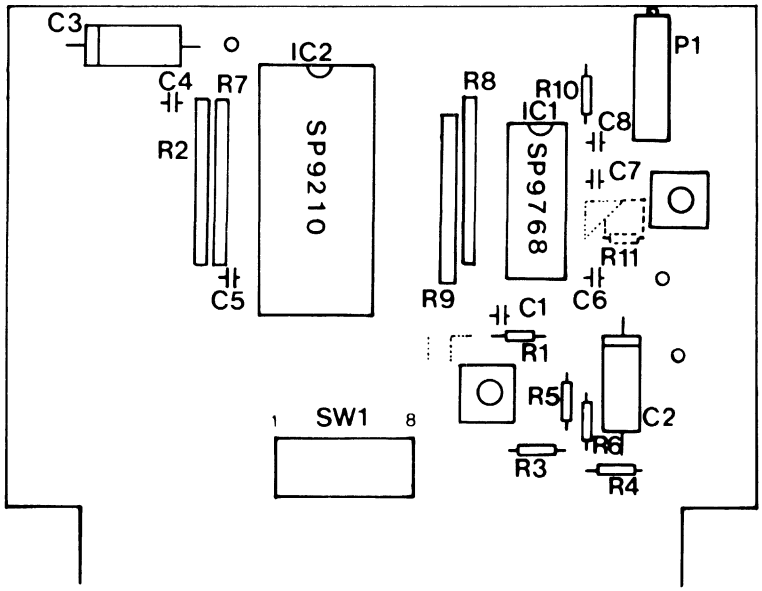
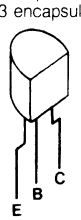


Fig.13 DAC board, component layout

ADC BOARD COMPONENTS

Resistors		Capacitors		Semiconductors	Miscellaneous
R0	47k	C1	10nF	IC1 SP9756-6, 6-bit ADC Plessey	2-off sub-vis connectors
R1	5.6k	C2	10nF	IC2 TAB1042 Quad op.amp Plessey	1-off Molex 5-pin connector
R2	3.9k	C3	10nF	IC3 SP9687 Dual comparator Plessey	270Ω SIL x 8 (Note 7)
R3	4.7k	C4	10nF	IC4 7805 5V regulator	150Ω SIL x 8 (Note 7)
R4	4.7k	C5	10nF	TR1 2N3904 (NPN)	
R5	2.2k	C6	10nF	TR2 2N3906 (PNP)	
R6	3.9k	C7	10nF		
R7	68 1/2W	C8	1μF		
R8	10	C9	47μF		
R9	220k	C10	1μF		
R10	2.2k	C11	47μF		
R11	68 1/2W	C12	10nF		
R12	10	C13	47μF		
R13	10	C14	47μF		
R14	47 1/8W	C15	47μF		
R15	330	C16	10nF		
R16	47 1/8W	C17	1nF		
R17	330	C18	220nF		
R18	1k	C19	47μF tant		
R19	3.3k	C20	10nF		
RV1	1k	C21	10nF		
RV2	1k	C22	12pF		
RV3	1k	C23	10nF		
RV4	1k	C24	10nF		
RV =	(43P102 TYPE SPECTROL)	C25	10nF		
		C26	10nF		
		C27	10nF		
		C28	10nF		
		C29	47μF		
		C30	10nF		
		C31	10nF		
		C32	10nF		

NOTES
1. Resistors are 1/4W when not specified.
2. RV1 to RV4 are 20 turn preset potentiometers (43P102/R8432).
3. 1nF = 1000pF = 103 encapsulated chip.
4. 2N3904
   2N3906



5. Analog and clock inputs are connected using sub-vis type connectors.
6. The input can be AC coupled at link 1. An extra capacitor = 100nF (non-electrolitic) should be used.
7. If the board is to be used directly into another circuit without connecting lead, output termination on the board can be provided using two '8' single in line resistor strips. 270 ohm strip should be connected to -5.2V and 150 ohm should be connected to 0V. (RS part numbers are 140-237 and 140-215 respectively.)
8. Holes have also been provided for Q and $\overline{Q}$ clock pulldown resistors. 330 ohm resistors may be used on the ADC board.
9. The loom connecting this board to the DAC board is twisted pair with a characteristic impedance of 100 ohm. RS Stock No. 360-071.
10. All capacitors have minimum voltage rating of 16V.

DAC BOARD COMPONENTS

Resistors	Capacitors	Semiconductors	Miscellaneous
R1 47 1/8W	C1 10nF	IC1 SP9768 8-bit DAC Plessey	In-line switch,
R2 8 x 150 single in-line (RS Part No. 140-215)	C2 47μF	IC2 SP9210 8-bit Latch Plessey	RS8447/337-560
R3 150	C3 47μF		
R4 150	C4 10nF		2-off sub-vis
R5 270	C5 10nF		connectors
R6 270	C6 10nF		
R7 8 x 270 single in-line (RS Part No. 140-237)	C7 10nF		
R8 8 x 150 single in-line (RS Part No. 140-215)	C8 22nF		
R9 8 x 270 single in-line (RS Part No. 140-237)			
R10 150			
R11 47			
RV1 1k multi turn (43P102) (R8432)			

NOTES
1. Link 1 can be repositioned for Q or $\overline{Q}$ clocks from the edge connector or from the on board sub-vis connector.
2. Link 2 can be repositioned for true or inverse analog outputs.
3. The output amplitude should be adjusted to 0.5V p-p with RV1.
4. R11 is optional. A 1V p-p output can be obtained by replacing R11 with a link.
5. The output will be DC biased below ground by 0.25V with R11, or -0.5V with R11 shorted.
6. The DAC board will accept an 8-bit input for future expansion.

EDGE CONNECTIONS

TOP VIEW

ADC BOARD		DAC BOARD	
Pin No.	Function	Pin No.	Function
1	N/C	1	N/C
2	N/C	2	N/C
3	N/C	3	N/C
4	N/C	4	N/C
5	+12V	5	N/C
6	N/C	6	N/C
7	-12V	7	N/C
8	-5.2V	8	-5.2V
9	-5.2V	9	-5.2V
10	N/C	10	A0 LSB
11	N/C	11	A1
12	A0 LSB	12	A2
13	A1	13	A3
14	A2	14	A4
15	A3	15	A5
16	A4	16	A6
17	A5 MSB	17	A7 MSB
18	N/C	18	N/C
19	N/C	19	N/C
20	N/C	20	N/C
21	$\overline{CO}$	21	N/C
22	N/C	22	N/C
23	N/C	23	N/C
24	N/C	24	N/C
25	Q CLOCK	25	Q CLOCK
26	$\overline{Q}$ CLOCK	26	$\overline{Q}$ CLOCK
27	+5V	27	+5V
28	N/C	28	N/C
29	N/C	29	N/C
30	N/C	30	N/C

Evaluation and Comparison of High Speed ADCs

High speed ADCs are used in many varieties of applications; each application requires special consideration to a particular parameter. For example, designers of video (radar or TV), would pay particular attention to differential linearity, whereas designers using the ADC for measurement systems would need to pay attention to integral linearity. Other systems may need accurate information on analog power bandwidth or bit accuracy.

Specification requirements therefore differ from application to application, and this can make comparison of ADCs difficult. Outlined below is a list of important tests and evaluation methods, starting with the most simple and progressing to the more sophisticated.

ADC evaluation falls into two main groups: the first group utilises a high speed digital to analog converter to reconstruct the digital output into an analog form that can then be displayed on an oscilloscope (Fig.21). The second group of methods looks directly at the digital data. This requires a high speed logic analyser and usually a GPIB-compatible desk-top computer (Fig.22). Computer programs and detailed test methods are available from Hewlett Packard, product note 5180A-2.

TESTS USING RECONSTRUCTION THROUGH A DAC

Test 1. Low Speed Ramp (Fig.14)

This test is very simple. A linear full scale triangular wave (or ramp) is applied to the ADC input, at a frequency that is less than $f_{clock}/(2 \times 2^N)$, where N = number of bits. This ensures that all the timing intervals are displayed. The output from the ADC is then reconstructed in a DAC which should have a greater resolution than the ADC to ensure that all output codes are displayed. The results can then be viewed on a good high resolution oscilloscope.

The resultant staircase has vertical voltages that are due to the DAC and horizontal time intervals that are due to the ADC. Therefore any vertical errors can be ignored as they are due to the DAC alone (using the six most significant bits of the Plessey SP9768 DAC, the vertical steps will appear ideal for a 6-bit ADC). The horizontal time intervals can be viewed in more detail by using the oscilloscope to invert and add the input signal. The remainder will be the quantisation noise. The error will be 1 LSB high $\pm$ 1/2 an LSB. Beware of 'scope input overload and the delay between the two signals when using this method.

A point of major interest is that a differential error or high speed groups of glitches occurs at the mid-step or zero crossing. This is a common problem with many ADCs. At this point the digital section of the ADC is changing from 100000 to 011111; as all the binary outputs are changing at once, large current spikes can result.

Another cause of zero crossing error is two-stage design. Within many flash ADCs the reference chain and/or the comparators are split into two ranks. The device then behaves as two 5-bit devices. This has been avoided in the design of the SP9756.

Reference voltage considerations

The overall accuracy of the staircase will be mostly proportional to the reference voltage. This is because the comparator offsets will remain constant while the bit size will vary with the reference voltage. Therefore it is important to know the reference voltage before making comparisons. Disadvantages of the ramp method are (a) it is difficult to obtain numerical results - although this can be achieved using a Tektronix 7854 scope and (b) this test does not reflect the accuracy at speed.

Test 2. Near Nyquist Beat (Fig.15)

The Nyquist frequency is exactly one half the clock frequency. If a sinewave analog input is set close to this frequency in an unfiltered system, a beat will result. The beat frequency will be

$$f_B = \left|\frac{fc}{2} - f_{in}\right| \text{ (3MHz in Fig.15)}$$

This test is primarily for evaluation of analog bandwidth. The comparators acquire voltages at each end of the input range on successive samples. An ADC that can slew both positively and negatively fast enough to produce an undistorted sinewave beat, contains an extremely fast comparator section. Disadvantages of this method are (a) it is difficult to produce a numerical value of merit, (b) scope triggering is delicate and (c) DAC overshoot can cloud the results.

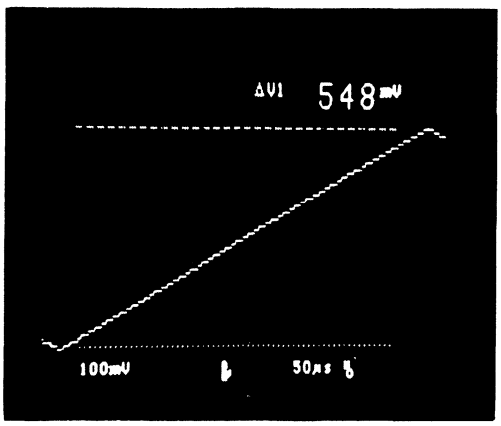


Fig.14 SP9756-6 ADC Linearity. 1kHz ramp input sampled at 100MHz (1V I/P to ADC)

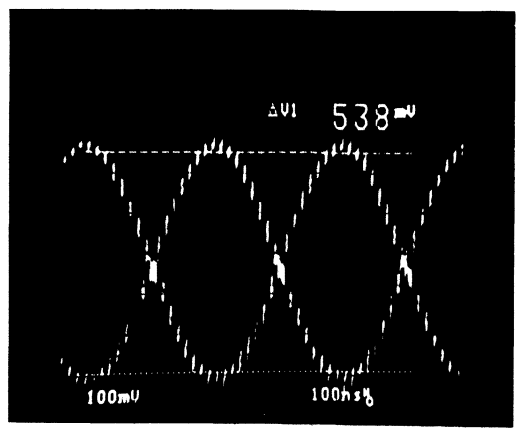


Fig.15 ADC Near Nyquist Beat. 53MHz input sampled at 100MHz 1V I/P to ADC

Test 3. Near Clock Beat (Fig.16)

This is similar to Test 2, except the analog frequency is set close to the clock frequency. Again a beat is produced, $f_B = |fc - f_{in}|$ (3MHz in Fig.16). This is an extremely severe test of input bandwidth. An undistorted sinewave with full amplitude can be produced by the Plessey SP9756 followed by the SP9768 DAC. This test can be extended by increasing the clock and analog frequency i.e. keeping the beat constant, until the output amplitude is reduced by 3dB. This gives an approximate figure for power bandwidth (300MHz using the SP9756).

The disadvantage of this method is that the test can be affected by the DAC. As the DAC is being updated beyond its specified limits, slight glitches and disturbances can result.

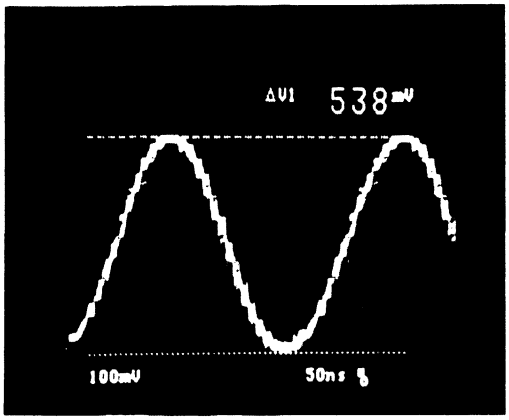


Fig.16 ADC Near Clock Beat. 103MHz input sampled at 100MHz 1V I/P to ADC

TESTS USING DIRECT DIGITAL ANALYSIS

This group of tests are performed by acquiring the digital data directly from the ADC. The data is usually acquired by a high speed logic analyser and then transferred to a desk-top computer for analysis. The ADC is usually driven with a sinewave of full amplitude. The following gives the more popular methods of analysing and plotting the data. It is essential with all the following methods that the input is set to precisely full scale.

Most of the methods below benefit from phase-locked sampling (stationary sampling). In most cases this enables the number of samples taken to be greatly reduced and therefore improving test times.

Method 1. Histogram Test (Fig.17)

This test plots the output code against occupancy of that code. A histogram is produced that theoretically should form a sinewave cusp. Deviations from this cusp will represent differential and integral linearity errors. A differential error would weight the probability of a code being occupied, either more or less than it should be. This distorts the cusp in a positive or negative direction at the code in question. The advantage of this test is that it will indicate the dynamic accuracy of the ADC, i.e. the accuracy to input frequencies up to Nyquist. This is of course not practical using a DAC and oscilloscope. The disadvantages of this method are that (a) it requires a large number of samples and (b) as a cusp is formed, direct reading of linearity from the curve is difficult.

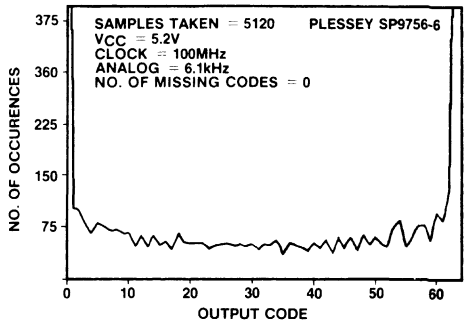


Fig.17 Histogram test

Method 2. Non-lin in LSB (Fig.18)

This test is almost identical to the histogram method. The same data can be used within the desk-top computer. Again a large number of samples are taken and again the occupancy of each code is plotted. The subtle difference is that a $\sin^{-1}$ weighting is applied to the results. This removes the cusp. A graph of differential linearity can be plotted from

$$\frac{\text{(Actual probability)}}{(\sin^{-1}\text{ weighted probability})}$$

As the cusp has been removed, the resulting graph shows at a glance differential non-linearity in terms of LSB. This test can also be performed up to Nyquist limits. A disadvantage is that noise and bandwidth limitations are not evident.

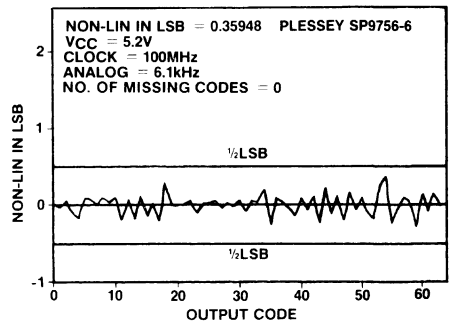


Fig.18 Differential non-linearity in LSB

Method 3. Accumulation Error (Fig.19)

Again, this test can be performed from the initial data. The data is processed to give a graph of integral linearity which can be expressed in two main ways - 'end point' or 'best fit'. The 'best fit' method allows the points to be compared with a line drawn through the average of the results. The 'end point' method is more severe as the line is defined by the end points of the results. From Fig.19 we could quote an integral linearity of 0.25 LSB for 'best fit', but only 0.35 LSB for 'end point'. Therefore it is very important to know which method has been used before comparing integral linearity figures. To form the graph a statistical method is used with many samples taken. The results are corrected for the input sinewave and a graph plotted of levels against deviation from the straight line drawn between end points. This method can also be performed at frequencies up to Nyquist. Fig.20 shows a plot of end point integral linearity at near Nyquist frequencies for the SP9756. As this test represents the total deviation from a theoretically perfect ADC it is a very useful measurement. It also gives a clear representation of distortion caused by the quantising system.

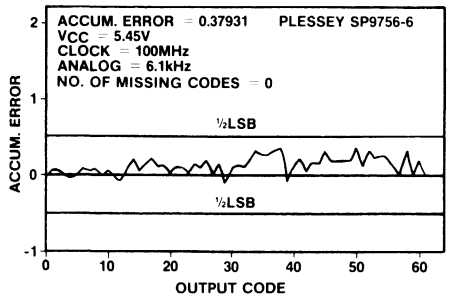


Fig.19 Accumulation error (integral)

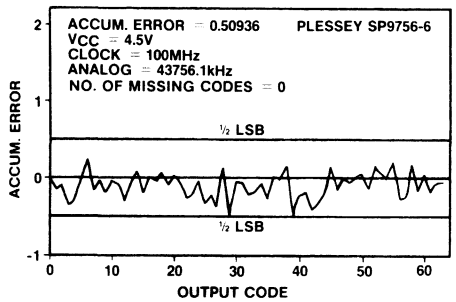


Fig.20 Accumulation error at near Nyquist

Method 4. Sinewave Curve Fit

This test is similar again in that the data is processed by a desk-top computer. The idea is to take a theoretically perfect ADC, generated by the computer and then subtract the actual ADC information contained in the logic analyser from it. The data for the perfect ADC is produced by curve fitting: the Least Squares method is usually used to minimise the error between the actual and theoretical data. A theoretically perfect digitised sinewave which has exactly the same amplitude, frequency and phase as the actual data is required. The remaining difference between these groups of data now represents not only differential and integral linearity but also noise and aperture uncertainty effects. The disadvantages of the method are that (a) the programing must be precise, (b) analog bandwidth problems are not evident and (c) DC offset errors are ignored.

Method 5. Fast Fourier Transform

The fast Fourier transform (FFT) is simply a numerical method for conversion from the time domain to frequency domain. The method is based on the fact that any waveform can be constructed from a number of discrete pure sinewaves of different frequencies and amplitudes. These frequencies can then be plotted to give the spectrum of the signal.

Two methods are used for acquiring the data. The first and most popular, as in the previous methods uses a logic analyser, which transfers the data to a desk-top computer for FFT calculations. The second method (usually using TEK7854 waveform analyser) uses a DAC to reconstruct the data which is digitised and sent to the computer for FFT. The spectral information from this method contains DAC distortions within the results. This can be an advantage if a complete system is to be analysed.

The FFT contains not only linearity information but also other problems that deteriorate the signal-to-noise ratio. Linearity errors cause sidebands to be produced in the frequency domain and so measurement and analysis of the system can be performed in great detail.

The disadvantages of the FFT method are (a) it is important to choose the input frequency to avoid coincidence between the fundamental and harmonics reflected back into the baseband by the sampling technique, (b) the resultant spectrum will also contain the second harmonic of the input. For ADCs over 7 bits it is usually necessary to subtract this harmonic and its aliases from the results and (c) analog bandwidth is not apparent in the results.

CHOICE OF TESTS

To form a good general opinion of a high speed ADC it is necessary to perform the DAC reconstruction tests as they not only show any gross problems with minimal effort, but they give a clear picture of the analog bandwidth and slewing performance. For an evaluation and experimentation system the accumulation methods give a clear picture of performance but for a test system the sinewave curve fit or FFT methods test a wider range of parameters.

OTHER TESTS AND CONSIDERATIONS

Aperture Uncertainty

Aperture uncertainty refers to the amount of jitter at the instant the sample is taken. In other words the time taken between one sample point and the next may not be exactly the same as this time on the following cycle. This uncertainty is usually in the order of 20ps and so measurement is incredibly difficult. The results from techniques using stationary sampling are probably more than 50% inaccurate at high frequency. The effects of aperture uncertainty are usually masked by the phase jitter on the clock signal used to drive the ADC.

Aperture uncertainty is also found within the comparator section of the ADC. The aperture uncertainty will be increased if the comparators take slightly differing times to respond to the sample request.

Metastable States

This exotic term is used when discussing missing samples. There is a finite probability that when a comparator is latched it is at balance. This in fact would be a very rare event, as noise and hysteresis would tend to trip the comparator within the time it is being latched. Nevertheless figures as high as 1 missing sample in 10^{12} have been quoted. The Plessey SP9756 has been designed using techniques to reduce metastable states.

A balanced comparator would in fact cause an error within the decode ROM that in many ADCs causes an all '0's output code for that sample.

Mountain Climb Effect

The 'mountains' here are in fact the spikes produced by the fast edges of the clock. If they are not adequately removed from the reference chain and analog input an interesting effect occurs: as the clock edge speed is increased the reconstructed output will show a DC shift, sometimes above one LSB. This is due to the sample being taken at exactly the same time as the sample edge disturbs the input signal. The result is a 'DC' shift because they will always remain in phase. Good layout using split grounds and good decoupling will minimise this problem.

Data Valid Time

This is an important and frequently ignored parameter. It is simply the proportion of time that the output data is valid, expressed as a percentage of the minimum clock period. If the ADC has a maximum frequency of 100MHz i.e. a minimum period of 10ns, a 70 % data valid time indicates that the data would be valid for 7ns and could be acquired at any time within this period. This is important as the shorter the time, the harder it is to design the system. High cost can result if extra latches and delay lines are needed to collect the data consistently over the specified temperature range.

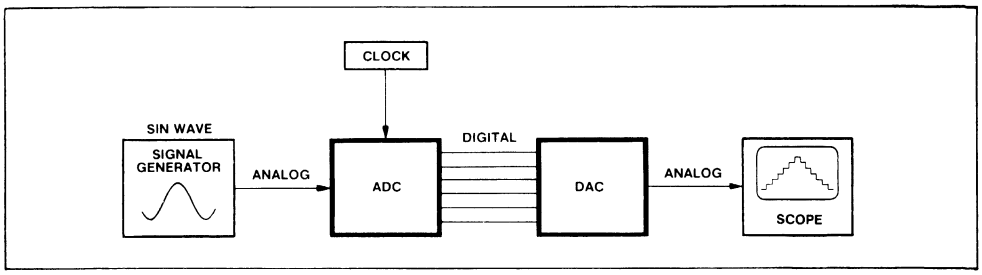


Fig.21

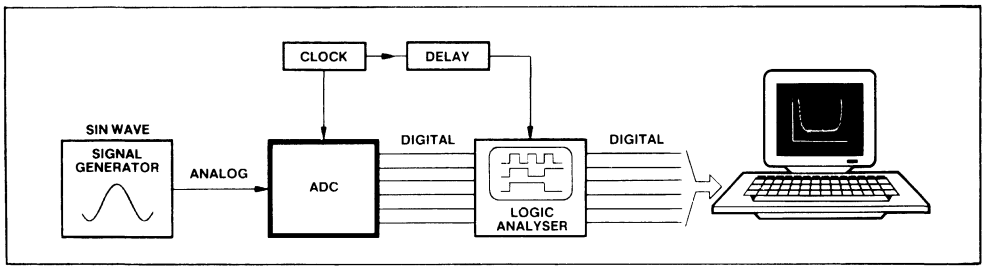


Fig.22

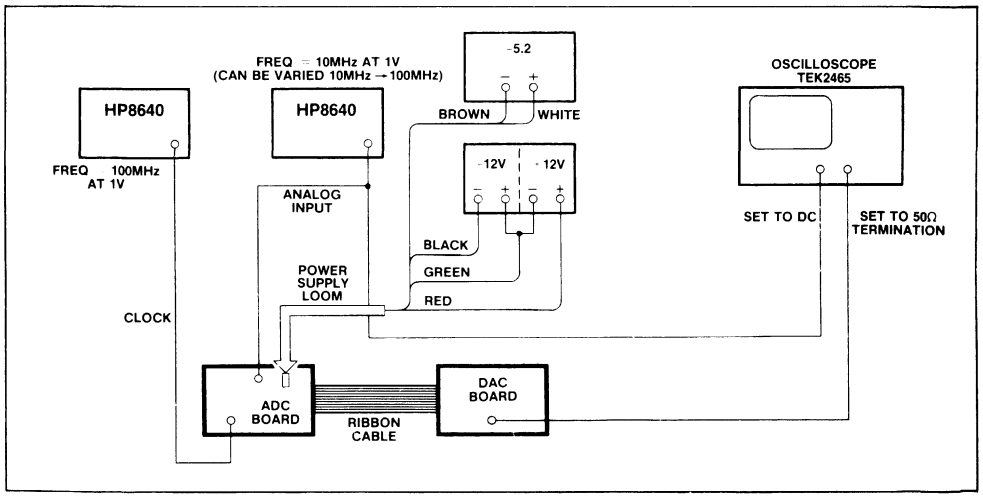


Fig.23 Connection to equipment

RELATED DOCUMENTS

Low Cost Video Speed A-D/D-A (Plessey Semiconductors SP9754 Application Note PS 1993)
Data Products Integrated Circuits Handbook (PS 1989) (Plessey Semiconductors)

ACKNOWLEDGEMENTS

Plessey Design UK
Plessey Applications California USA
Plessey Applications UK

REFERENCES

Dynamic performance testing of A to D converters - Hewlett Packard Product Note 5180A-2.

SP973T8 - An 8-Bit Wideband Flash ADC with TTL Outputs

AN72

This Application Note covers both general ADC system Design and practical circuit ideas to support the Plessey SP973T8 30MHz Flash TTL ADC.

DYNAMIC RANGE

The dynamic range of any flash ADC can be calculated very simply. As each extra bit causes a doubling of the number of comparators used in the device input, this in turn causes a two to one improvement in the dynamic range of the device. A two to one improvement is 6dB, so if we multiply the number of bits by 6, we get the approximate dynamic range of the device in decibels.

This can be further refined by taking into account the shape of the remaining quantisation noise produced by the ADC. Theoretically this gives a constant 1.8dB improvement above the 6 x N figure. However in any practical system we would have a variation in the amplitude of the quantisation noise, caused by the differential linearity error within the ADC. Therefore an ADC with an accuracy of ± ½ LSB will not have the full 1.8 dB advantage. It can be shown that for a ± ½ LSB device an improvement of about 1.2 dB is seen.

Hence, for an ADC with N bits and ± ½ LSB accuracy, the theoretical maximum dynamic range is given by:-

6 x N + 1.2. For an 8- Bit device we have : 49.2dB

The Bit accuracy of many ADCs falls sharply with increasing analog input frequency; all Plessey Semiconductors' standard products are tested dynamically to avoid such problems.

ANALOG INPUT

The SP973T8 is a high speed flash ADC with a wideband input. Therefore the input circuitry is guaranteed not to slew rate limit at high input frequency. This is very important when digitising pulses or when high accuracy is required, up to the Nyquist frequency limit.

The Nyquist limit is simply one half of the clock frequency, and if any signal is applied to the ADC input above this limit it will be reflected, by the clock, back into the passband of the ADC. This effect is called *aliasing*.

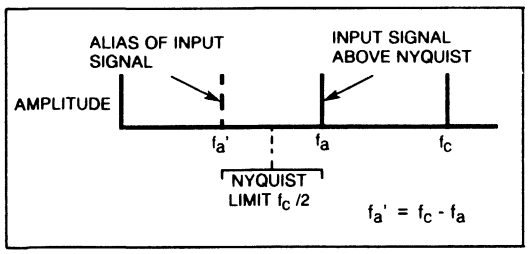


Fig 1

In many systems anti-aliasing filters are required to prevent any high level inputs above fc /2.

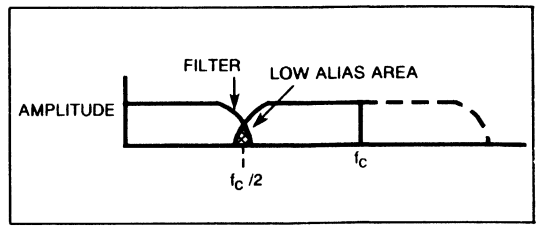


Fig 2

With many video ADCs on the market the analog bandwidth of the input stage will produce slight distortion, and hence produce intermodulation products which can be above the Nyquist frequency limit. With these ADCs restricting the analog input bandwidths is largely ineffective, as it is the ADC itself which causes signals above Nyquist to be generated.

These distortion effects would be difficult to determine from the specification of the device, as they are difficult to test in production. To make matters even worse, sometimes when specifing signal to noise of a device the alias signals are ignored.

Bit Accuracy

One parameter sometimes specified by manufacturers, which will show the true bandwidth and quality of an ADC, is Bit Accuracy. For any ADC to maintain ± 1 LSB at near Nyquist frequency requires an input stage with excellent bandwidth and very low distortion. (see 'near Nyquist beat' test in Application Note AN56 for further information)

To achieve this within the SP973T8 an input bandwidth of over 80MHz was required; this maintains virtually ideal characteristics within a 10MHz input bandwidth.

The high f_T (7GHz) of Plessey's new WS process has made high input bandwidths possible on a device with similar and in most cases lower power consumption than competitive products.

DRIVING THE INPUT CAPACITANCE

Not only is it important to have low distortion within the ADC but also the circuit driving the ADC must show equivalent wideband performance.

High speed flash 8-Bit ADCs have 255 comparators all connected to the input. The SP973T8 is no exception, and hence it has an input capacitance of about 40pF. This capacitance is slightly voltage-dependent and therefore it is important to provide a good quality low impedance drive for the SP973T8.

Plessey provide two op-amps with the required performance: the SL541 and the SL9999.

SL541

The SL541 is a bipolar device with high slew rate and excellent pulse handling, plus very good overload performance. The device has been used by many manufacturers as the op-amp driver in ADC systems.

One reason for this is the provision for adjustable open loop gain. The open loop gain can be reduced by a single resistor for stable operation at closed loop gain as low as unity.

The SP973T8 input requires a high current drive at high frequency. Therefore it is advised that one of the Plessey range of high performance transistors is used within the op-amp feedback loop (2N3904 or equivalent).

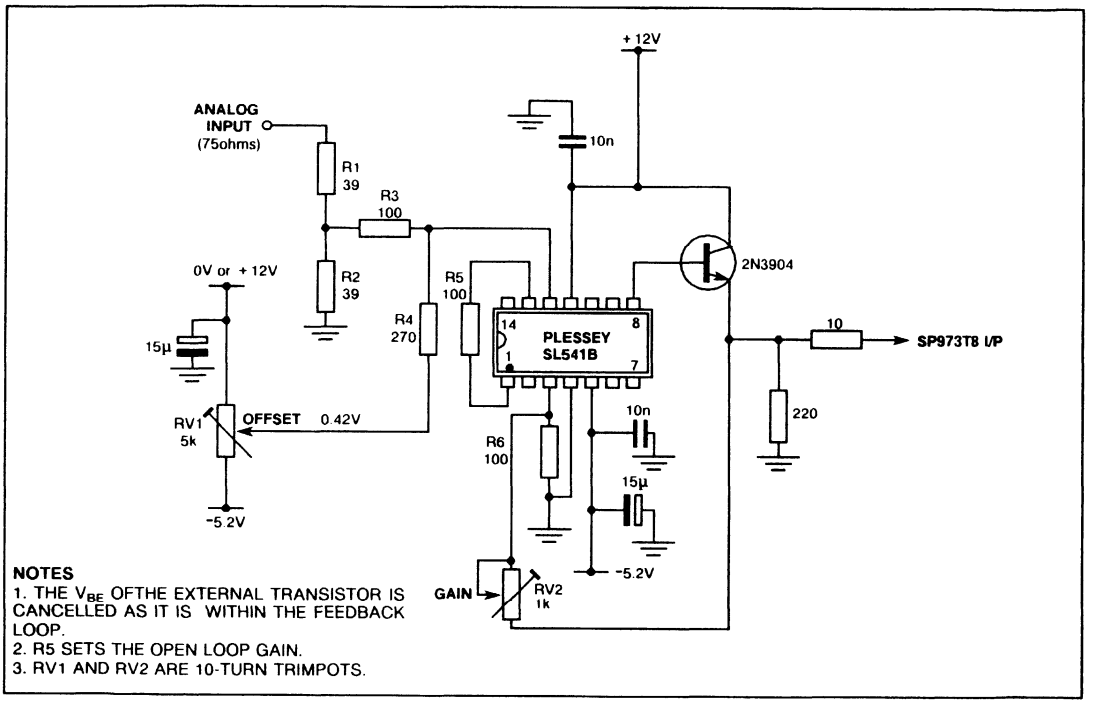
SL9999

This device is similar to the SL541, but has three main differences.

First, the bandwidth of the SL9999 is up to 400MHz under unity gain conditions and at least 200MHz when driving a 30pF capacitive load.

The second difference is that the SL9999 contains a power output stage which is capable of driving at least ± 50mA, this is adjustable down to ± 10mA using an external resistor (R_X in Fig 4).

The third difference is that external compensation cannot be provided. To avoid problems it is recommended that a closed loop gain of about 4 is used, when driving ADC inputs.



NOTES

1. THE V_{BE} OFTHE EXTERNAL TRANSISTOR IS CANCELLED AS IT IS WITHIN THE FEEDBACK LOOP.
2. R5 SETS THE OPEN LOOP GAIN.
3. RV1 AND RV2 ARE 10-TURN TRIMPOTS.

Fig. 3

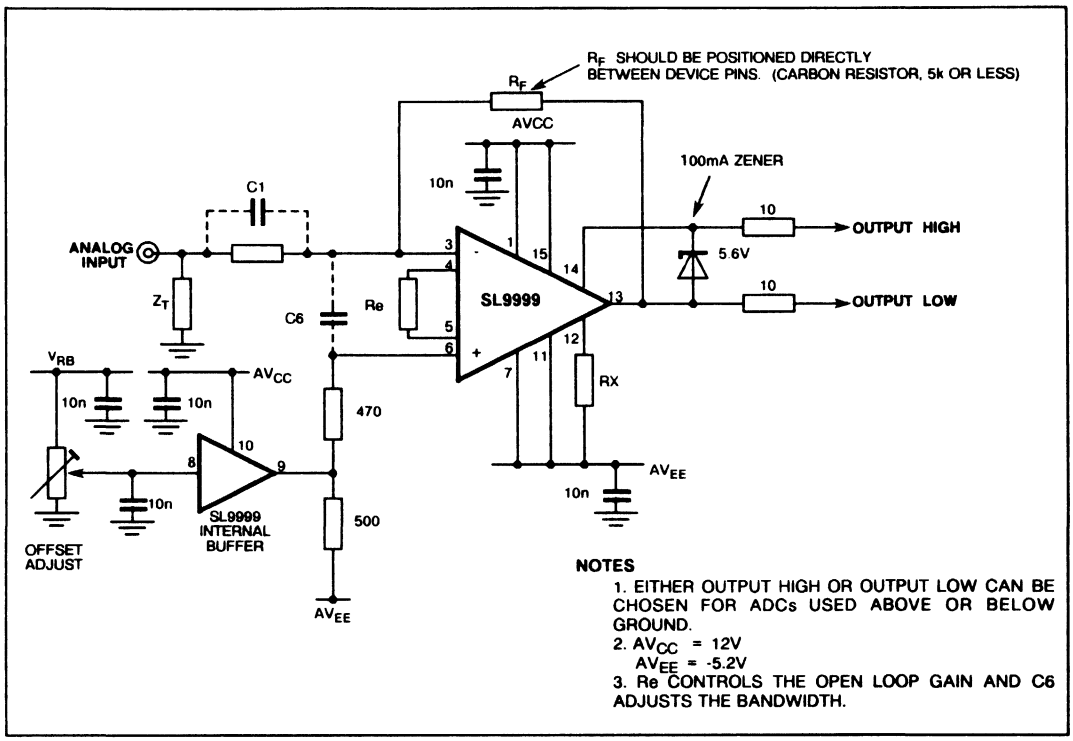


Fig 4

OTHER ADC DRIVERS

Another device of interest for ADC input driving is the SL6140 400MHz Wideband Amplifier. Although this device may not have the current drive required for precision at high speed, its AGC capabilities can be very useful in wide dynamic range applications. The SL6140 has current sourced outputs which require pull-up resistors. See also the ZN428 DAC for AGC input control from a microprocessor.

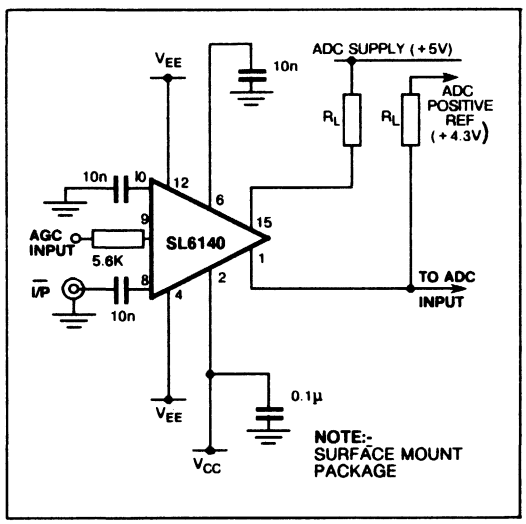


Fig 5

CLOCK INPUT

The SP973T8 is specified as a 30MHz ADC. However, the typical production device will perform adequately at clock frequencies of over 50MHz with an input of up to 10MHz.

Unlike many ADCs the SP973T8 has an internal clock amplifier and buffer. This amplifier has been introduced to avoid one of the most difficult problems when using an ADC in a system design : clock pickup. A fixed frequency at up to 30MHz with TTL type levels, would cause crosstalk resulting in reduced performance (patterning on video signals, etc.)

The clock input has been designed so that both differential or single ended drive can be used at low voltage levels. Pins 5 and 6 can be used differentially and will accept standard ECL. (See SP92701 device). For single ended operation pin 6 can be decoupled to ground, and pin 5 driven with a 1V peak to peak signal. Pin 6 will then bias to +3.8V and can then be used to bias pin 5, through a resistor for AC coupled clock applications. See Fig 6.

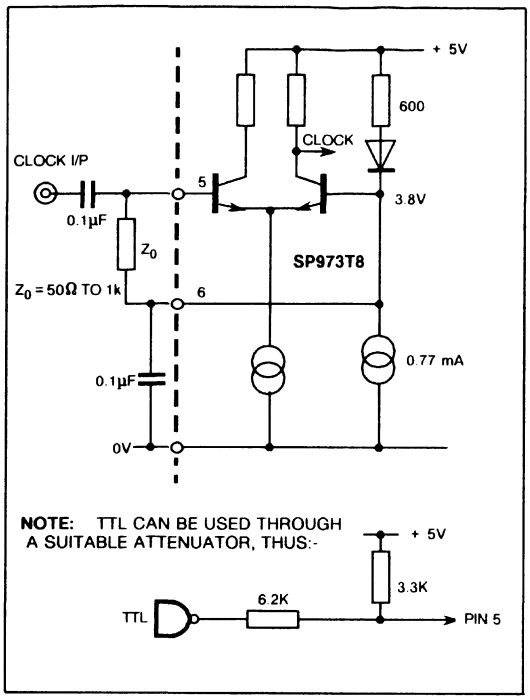


Fig. 6

REFERENCE VOLTAGES

The internal reference chain requires two DC voltages applied to the top and bottom of the internal resistor ladder, as shown in Fig. 7.

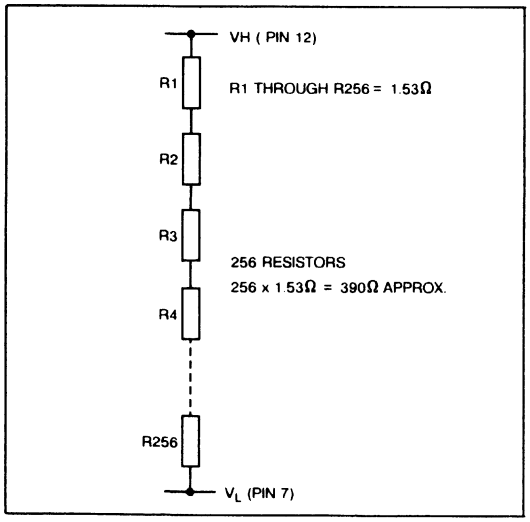


Fig. 7

The best differential linearity from any flash ADC is achieved when the maximum reference voltage is applied to the reference chain. This is because the offset voltages of each internal comparator will remain constant.

So increasing the reference voltage will improve the ratio of Bit size to offset voltage and hence improve the overall accuracy. For the SP973T8:-

VH Max = + 4.5V

VL Min = + 1.9V

Therefore the recommended values for VH and VL are

VH = + 4.3V

VL = + 2.3V

The tolerance on the reference chain's absolute resistance is about ± 25% from batch to batch, therefore the current taken by the reference chain for worst case conditions is approximately

$$\frac{2V}{390\text{-}0.25\times390} = 6.8mA$$

Using a reasonable safety factor 8mA worst case current should be catered for.

SETTING THE REFERENCE VOLTAGES

Method 1

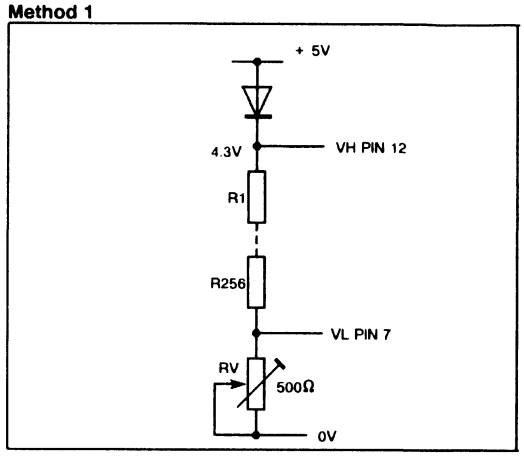


Fig. 8

This is the simplest and least precise method. RV is adjusted to maximum resistance then when power is applied RV is decreased until VL = 2.3V.The diode will set VH to approximately 4.3V. There are three main disadvantages with this method. First, setup of RV is needed for each device, second, the 2mV/°C of the diode will change the VH voltage with temperature (over 100mV drift) and third, no supply line regulation is provided.

Method 2

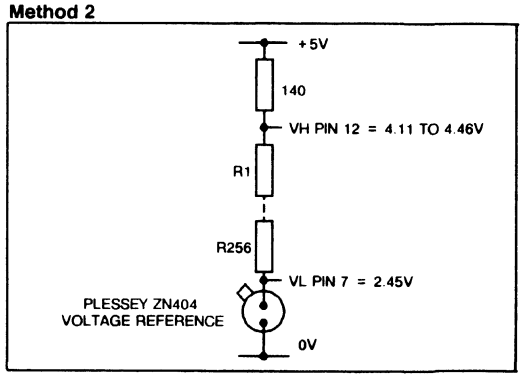


Fig. 9

This method is more temperature stable than method 1 and requires no setup as long as a device batch to batch tolerance on VH of 4.11V to 4.46V can be tolerated.

Once again, no supply line regulation is provided using this method. As the differential linearity of the SP973T8 is well within the ± 0.5 LSB limit, the reduced reference voltage has little or no effect (VH -VL = 1.85V)

Method 3 (precision reference voltages)

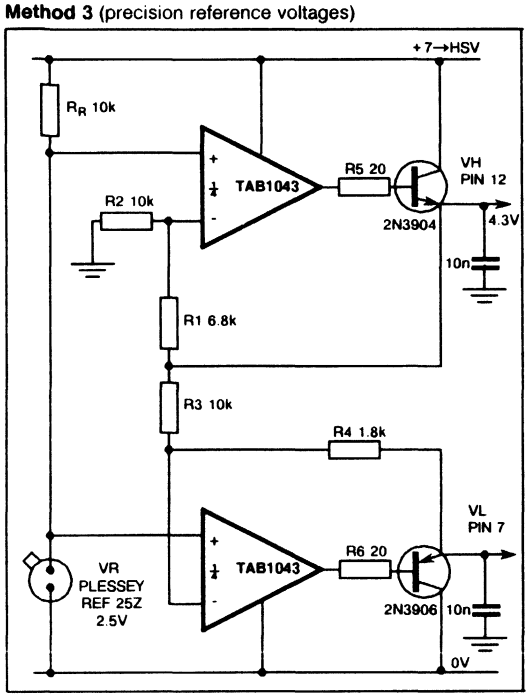


Fig. 10

$$VH = \frac{(R1 + R2)}{R2} VR \quad \text{---------- (1)}$$

$$VL = \frac{VR\,(R3 + R4) - VH\,R4}{R3} \quad \text{------- (2)}$$

With R2 and R3 set to 10k. R1 can be calculated by re-arranging equation (1):

$$R1 = \frac{R2\,VH - R2}{VR}$$

R4 can be calculated by re-arranging equation (2):

$$R4 = \frac{R3\,(VR - VL)}{VH - VR}$$

This method gives excellent supply line regulation and precise voltage settings of VH and VL.

The temperature stability will also be excellent and will depend primarily on the input offset with temperature variation of the op-amps used. The Plessey SL562 is a suitable single op-amp or the TBA1043 is a quad version which can also be used.

The only disadvantage with this method is that a separate supply at least 2V above the ADC supply is required. This is a consequence of the output high voltage from the op-amp (we would require a +5V output with the op-amp on a +5V supply!)

SP973T8 OUTPUT DATA (see SP973T8 datasheet Fig. 5 for typical test load)

The output levels are TTL compatible, and switch from 0V to +4V. The output drive is capable of providing a useful output with 10pF loads at clock frequencies of over 120MHz.

The outputs are double latched which gives a very good data valid time. This means that the data can be captured any time within the clock cycle except the first 10ns (t_{pd}). The data is clocked onto the output pins by the falling edge of the clock signal. The typical system would therefore use the rising edge of the clock to capture the data into RAM or directly into a digital to analog converter (the Plessey MV95308 is a suitable complementary DAC).

SINGLE- SHOT OPERATION

To produce a single sample of an analog input the device must be clocked twice. This is due to a one cycle delay inherent within the device.

MID- REFERENCE

This is simply the centre of the reference chain bonded out to pin 10 of the device. One of its uses is to provide a decoupling point which aids in the removal of digital noise from the reference chain.

Another use is to trim the device integral linearity in precision measurement systems, as shown in Fig. 11.

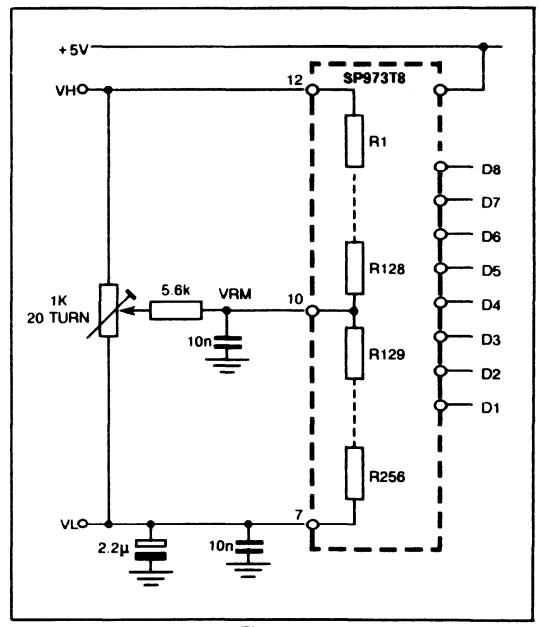


Fig. 11

Another and more common use of VRM is to provide a bias input for AC coupled analog inputs, as shown in Fig. 12 . Pin 10 is used to bias the analog input.

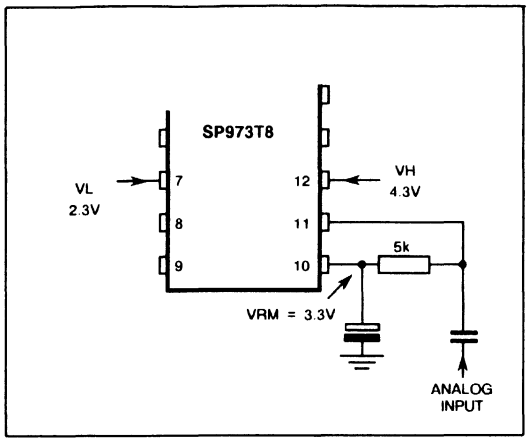


Fig. 12

LAYOUT AND GROUND SYSTEM

The main objective when laying out the PCB, is to avoid clock or data edges crosstalking into the analog input or onto the ADC references. This can be achieved most effectively by the use of a split ground plane. One analog and one digital ground plane connected together at one point close to the device, is the most suitable approach.

Supply line decoupling is very important when dealing with a mix of analog and digital signals. Low inductance capacitors should be used located close to the device pins.

STANDARD TV VIDEO ENCODING

The SP94308 is a Plessey 8-Bit 20 MHz TTL ADC which has been specially designed for digitisation of composite video PAL or NTSC signals. Its speed and performance allow digitisation at the standard digital video clock speed equal to three times colour subcarrier with analog bandwidths of over 6MHz (NOT for wideband applications).

The SP94308 contains clock buffering, input buffer and x2 input amplifier, plus a black level clamp and many other useful features that benefit system design (refer to Application Notes AN52 and AN 57).

The SP973T8 is recommended for composite video systems where the bandwidth of the signal exceeds 6MHZ (satellite systems, MAC systems,etc.).

HIGH FREQUENCY DIGITISATION

The SP973T8 is only one device in a complete range of ADCs from Plessey, its equivalent part with ECL outputs is designated SP973E8. This device is identical to the SP973T8 except for pinout and output stage.

100MHz AND ABOVE

The Plessey SP97508 8-Bit 110MHz ADC has ECL outputs and is also designed for wideband applications (refer to Application Note AN65).

CHARGE COUPLED DEVICES (CCDs)

Many systems require ADCs and then RAM to store and processed analog information. If random access to the stored information is not required, i.e., time delay or time expansion or contraction, then it can be more cost effective to use a CCD. The Plessey range includes devices such as the MS1013, 20MHz low cost 910 element device, which is ideal for video applications. Devices which can be used in systems at 100MHz and above are included in the CCD range (ask you local Plessey Office for Application Note AN55 - not published in this Handbook).

SUMMARY

Finally, we hope that a clearer distinction has been made between a standard video ADC and the wideband SP973T8. Not only can a wideband device be used in quality video systems, but also in pulse measurement equipment, digital oscilloscopes, radar I and Q channel, video digitisation, nucleonics collision ionisation pulse measurements - indeed, any other system in which the performance of the equipment is defined by the quality of the ADC.

ZN425 8-Bit A-D/D-A Converter Applications

1. INTRODUCTION

Digital to analogue, (D-A), and analogue to digital (A-D), conversion is a specialised field of electronics. It is useful to consider first the general principles of such conversion techniques, and definitions commonly used in the general field of A-D and D-A conversion.

The discussion is limited to 8-bit converters of a type similar to the ZN425E, illustrated in Fig.1a.

Digital information, fed in to the converter, normally as parallel bits, generates an anlogue output corresponding to the value of the binary coded number entered at the input. Ignoring errors for the moment, and assuming that the analogue output is a voltage, the output can be expressed as:

$$V_{out} = V_{full\ scale} \times \frac{\text{Binary input}}{\text{Full-scale binary input}}$$

which, in the case of the ZN425E, is

$$V_{out} = V_{REF} \times \frac{\text{Binary input}}{256}$$

The voltage output is obtained using a resistive ladder network shown in Fig. 1b. Switches connect resistors within the network either to the reference voltage or to the ground line according to the state of the binary inputs controlling each particular switch.

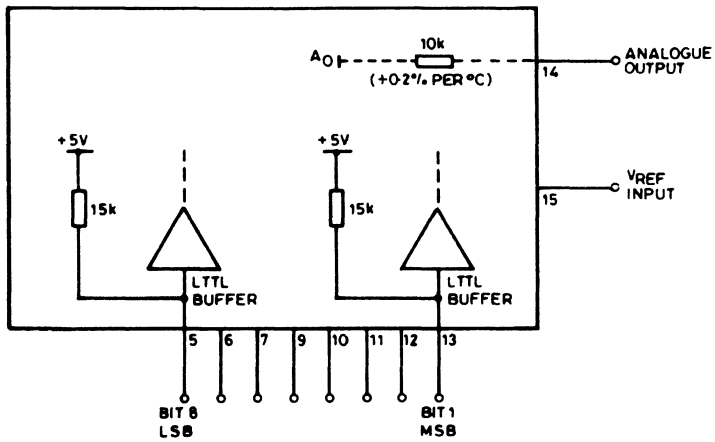


Fig. 1a Basic 8-bit D-A converter

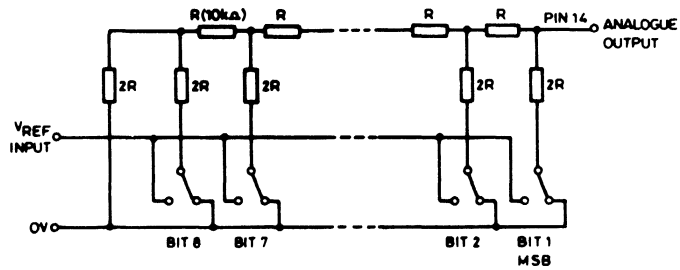


Fig. 1b The R-2R ladder network

The block diagram of the ZN425E circuit is reproduced in Fig. 2.

The integrated circuit is fully monolithic. It contains a resistive ladder network, a logic input select switch, voltage switches, an internal reference and a counter. The D-A reference may be connected to the internally generated reference or to an external reference voltage. The inclusion of a counter within the circuit considerably extends its application. A 'staircase' waveform can be very simply generated at the analogue output by feeding a train of clock pulses into the counter.

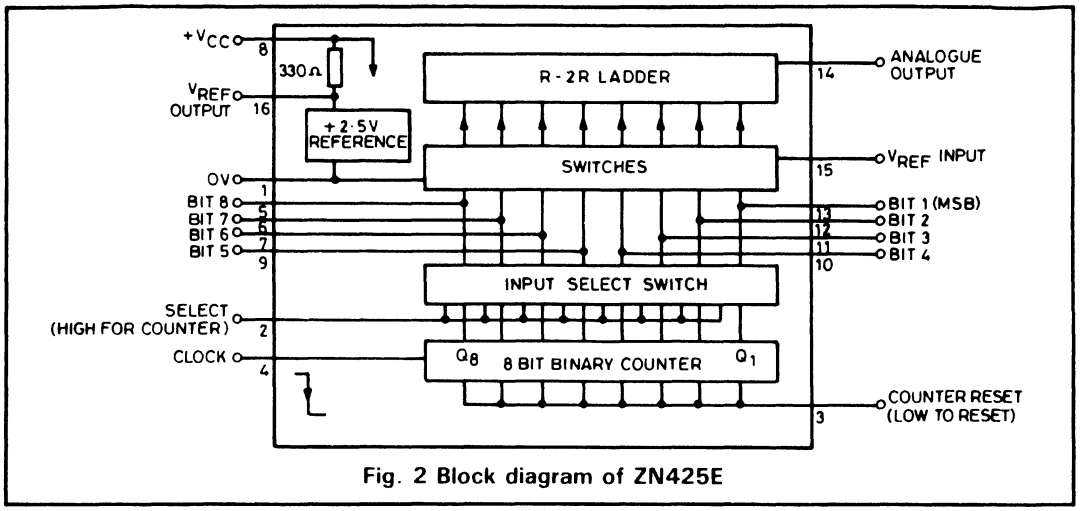


Fig. 2 Block diagram of ZN425E

The ZN425E system operation is outlined in Fig. 3. The counter may be clocked by negative going inputs and reset by applying a '0' level to the reset pin.

The digital inputs to the converter may be obtained either from an external source when the 'logic select' pin is at logical '0', or from the counter when it is set to logical '1'. In the latter case the state of the counter appears at the digital input terminals as '0' or '1' levels on open collectors with 15kΩ pull up resistors. In the D-A mode the digital input terminals may be considered as low power TTL inputs.

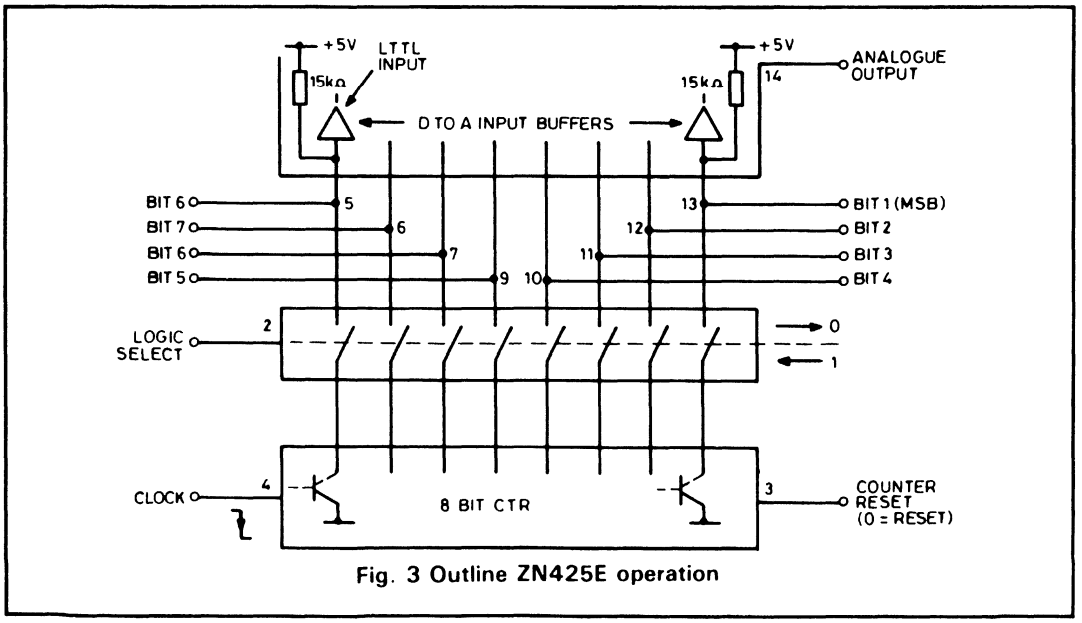


Fig. 3 Outline ZN425E operation

1.1 Definitions

Various terms commonly used when discussing D-A and A-D converter operation are defined below.

Resolution

The resolution is determined by the number of digital inputs, i.e. an 8-bit ADC, (digital to analogue converter), is said to have 8-bit resolution. No particular level of accuracy is implied

Staircase/Ramp

As the binary code is increased step by step, the analogue output also increases in discrete steps. If the input code increases at a constant rate the resulting output will be a staircase.

Since the number of discrete steps is normally large, e.g. 255 for 8 bits, the staircase is frequently termed a ramp, though this is not strictly accurate.

Monotonicity

A DAC is said to be monotonic if an increase in the applied binary coded digital number always produces an increase in the analogue output. Waveforms produced by a D-A 'staircase' generator illustrated in Fig. 4a shows the effect of non monotonicity.

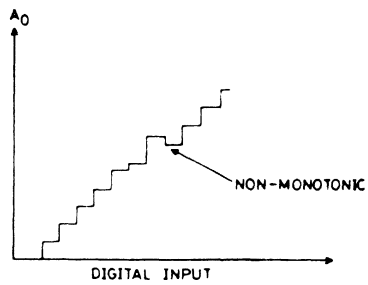


Fig. 4a Non-monotonicity

Ideal DAC Output

The ideal DAC output of a staircase generator is shown in Fig. 4b.

The output is defined as a set of points on a straight line between zero and full-scale. For an ideal 8-bit DAC:

$$V_{out} = \frac{n}{2^8 - 1} \times V_{FS}$$

$$= \frac{n}{255} \times V_{FS}$$

and $$V_{FS} = \frac{255}{256} \times V_{REFinput}$$

$$\therefore \quad V_{out} = \frac{n}{256} \times V_{REFinput}$$

where 'n' is the number represented by the digital input.

For example

$$01101100 = 2^6 + 2^5 + 2^3 + 2^2$$

$$= 108$$

gives an output $$V_{out} = \frac{108}{256} \times V_{FS}$$

$$= \frac{108}{256} \times V_{REFinput}$$

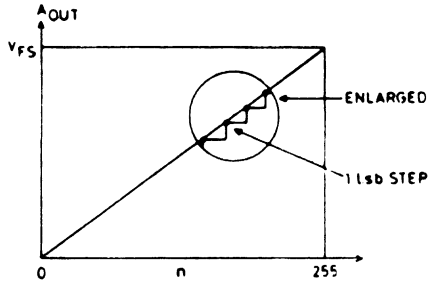


Fig. 4b Ideal DAC output

Linearity error

A DAC may deviate from the ideal as shown in Fig. 4c. The error is usually specified as a maximum deviation of the analogue output from the ideal output, as a fraction of the least significant bit'. The ZN425E has a linearity better than ± ½LSB, and

$$\tfrac{1}{2}\text{LSB} = \tfrac{1}{2} \times \frac{V_{FS}}{255}$$

Relative accuracy

The error expressed as a percentage of the full-scale voltage, V_{FS}, is termed the relative accuracy.

The ZN425E, an 8-bit converter with ± ½LSB linearity, has a relative accuracy of $\frac{1}{510} \times 100\%$, i.e. approximately 0.2% accuracy.

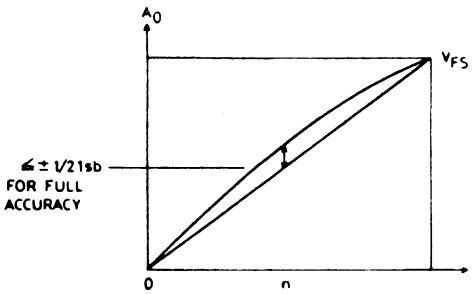


Fig. 4c Error definition

2. D-A/A-D CONVERTER SYSTEM

2.1 8-bit D-A and calibration procedure

The ZN425E gives an analogue voltage output directly from pin 14, so that the usual current to voltage converting amplifier is not required. However, in order to buffer the resistive ladder output impedance, to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary. Figs. 5a and 5b show a typical scheme with either the ZN424P or 741 as the buffer amplifier. The internal voltage reference source ($V_{REF\ out}$) is used, and to minimise temperature drift the source resistance to the inverting input of the buffer amplifier should be approximately 6kΩ. Calibration procedure is as follows:

procedure is as follows:

(i) Set all bits to LOW and adjust R2 until $V_{out} = 0.000V$

(ii) Set all bits to HIGH and adjust R1 until V_{out} = nominal full-scale reading - LSB

(iii) Repeat (i) and (ii)

e.g. Set F.S.R. to +3.840V -1LSB = 3.825V.

$$(1LSB = \frac{3.84}{256} = 15mV)$$

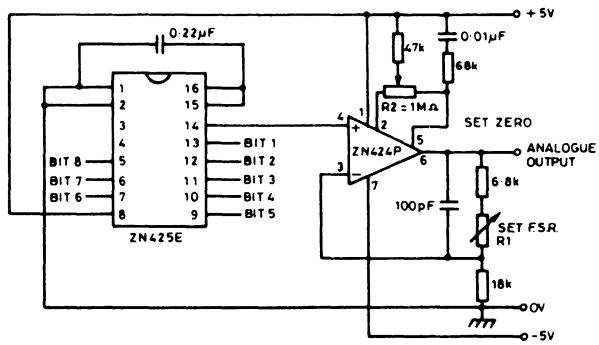


Fig. 5a 8-bit DAC using ZN424P

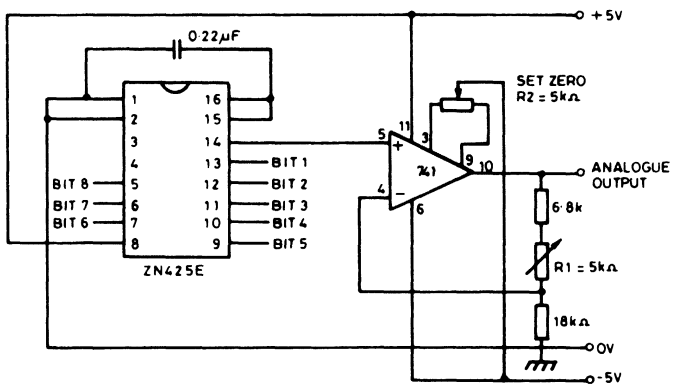


Fig. 5b 8-bit DAC using ZLD741CP

2.2 8 Bit A-D and calibration procedure

Fig. 6 shows the ZN425E in a counter type ADC which comprises a comparator and a latch and requires an external clock. Upon application of a convert command pulse (15μs minimum) the counter is set to zero and at the same time the state of the latch is altered.

The gate is opened, enabling clock pulses to be fed to the counter input (Pin 4) of the ZN425E. The analogue output of the ZN425E begins to ramp up until its amplitude equals that of the analogue voltage at the non-inverting input of the comparator. At this point the comparator changes state, altering the latch to its initial resting state, thus inhibiting further clock pulses. Hence the digital number stored in the respective bits of the ZN425E is a true representation of the analogue input voltage. The diode is included so that when the comparator changes state, its output is effectively clamped at zero (LOW).

Operating clock frequencies can be as high as 400kHz. Improved results may be obtained by using narrow clock pulses to avoid the trailing edge affecting ramp settling. At frequencies above 100kHz a faster comparator than the ZN424 should be used for optimum linearity around zero.

The conversion time is dependent upon the analgoue input and for full-scale reading (F.S.R.) is given by the clock period multiplied by the number of counts.

If $F_{clock} = 256kHz$,

$$T_{Convert} = \frac{2^8}{256 \times 10^3} \text{ seconds} = 1ms$$

The calibration procedure is as follows:

(i) Apply continuous CONVERT COMMAND PULSES

(ii) Apply full-scale minus 1 ½LSB to analogue input and adjust F.S.R. pot until the converter LSB just switches between 0 and 1 with all other bits at 1.

(iii) Apply zero + ½LSB to analogue input and adjust zero pot until the converter LSB just switches between 0 and 1 with all other bits 0.

(iv) Repeat step (ii).

E.g. Full-scale = 4 volts.

$$1LSB = \frac{\text{Full-scale}}{256} = \frac{4V}{256} = 15.63mV$$

Input for zero setting = ½LSB = 7.82mV

Input for full-scale setting = 4V - 1½LSB = 3.97656 volts.

After conversion is complete the analogue input is available from the ZN425E in digital and analogue form and therefore the ADC may be used as a sample and hold with infinite hold time. The convert command is replaced by a sample command.

A peak detect circuit may also be constructed using similar techniques, and is described in section 3-4.

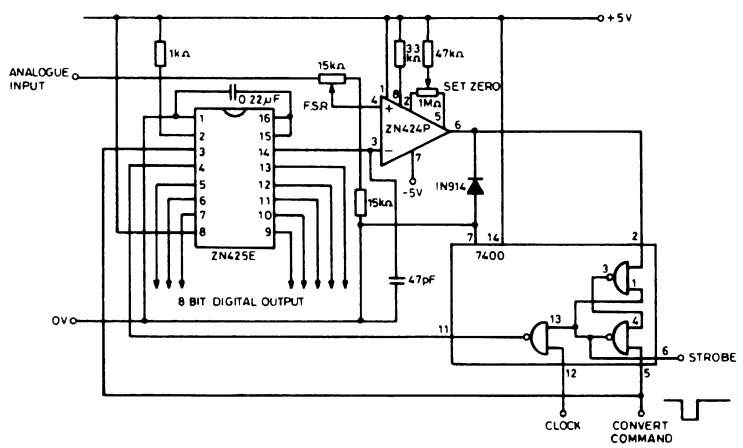


Fig. 6 8-bit A-D converter

2.3 Bipolar operation

Previous circuits described have entailed the use of a uni-polar buffer amplifier (using ZN424P and 741) following a DAC as a means of removing the offset voltage, minimising temperature drift and calibrating the DAC. A natural sequal to this is the derivation of a bipolar buffer amplifier which fulfils these conditions. This entails buffering the output of a DAC such that the amplifier output from the buffer is symmetrical about zero. To effect this, the conditions that have to be satisfied are:

(i) When the DAC output $= \frac{V_{REF}}{2}$ (digital input = 10000000) then the buffer amplifier output = zero.

(ii) Gain can be easily selected and suitable resistor values calculated. Actual gain and offset must be capable of fine adjustment.

The circuit of Fig. 7a was first devised as a possible solution.

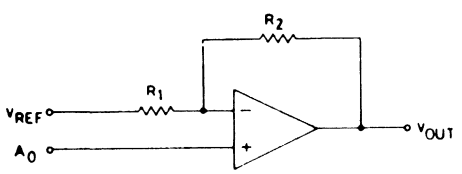


Fig. 7a Bipolar operation, starting point

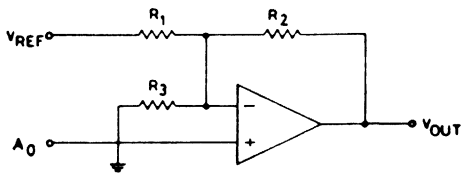


Fig. 7b Bipolar operation, concept progression

If F_N = non-inverting feedback return $= \frac{R1}{R1 + R2}$ and F_I = inverting feedback return $= \frac{R1}{R2}$

Then V_{out} is given by:

$$V_{out} = \frac{A_O}{F_N} - \frac{V_{REF}}{F_I} = A_O\left(\frac{R1 + R2}{R1}\right) - V_{REF}\frac{R2}{R1} \quad \text{. . . equation 1}$$

If $A_O = \frac{V_{REF}}{2}$ and R1 = R2 the V_{out} = 0 satisfying condition (i).

However Gain $\left(\text{defined as } \frac{V_{out}}{A_O}\right) = \frac{R1 + R2}{R1} = 2$ and condition (ii) would not be satisfied since adjusting R1 or R2 would upset the gain on offset. To minimise these disadvantages therefore the circuit of Fig. 7b was devised using an additional resistance, with its Thevenin equivalent of Fig. 7c. Using equation 1 then an expression for the output voltage V_{out} can be shown as:

$$V_{out} = A_O\left[1 + \frac{R2(R1 + R3)}{R1\,R3}\right] - V_{REF}\frac{R2}{R1}$$

For $A_O = \frac{V_{REF}}{2}$ (Condition (i)) then $V_{out} = 0$

and $R1 = \frac{R2\,R3}{(R2 + R3)}$ i.e. R1 = parallel combination of R2 and R3.

Substituting this expression for R1

then Gain $G = \left[1 + \left(\frac{2R2 + R3}{R3}\right)\right] = \left[2 + \frac{2R2}{R3}\right]$

If we let say $R2 = \lambda R3$ the $G = 2(1 + \lambda)$ and $\lambda = \left(\frac{G - 2}{2}\right)$

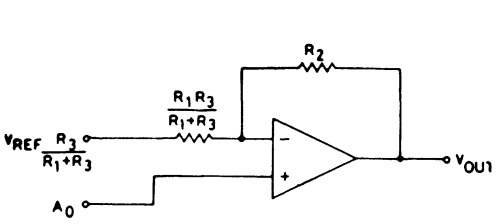


Fig. 7c Thevenin equivalent of Fig. 7b

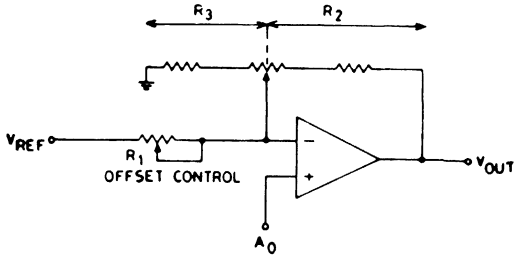


Fig. 7d Bipolar operation, control schematic

i.e. $G \geqslant 2$ from which $R2 = \left(\frac{G-2}{2}\right) R3$

And $R1 = \left(\frac{R2\ R3}{R2 + R3}\right) = \left(\frac{\lambda}{1 + \lambda}\right) R3 = \left(\frac{G-2}{2}\right) R3$

Furthermore the buffer amplifier input impedance =

$$\frac{R1R2\ R3}{R1R2 + R2R3 + R1R3} = \left(\frac{G-2}{2G}\right) R3$$

All the above expressions and relationships form a basis for development of the circuit of Fig. 7d whereby by defining a certain gain (G) all resistor values can be appropriately calculated as illustrated.

e.g. Let $G = 4$, then $R_{in} = \left(\frac{4-2}{8}\right) R3 = \frac{R3}{4}$

If $R_{in} = 10k\Omega$ (the value required for minimum offset taking into consideration R_{out} of ZN425E DAC $\simeq 10k\Omega$) then $R3 = 40k\Omega$.

$R2 = \left(\frac{G-2}{2}\right) R3 = \left(\frac{4-2}{2}\right) R3 = R3 = 40k\Omega$

And $R1 = \left(\frac{G-2}{G}\right) R3 = \left(\frac{4-2}{4}\right) R3 = \frac{R3}{2} = 20k\Omega$

It has been shown that $R1 = \frac{R2\ R3}{R2 + R3}$. The simplest approximation ensuring this relationship is by using a potentiometer as a gain control.

The finalised circuit is shown in Fig. 8.

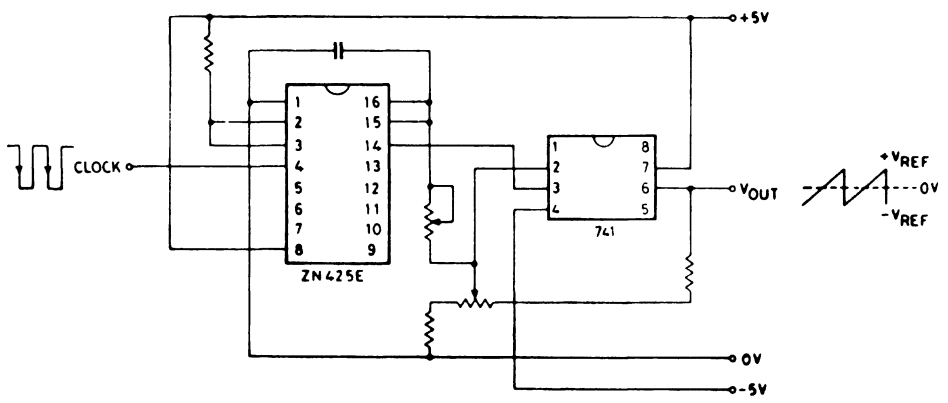


Fig. 8 Bipolar operation, circuit diagram

2.4 Applications

Applications for the use of the ZN425E in its D-A or A-D mode are those where 8-bit accuracy suffices. This is the majority of transducer applications, particularly as system hierarchy is tending to change with the advent of microprocessors, taking the conversion near to the point of measurement. For example, in data acquisition monitoring say 100 channels, it is feasible and economic to use one D-A per channel and multiplex one A-D per 8 channels using a single microprocessor.

If one reference is required to power several converters, additional source current may be provided by an external parallel resistor from supply to reference providing 1.2mA per additional converter in excess of three. In this case the additional earth pin current causes an offset due to a pin resistance of around 0.1Ω.

Specific applications of 8-bit A-D are in conjunction with stress or strain gauges, and many temperature applications. 8-bit D-A may be used for driving chart recorders, programmable power supplies and actuators.

3. RAMP GENERATION

The counter in the ZN425E is very convenient for feeding in a clock to generate a staircase. This facility is used in the majority of applications detailed below.

The count rate which may be used to obtain full ramp accuracy, determined by the worst case settling time of 2μs, is 500kHz, giving a cycling time of around ½ms. However, the counters are capable of being clocked at up to 5MHz, though there will be a loss in staircase accuracy at this speed.

3.1 Continuous

This is illustrated by the circuit of Fig. 9 and is simply accomplished in the normal DAC mode by applying clock pulses to the on chip counter (pin 4) of the ZN425E, which produces a staircase waveform. When the counter is full it returns to its empty state and counting recommences resulting in a continuous ramp.

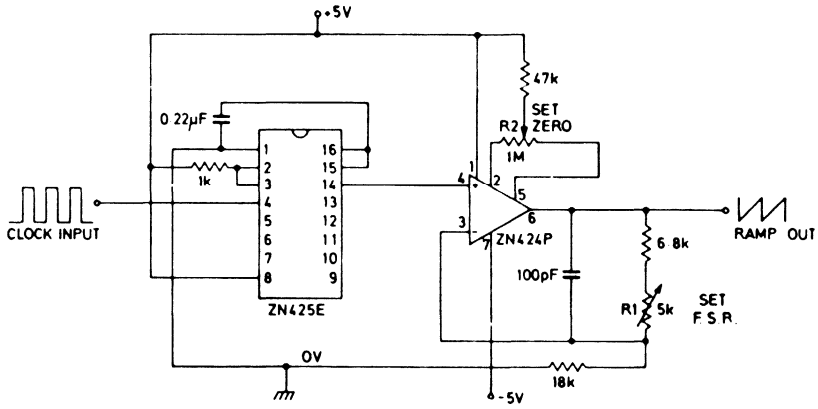


Fig. 9 Precision ramp generator

In order to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary as previously described for the DAC.

The ramp period for 8 bits will be equal to 256 times the clock period, and the maximum amplitude of the ramp from the ZN425E using the internal reference voltage will be V_{REFout} – 1LSB. Therefore, the peak ramp amplitude from the buffer will be this value times the amplifier gain, which, with gain adjustment potentiometer set halfway is

$$2.5V \times \frac{3}{2} = 3.75V.$$

A duty cycle drive signal is sometimes required from an input voltage generated by a potentiometer, for example, for actuator drives, or general power control. This may be provided as shown in Fig. 10, where the ZN425E provides a continuous ramp, against which the voltage reference is compared using a ZN424P. The output from the comparator then provides the duty cycle signal directly.

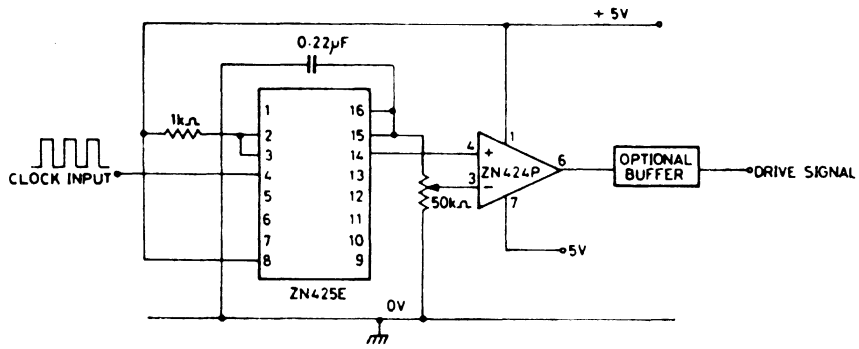


Fig. 10 Duty cycle drive signal

3.2 One shot

A single one shot ramp can be generated quite simply (Figs. 11a and 11b) by using a latch and two capacitors to control the counter reset of a ZN425E DAC. Operation is as follows:

The stationary states of the latch are shown, these being initially determined by the charging times of capacitors C1 and C2, which ensures the counter reset of the ZN425E (Pin 3) is LOW. Upon operating the START button the states of the latch are altered and a HIGH is fed to the counter reset enabling counting of the input clock pulses to commence. The analogue output begins to ramp up until the counter is full at which point the MSB goes LOW altering the latch to its initial resting states. This resets the counter and terminates the ramp. It should be noted that even if the start button is held down at the commencement of the operation, only a one shot ramp results, and not a periodic function.

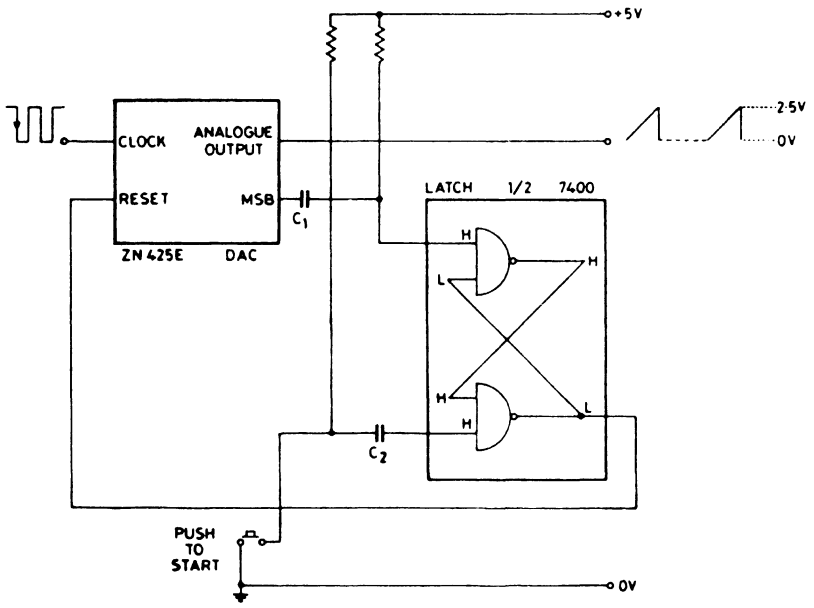


Fig. 11a One shot schematic

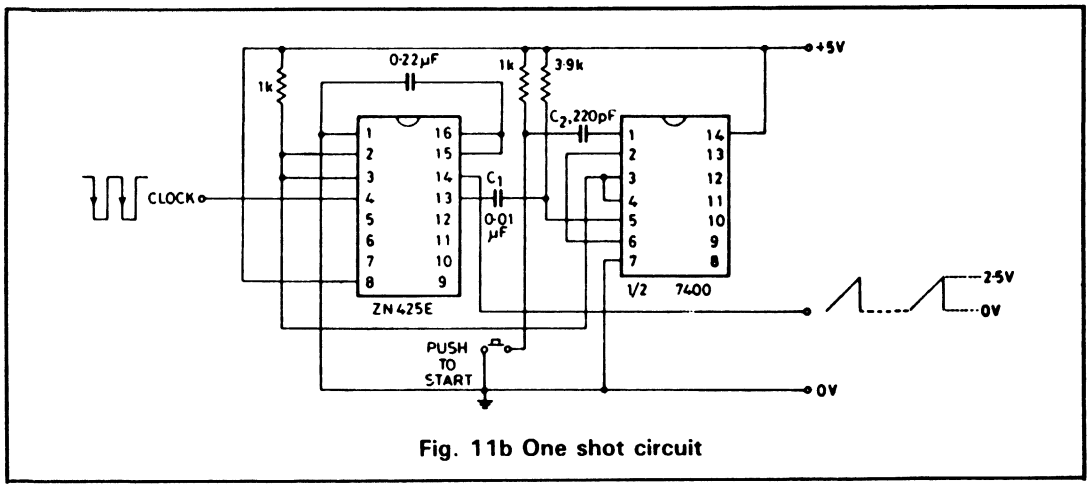


Fig. 11b One shot circuit

A more sophisticated alternative method performing the same function, which replaces capacitors by logic, is outlined in Figs. 11c and 11d. Stationary states of the various logic elements are as indicated. The initial state of the flip-flop is determined by the relative states of the PRESET and CLEAR inputs. Upon switching on the supply the PRESET is held LOW with respect to CLEAR because of the charging time associated with C1 and R1. This results in Q = HIGH, $\overline{Q}$ = LOW, therefore, the counter reset on the ZN425E is LOW.

When the start button is pressed, a pulse from the monostable clears the flip-flop, the counter reset goes HIGH enabling the counter of the input clock pulses to commence. The ZN425E analogue output begins to ramp up until the counter is full, at which point the MSB goes LOW. This is fed to the CLOCK input of the flip-flop which then toggles, reverting to its orginal state, thereby resetting the counter and terminating the ramp. As with the previous circuit only a one shot ramp will be generated even if the start button is held down.

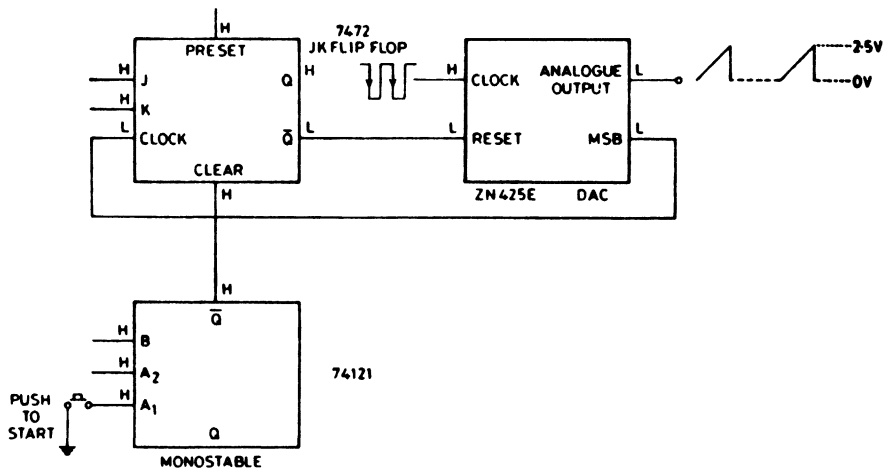


Fig. 11c Alternative one shot schematic

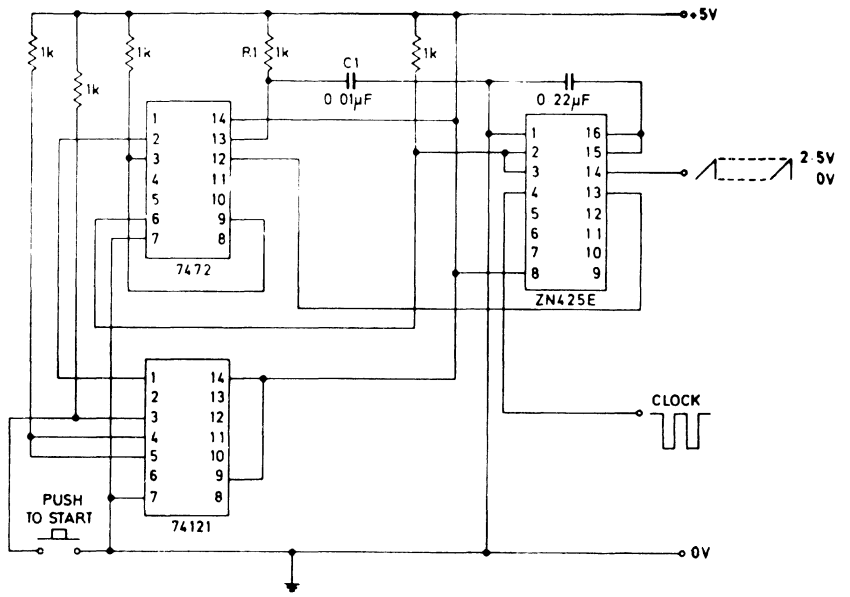


Fig. 11d Alternative one shot circuit

3.3 Weighing and auto zero

The system to be described is intended for either static or on-vehicle load indicating applications and employs integrated circuits from the Plessey Standard Product range. Variations of the scheme are indicated which increase its range of applications. The overall system is shown in the circuit diagrams of Figs. 12a to 12e.

The basic measuring function is a 3½ digit DVM using the dual slope analogue to digital converter principle. This displays an analogue input of up to ±1999mV which is scaled as required. All the DVM digital and control functions are carried out by a ZNA116E.

The DVM input is driven from a separate unity gain summing amplifier which accepts inputs from any number of channels each consisting of transducer and pre-amplifier.

Included in the system is a push button auto-zeroing circuit which automatically sets the output of the summing amplifier to zero. This facility eliminates any small zero errors which may have accumulated in the transducer and pre-amplifier chain or any false zero readings which can appear when on-vehicle systems are operated on uneven ground. For this function the ZN425E 8-bit digital to analogue converter is used. This monolithic integrated circuit also includes an 8-bit binary up-counter and a reference voltage generator and by clocking the counter a voltage ramp of 256 discrete steps is generated. This ramp is level shifted to become symmetrically bipolar with respect to 0V and then applied to the virtual earth of the summing amplifier. This forces the amplifier output through 0V and a comparator circuit detects the 0V condition and inhibits the clock pulses to the counter. The selected ramp output level is therefore held indefinitely unless the auto-zero is switched off when the system reverts to the original zero conditions.

Additional facilities include B.C.D. outputs for data logging purposes and an overload alarm system with warning indications.

The alarm system uses two comparators, into which are set two analogue levels, one corresponding to a preset percentage of full load and the other to full load. When the load reaches the first level a 1Hz square wave output is available and a separate output gives a continuous signal at the second level. These outputs may be wire-ORed or used separately to drive visual or audible alarms.

It is not essential for the DVM function to be fully bipolar in this application because negative readings occur only as small zero errors. A minor modification enables the circuit to display lower accuracy negative readings at the same time eliminating one of the ZN423 reference generators.

Further modification, appropriate for some applications, results in a 3 digit display with a 1Hz flashing leading zero to indicate a small negative zero error.

This approach, using a mix of standard function integrated circuits gives maximum system flexibility. For example, an on-vehicle application may require separate auto-zero functions on a number of axles or an overload alarm indication may require duplication. By adding the appropriate integrated circuits the system can be tailored to suit a range of vehicle requirements with a minimum of chip function redundancy and therefore minimum cost.

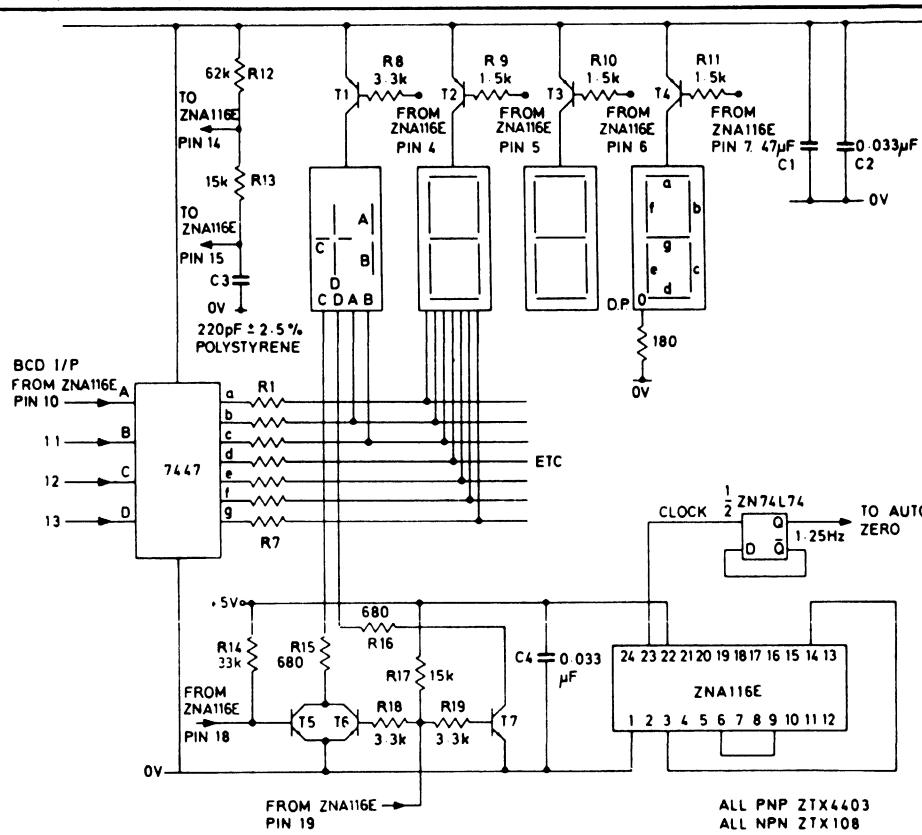


Fig. 12a Display/digit circuit

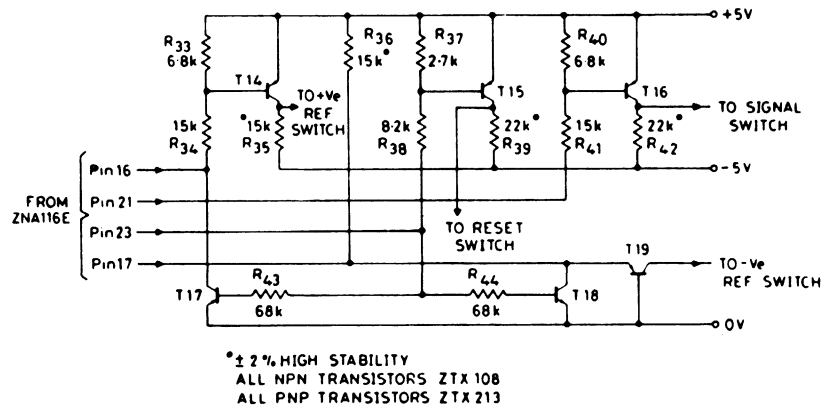


Fig. 12b Analogue switch

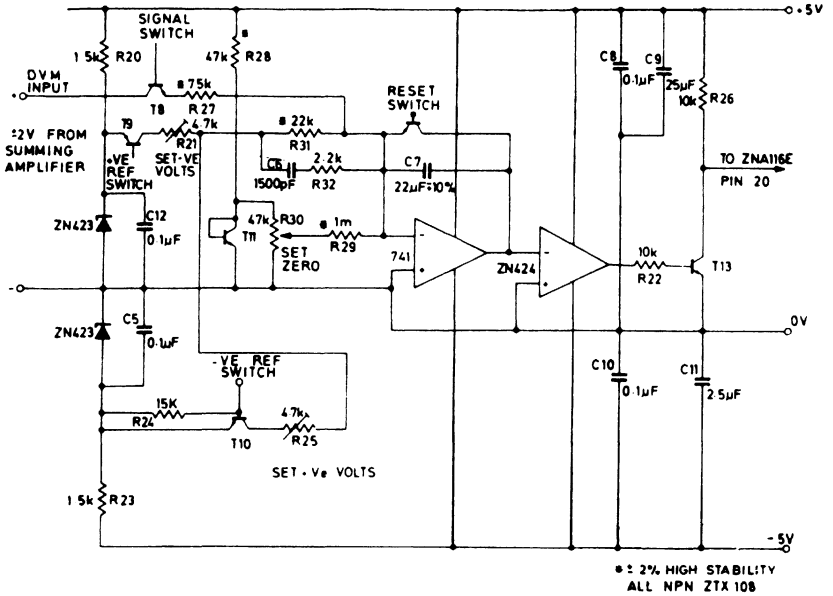


Fig. 12c Dual slope integrated circuit

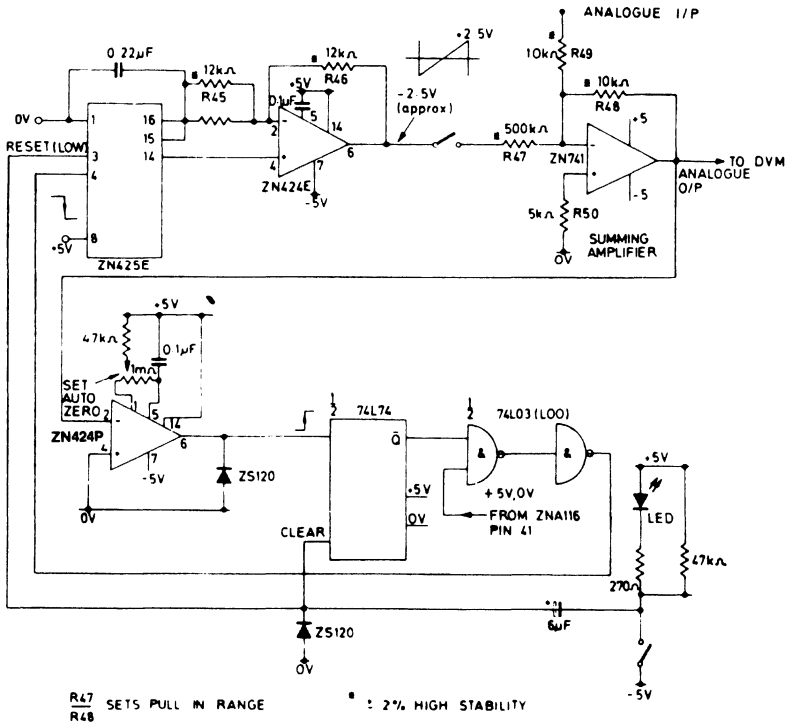


Fig. 12d Auto zero circuit

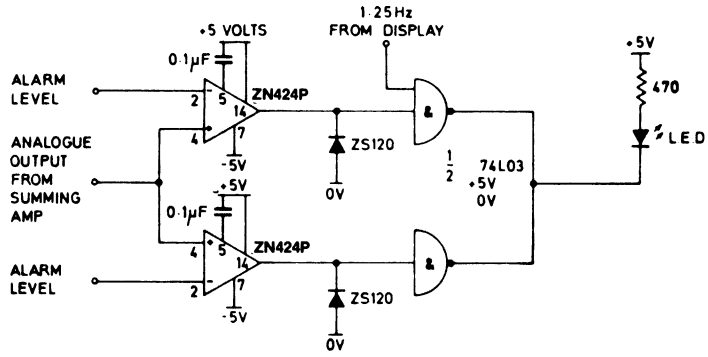


Fig. 12e Alarm circuit

3.4 Peak detect

A peak detect circuit may be constructed simply using the form of A to D system shown in the schematic of Fig. 13. When left running continuously it will hold the maximum input signal level it is able to track i.e. peak detect.

After application of a reset pulse, the state of the comparator enables clock pulses from the Schematic trigger circuit to be fed to the counter of the ZN425E. The analogue output begins to ramp up until it attains the level of the analogue input voltage at which point the comparator changes state and inhibits further clock pulses. Therefore, the analogue output is held and stored digitally in the bits of the converter. It will continue to hold this level until a further increase in analogue input voltage changes the comparator state, enabling the clock, and the sequence is repeated.

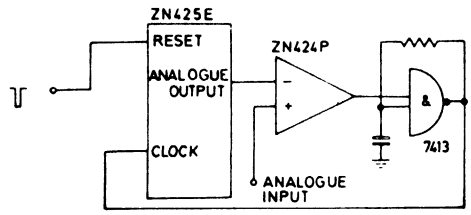


Fig. 13 Peak detect schematic

3.5 Channel Selector

Another interesting application of the A-D principle is for a channel selector in communications, e.g. citizens or amateur band. In effect it replaces a multiway switch, mechanically limited to 24 or 30 channels, by a 10 turn potentiometer which can be used with the system of Fig. 14 to generate many more discrete steps, typically 64 but up to 256.

The ZN425E with internal counter, provides the A-D conversion function, using a single 7400 package for external logic, and a high performance ZN424P op-amp as comparator. A 7413 dual Schmitt trigger provides the necessary clock and conversion oscillators, no sync is needed here. Channel selection is by the 10 turn potentiometer 'Main Tune' or, optionally, by preset potentiometers, to preferred channels. Resistance values for the pots are not critical.

The binary output is converted to BCD by the 74185 and latched to provide a steady output signal i.e. when a particular channel has been selected no jumps occur during cycling. The conversion oscillator periodically checks the state of the input voltage, by a fresh conversion on the ZN425E, and updates the latches when the status command indicates that the conversion is complete. The BCD signals drive

7-segment indication of channel number and provide the drive outputs for either a modulo-N digital synthesiser, a crystal-bank synthesiser, or a crystal selector. Features of the system are:

1. Bi-directional, quasi-continuous tuning on a single control.
2. Electronic tuning lock.
3. Simple switching between 'tune' and 'preferred channel' operation.
4. Preferred channels selected by preset potentiometers operating through to the synthesiser. Channels are user-alterable.
5. Inherent non-volatile 'memory' on potentiometers.
6. Channel number indication shows channel actually in use, particularly suitable for non-co-channel working, repeaters, etc.

In addition, a scanning facility can be easily added if the receiver used has a squelch switched output.

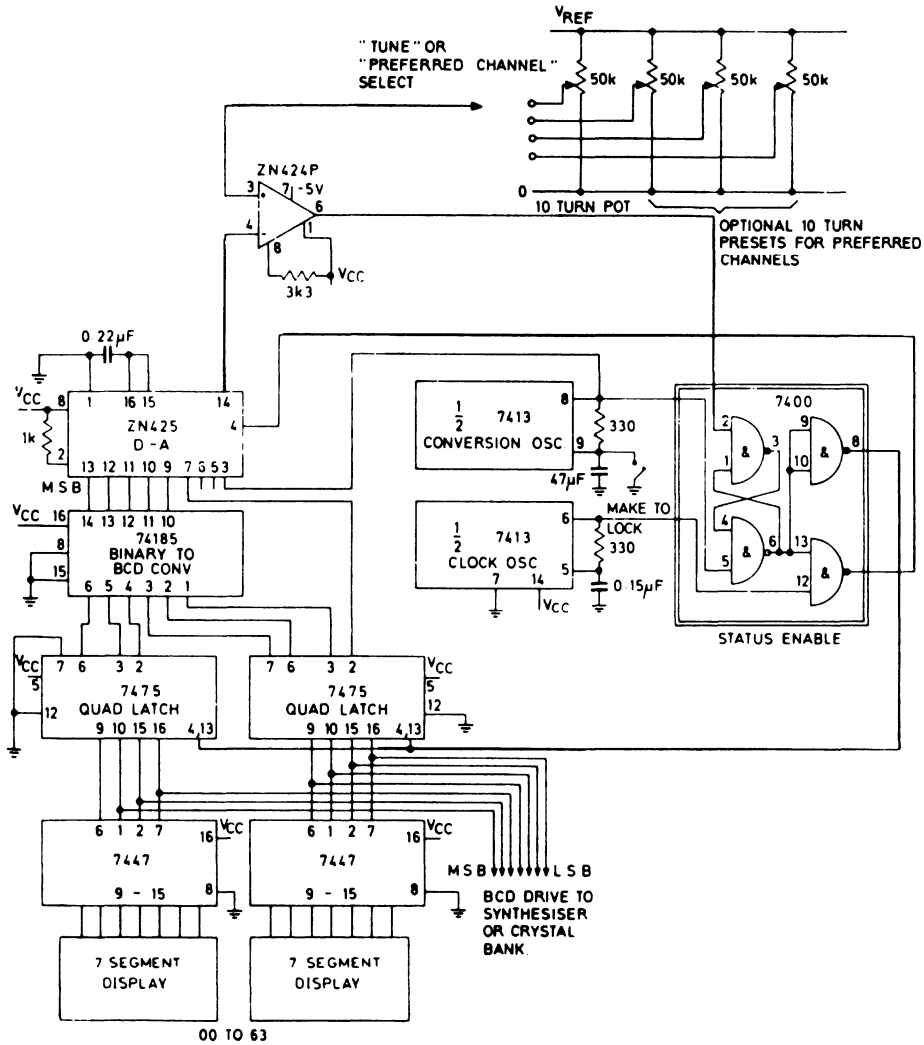


Fig. 14 Channel selector, 64 way

3.6 Bargraph display drive system

The ZN425E may be used in its continuous ramp mode very advantageously in conjunction with linear light emitting diode (LED) displays, e.g. Bargraphs. This is because the LED displays lend themselves to being accessed in a matrix fashion using a time sharing or multiplexing technique. This allows a reduction in the number of connections required, to m + n in an array of m n diodes (Fig. 15a). This reduction in connections also allows a simplification of the drive system, as described below.

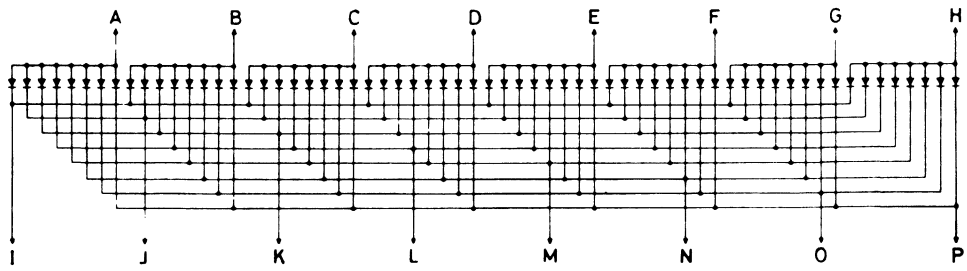


Fig. 15a Diode matrixing connections

The simplest techniques for providing for a bar output whose length is proportional to an analogue input is shown in Fig. 15b. The ZN425E is driven in its continuous ramp mode. The six most significant digits from the counter are then decoded into two lots of 1 out of 8 drives. These drives then access the LEDs in a multiplexed fashion, so that the 64 LEDs are accessed once each in turn in a complete scan cycle. A high clock frequency is selected which ensures that the flicker rate is fast enough and therby indistinguishable to the eye.

At the same time as the LED scan cycle is taking place, the ZN425E provides a staircase analogue output, as shown. This is compared with the analogue input in a comparator, whose output controls the display enable. Thus while the ramp is less than the analogue input, the LEDs being scanned are enabled (the start of the Bargraph line), while once the ramp output is larger than the analogue input, the drives to the LEDs further along the line are inhibited. This, therefore, provides an illuminated bar length proportional to the analogue input.

This system as it stands suffers from a minor disadvantage, in that the duty cycle for accessing each LED is 1/m n, or 1/64 for the case of Fig. 15b. Although the LEDs become more efficient with pulsed operation, 1/64 duty cycle does not provide adequate brightness for some applications.

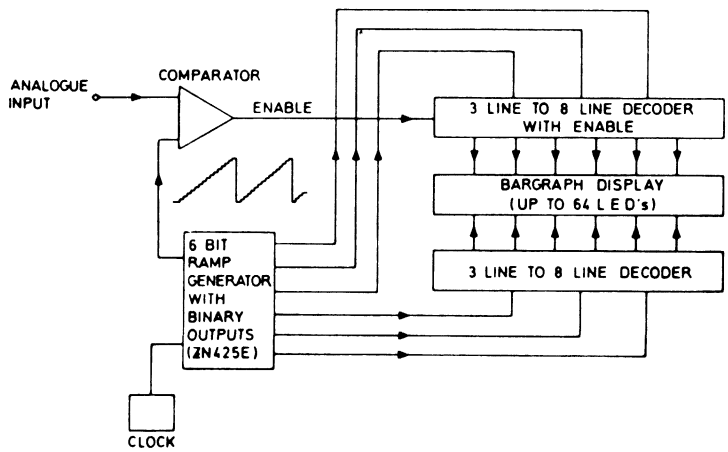


Fig. 15b Simple bar display schematic drive system

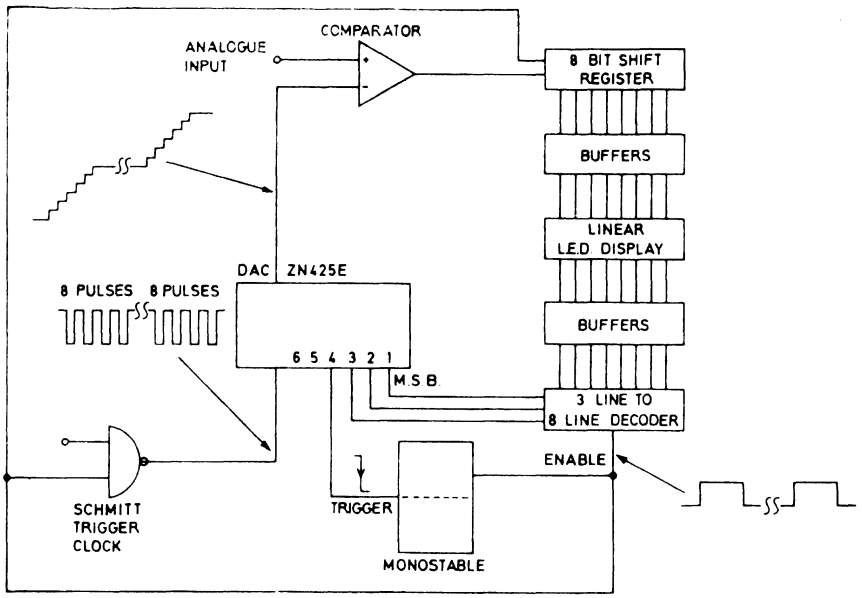


Fig. 15c Improved bar display schematic drive system

A technique to overcome this objection is shown in outline in Fig. 15c. The technique used here is to load a shift register rapidly serially, and subsequently use this register to provide LED multiplex drives in parallel. This means that the duty cycle for accessing the LEDs is improved (for a 64 LED array) from 1/64 to just less than 1/8. This is quite sufficient for acceptable brightness in virtually all applications.

This system operates as follows. While the monostable is in its mode of loading the shift register, the ZN425E staircase output increases in 8 discrete steps. Simultaneously the shift register is loaded with the comparator output to provide serial to parallel conversion. The comparator output is thus effectively changed from serial access to parallel access of the linear LED array.

When the monostable changes over to its (longer period) display mode, the LED array is accessed, and the LEDs are driven or otherwise according to the enable or disable information stored in the shift register. The display is incidentally disabled while the mono is loading the register.

To provide an example of operation, suppose the bar is to have the first 37 LEDs displayed, with the rest blanked. Starting from the ZN425E being reset and the mono in its register load state, operation is as follows.

The mono allows eight clock pulses through the gate to the ZN425E, after which the ZN425E count pulse retriggers the mono. These eight pulses generate the first eight steps from the analogue output, which produce from the comparator a continuous display enable (say logic 1). These are loaded into the shift register which thus finishes with 11111111 in parallel to the LED display.

At this point the mono is tripped into its display mode, and the counter has reached 8 (or 001 000). However the decoder must access the first eight LEDs, so that the second decoder output is connected to the first set of LEDs. These are all illuminated.

During the second register load period, the cycle is repeated, with again all ones being loaded into the register which subsequently brightens up the second eight LEDs (9-16). The same occurs during the third and fourth mono cycles, lighting up the first 32 LEDs.

During the fifth register load period, the analogue output goes up a further eight steps. However after the fifth step the comparator changes over to load zero for the remainder of this period into the shift register. If loaded from the left the register will then finish up as 00011111. Subsequently during the mono display period LEDs 33 to 37 inclusive will be lit, but 38 to 40 will be blanked off.

The sixth to eighth mono cycles will load zeros into the shift register, blanking off LEDs 41 to 64. The full LED scan cycle is therefore completed with the desired effect.

Typical system clock rates are 400kHz, and typical monostable periods 500μs for the values shown.

An actual circuit to achieve this is shown in Fig. 16 and it may be seen that this is elegant and simple. The type of display which may be accessed in this way is the Bowmar Microstic R1M-053-66A, which is connected in eights on its common anodes. This has 64 red LEDs and a further two LEDs at the ends, one to show the display is working, and the other for over-range. Similar techniques may be used with the 106 LED version.

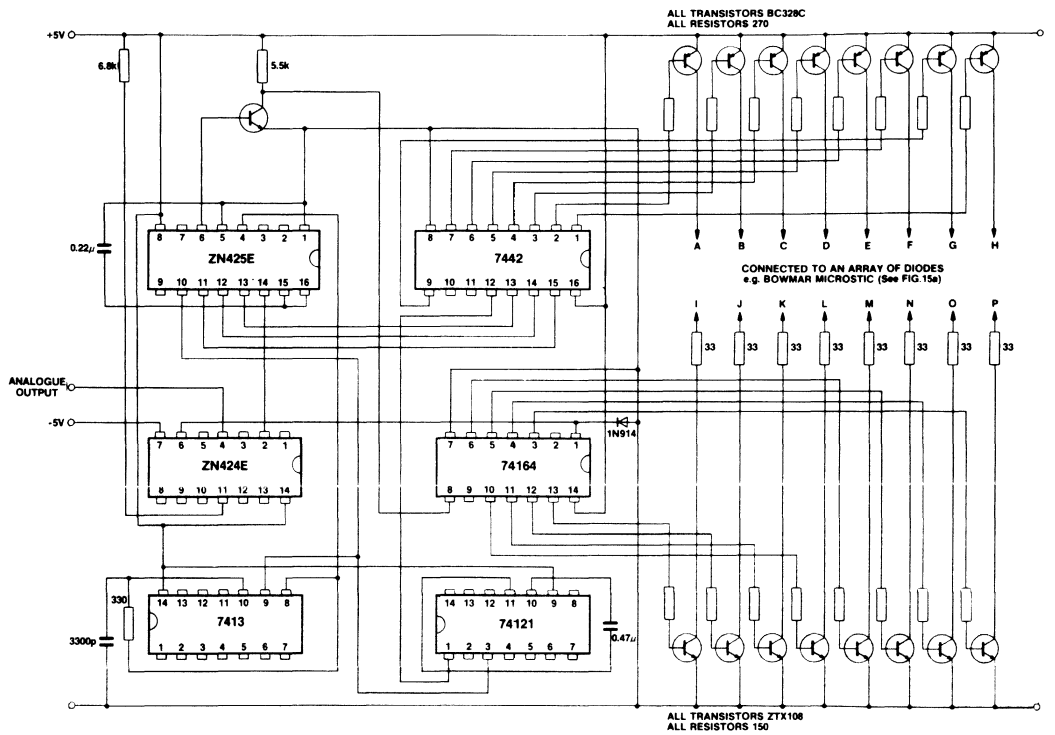


Fig. 16 Column display drive system

3.7 Up down or tracking

The counter on the ZN425E is only an up counter, and some systems, e.g. tracking converters or servos, amy require an up/down counter. This is conveniently provided externally, e.g. the 74193 using the ZN425E purely in its D-A converter mode and ignoring the counter (Fig. 17). While this may appear to be inelegant it is nevertheless economically sound.

The reference supply to the D-A section of the ZN425E has been purposely left on an uncommitted terminal, so as to allow connection either from its own reference or from an external reference. The point about an external reference is that it allows a multiplying effect, in that the analogue output is proportional both to the binary code and the reference voltage. For this reason this type of DAC is called a multiplying DAC.

4. MULTIPLY/DIVIDE

4.1 Multiplier

Practical limits in multiplying voltages are 0 and 3V.

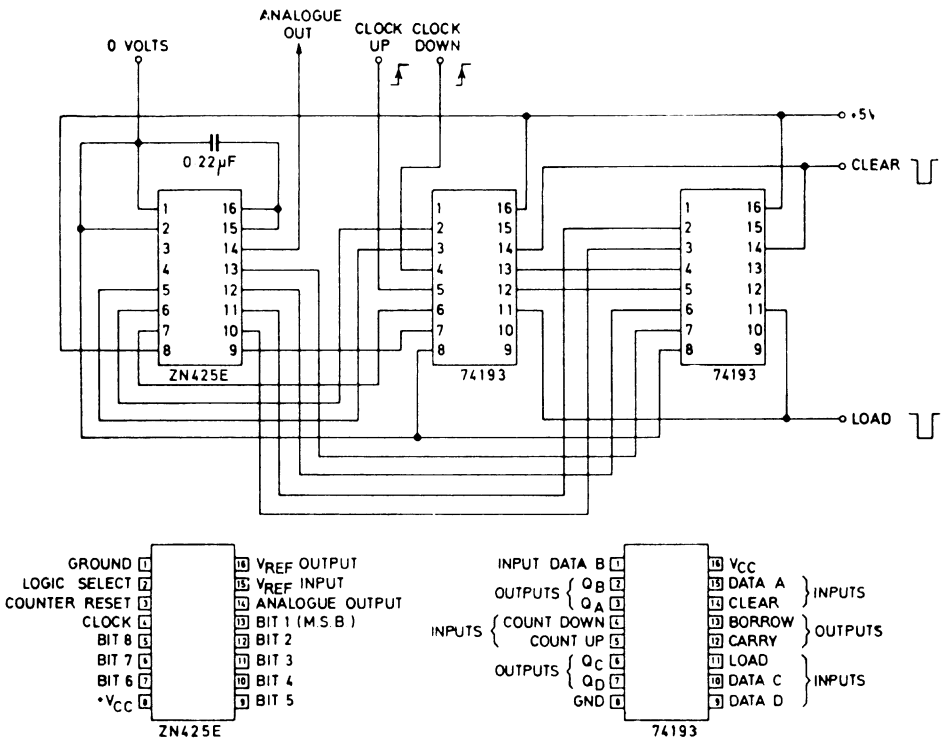


Fig. 17 Up/down counter or tracking DAC circuit

4.2 Variable frequency divider

If a ZN425E is operated in its continuous ramp mode in conjunction with a comparator whose output is fed back to the counter reset, a variable frequency divider can be constructed as shown in Fig. 18a. Here an analogue voltage can be used to control the number of steps before reset is applied, the overall effect being to provide variable frequency division under the control of a potentiometer.

4.3 Voltage controlled oscillator

The schematic of Fig. 18a may also be used as a voltage control oscillator. However the frequency is the inverse of the applied voltage, though the period is, of course, proportional. The corresponding circuit of Fig. 18b gives an output frequency or pulse rate which is inversely proportional to applied voltage as shown in Fig. 18c. It is, however, in some cases more desirable to produce an output frequency directly proportional to applied voltage. This is accomplished by the circuit depicted in Figs. 19a and 19b and involves the use of an inverse scaler described in the next section, for which a brief mention is necessary to understand the basic operation of the VCO.

By using a DAC in the feedback loop of an operational amplifier an output voltage is derived which is inversely proportional to a digital input number to the DAC. Clock pulses applied to the DAC counter will produce a repetitive output waveform which is a hyperbolic $\frac{1}{n}$ function. This waveform is applied to the inverting input of a comparator whilst the analogue input voltage to be frequency converted is applied to the non-inverting input. At the instant they become equal the comparator changes state and operates the Schmitt trigger which resets the DAC counter. The result is a train of negative going pulses whose frequency is directly proportional to the applied input voltage. This follows simply because if F_{Clock} = clock frequency to the DAC counter, and F_{out} = output frequency, then $F_{out} = \frac{F_{Clock}}{n}$ where n = digital input number and analogue input voltage to the comparator V_{in} $\alpha \frac{1}{n}$

Therefore, F_{out} αV_{in} and the appropriate characteristic is shown in Fig. 19c.

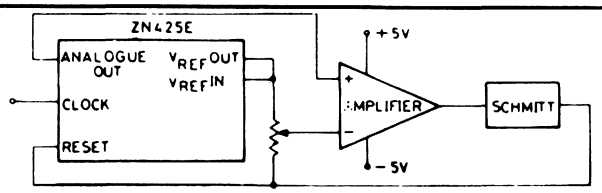


Fig. 18a Variable frequency divider or VCO schematic

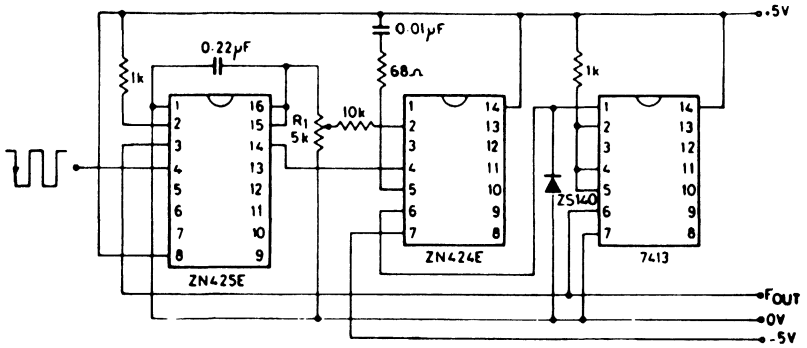
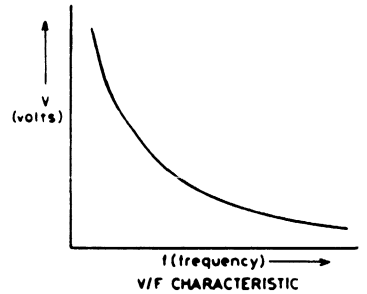


Fig. 18b Variable frequency divider or VCO circuit



V/F CHARACTERISTIC

Fig. 18c VCO characteristics

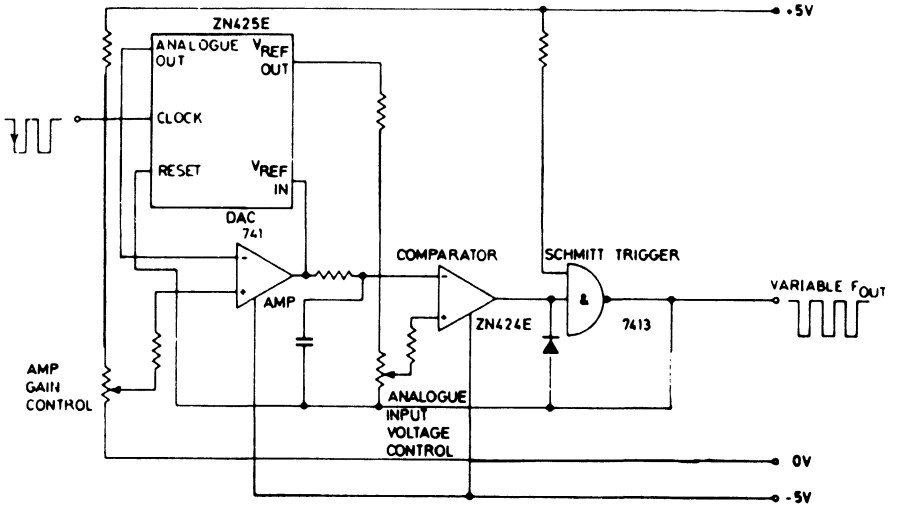


Fig. 19a Schematic of VCO giving frequency proportional to voltage

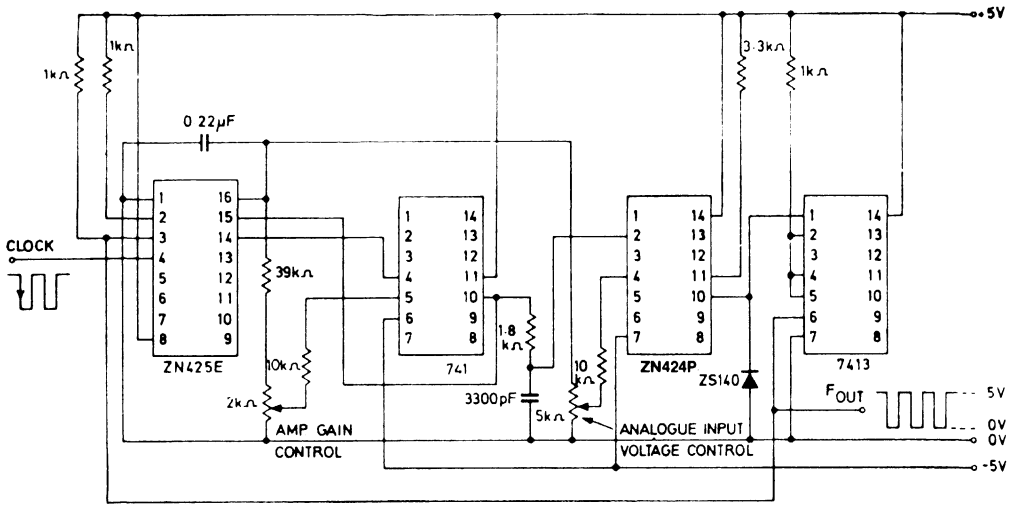
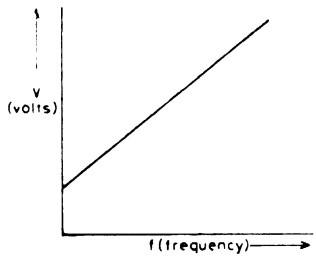


Fig. 19b Circuit of VCO giving frequency proportional to voltage



5091 V/F CHARACTERISTIC

Fig. 19c VCO characteristics

5. FUNCTION GENERATION

By virtue of the multiplying function, the ZN425E may also be used for function generation as described below.

5.1 Inverse scaler

If a DAC is operated in the feedback loop of an operational amplifier then the amplifier gain is inversely proportional to the input digital number or code to the DAC. The version giving scaling inversely proportional to positive voltage is shown in the schematic of Fig. 20a and the practical circuit of Fig. 20b.

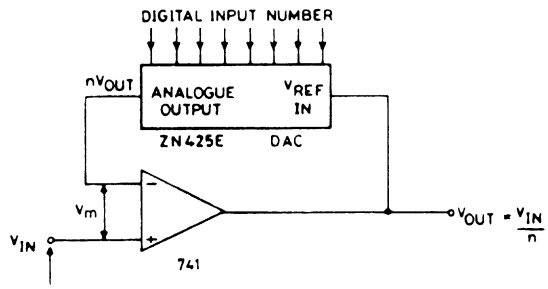


Fig. 20a Inverse scaler schematic

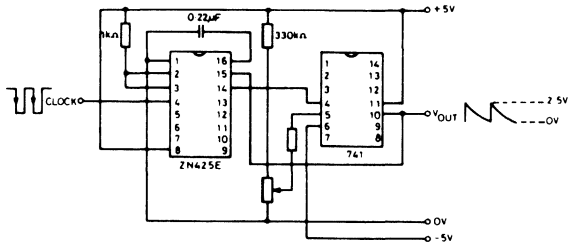


Fig. 20b Inverse scaler circuit

If A = open loop gain of the operational amplifier, and n is a fractional number representing any digital input (00000000 to 11111111 for 8 bits), that is a fractional number between 0 and $\frac{255}{256}$ then from the diagram $V_{out} = AVm$, and $Vm = (V_{in} - n\,V_{out}) \therefore V_{out} = A(V_{in} - n\,V_{out})$ from which

$$V_{out}(1 + An) = AV_{in} \quad \frac{V_{out}}{V_{in}} = \frac{A}{1 + An}$$

Since $An \gg 1$, $(A \simeq 100{,}000)$ then $\frac{V_{out}}{V_{in}} = \text{Gain (G)} \simeq \frac{A}{AN} = \frac{1}{n}$

For $n = 1LSB = \frac{1}{256}$ then the maximum allowable input voltage V_{in} to prevent saturation

$(V_{sat} \simeq 4V) = \frac{4}{256} \simeq 15mV.$

If n = 0 then G = A and for a fixed input level the amplifier output will normally be equal to the saturation voltage since $A \simeq 100{,}000$.

The complementary mode (scaling inversely proportional to negative voltage) is shown in Fig. 20c (schematic) and Fig. 20d (practical circuit).

$$V_m = \left[V_{in} - \left(\frac{V_{in} - n\,V_{out}}{R_1 + R_F}\right)\right], \text{ and } V_{out} = -AV_m$$

If $\frac{R_I}{R_F} = F_I$ = inverting feedback return then

$$V_{out} = -A\left[V_{in} - \left(\frac{V_{in} - n\,V_{out}}{1 + F_I}\right) F_I\right]$$

From which

$$V_{out} = -\left[\frac{A\,V_{in}}{1 + F_I + nAF_I}\right]$$

If the input voltage V_{in} is negative with respect to ground, then

$$\text{Gain (G)} = \left[\frac{A}{1 + F_I + nAF_I}\right]$$

If we make $F_I = 1$, i.e. $R_I = R_F$ then $G = \left[\frac{A}{2 + nA}\right]$

But $nA > 2$ (since $A \simeq 100{,}000$)

and $G = \frac{A}{nA} = \frac{1}{n}$ as with the non-inverting circuit.

Figs. 20a and 20c illustrate both types of inverse scalers, where a repetitive waveform of a $\frac{1}{n}$ function is generated by feeding clock pulses to the counter of the DAC.

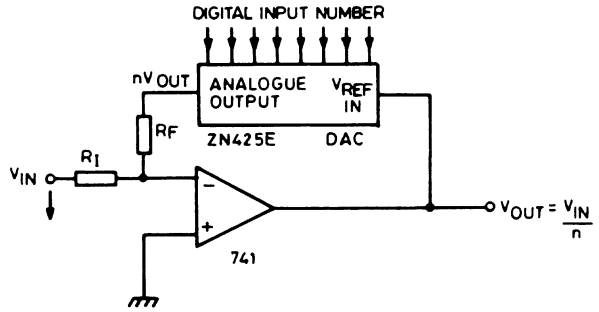


Fig. 20c complementary inverse scaler schematic

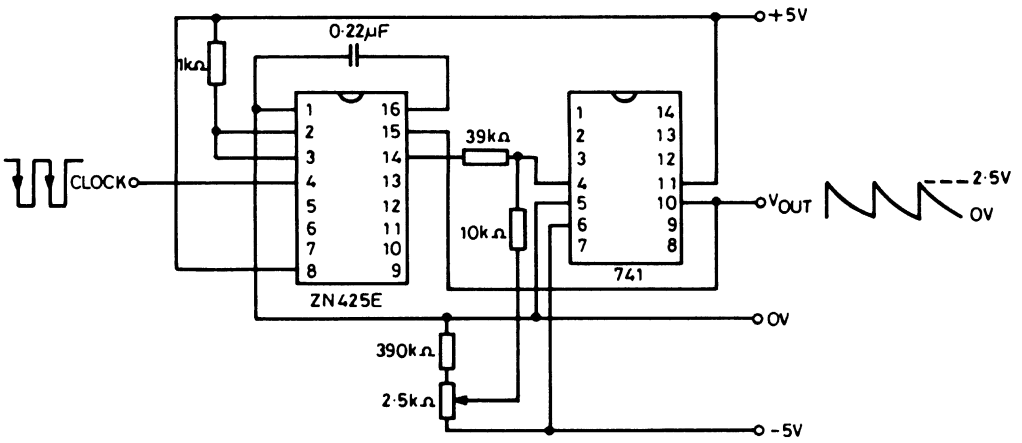


Fig. 20d Complementary inverse scaler circuit

5.2 Parabola

The multiplying action of the ZN425E may be used to generate a parabolic waveform shown schematically in Fig. 21a and a practical circuit Fig. 21b.

Basically the circuit operates as follows;

A continuous ramp output is generated by feeding clock pulses to the counter of a ZN425E DAC using its internal reference which is buffered, level shifted, and finally inverted using two operational amplifiers, so that the inverted ramp starts at a peak amplitude ($V_{1\ REF}$ = 2.5V) and decreases linearly to zero. This is then used as an external reference supply for a second ZN425E DAC whose bits are connected to the first DAC for synchronous clocked operation. The resulting analogue output from the second DAC is a repetitive parabolic waveform whose peak amplitude is equal to $\frac{V_{1\ REF}}{4}$ = $\frac{2.5}{4}$ = 0.625V.

This follows because,

If N = a fractional number representing the digital input to both DACs then the analogue output voltage from the first DAC = An (where A = $V_{1\ REF}$ = 2.5V).

This is then inverted and level shifted to provide the reference voltage to the second DAC = (A − An) = $V_{2\ REF}$.

Therefore the analogue output from the second DAC = n (A-An) = An − An^2 which is the equation of a parabola about the x axis of the form $y = ax^2 + bx + c$.

Peak amplitude of the parabola occurs when n = $\frac{1}{2}$

for which $V_{out} = \frac{1}{2}\left(A - \frac{A}{2}\right) = \frac{A}{4} = \frac{V_{1\ REF}}{4}$ as stated.

It should be noted that the ramp output from the non-inverting buffer amplifier will inherently have a gain greater than unity, and therefore its peak amplitude will be some factor in excess of $V_{1\ REF}$. However the ramp inverter and level shifter introduces corresponding attenuation to compensate this so that gain and level shift controls provide adequate adjustment in obtaining the desired inverted ramp output of peak amplitude.

$A = V_{1\ REF} = 2.5V.$

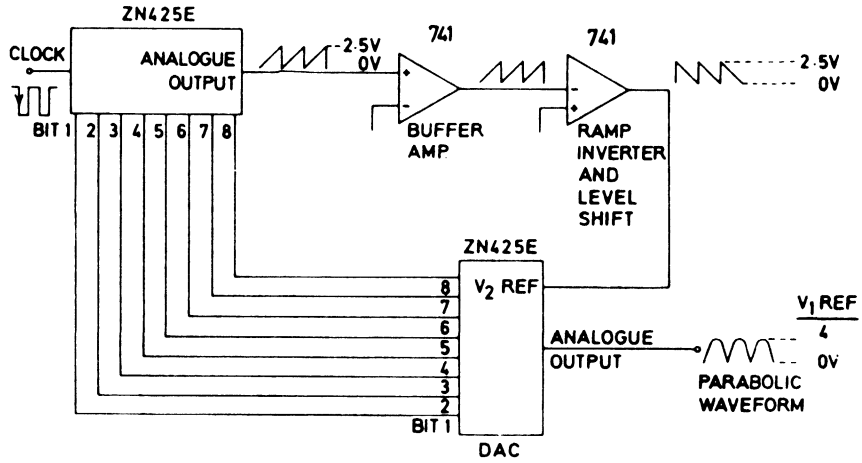


Fig. 21a Parabolic waveform generator schematic

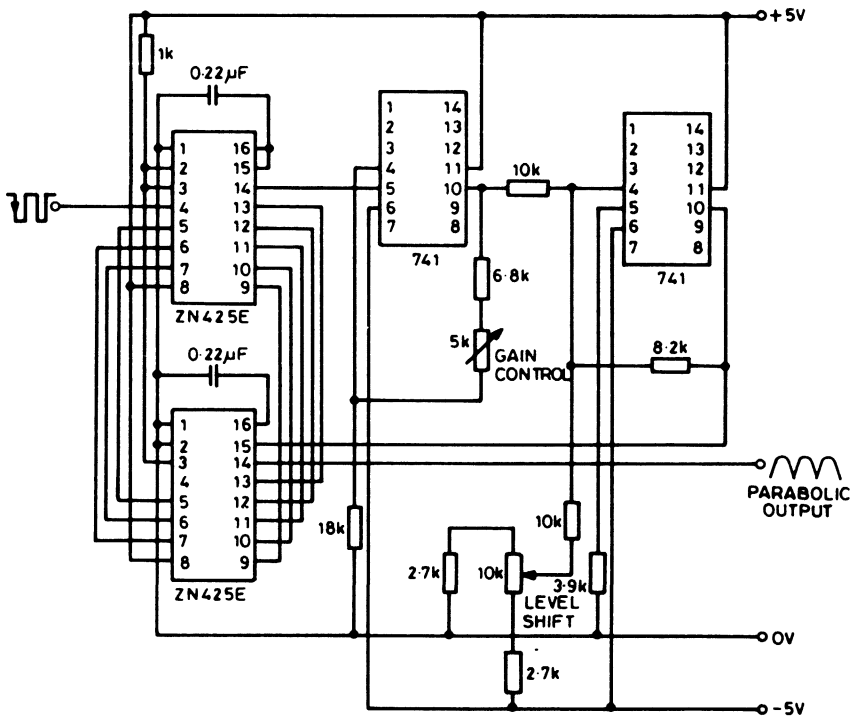


Fig. 21b Parabolic generator circuit

5.3 Log Approximation

A more complex function y = log n can be performed with the aid of previously described building blocks. A schematic arrangement as shown in Fig. 22a and the corresponding practical circuit of Fig. 22b provides a repetitive logarithmic relationship. The basic method is as follows.

An inverse scaler is used to generate an output voltage which is inversly proportional to a digital input number n to a ZN425E DAC. This voltage is then converted to a frequency or pulse rate using a VCO whose output frequency is proportional to an applied voltage. The derived train of pulses of varying mark to space ratio are then fed into the counter of a final ZN425E DAC, these are integrated and a logarithmic output

$$\left(\frac{1}{n}\,dn = \log n\right)$$ is obtained.

The period of the analogue $\frac{1}{n}$ function is dependent upon the input frequency to the inverse scaler. To rapidly convert this function to a pulse train and to generate a sufficient number of pulses for integration during this period, the clock frequency to the VCO derived from the Schmitt trigger must be high. The lower input frequency to the inverse scaler in synchronism with this clock frequency is obtained by using two 7493 dividers and equals the clock frequency divided by 256. For the CR values indicated in the Schmitt trigger $F_{Clock} \simeq 512kHz$ therefore the input frequency to the inverse scaler $= \frac{512 \times 10^3}{256}Hz = 2000Hz$.

And the output repetition frequency of the $\frac{1}{n}$ function $= \frac{2000}{256}$ Hz, for which the period $= \frac{256s}{2000} = 128ms$.

Some means must be incorporated of resetting the counter on the final ZN425E DAC and thereby the logarithmic analogue output to zero at the completion of a full cycle of input pulses. Otherwise the analogue output would continue to increase with each cycle of pulses until it equalled the internal reference voltage, resulting in a 3 cycle logarithmic waveform. This is accomplished by using the negative going edge from the 4th significant bit which in fact resets the counter on the final DAC the completion of a full cycle of input pulses. Whereas to be strictly correct resetting should be effected from the MSB; bit 4 having been selected purely for convenience as it allows the logarithmic characteristic to be more easily displayed on the oscilloscope, since it accounts for a greater proportion of the output waveform, with negligible loss in amplitude.

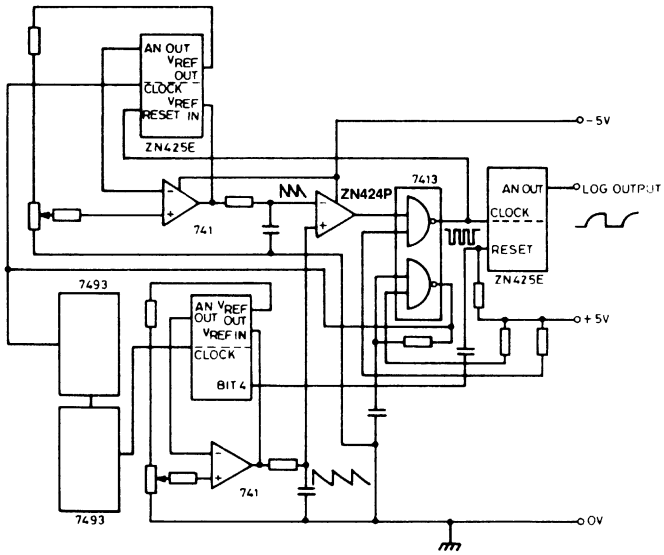


Fig. 22a Logarithmic waveform generator schematic

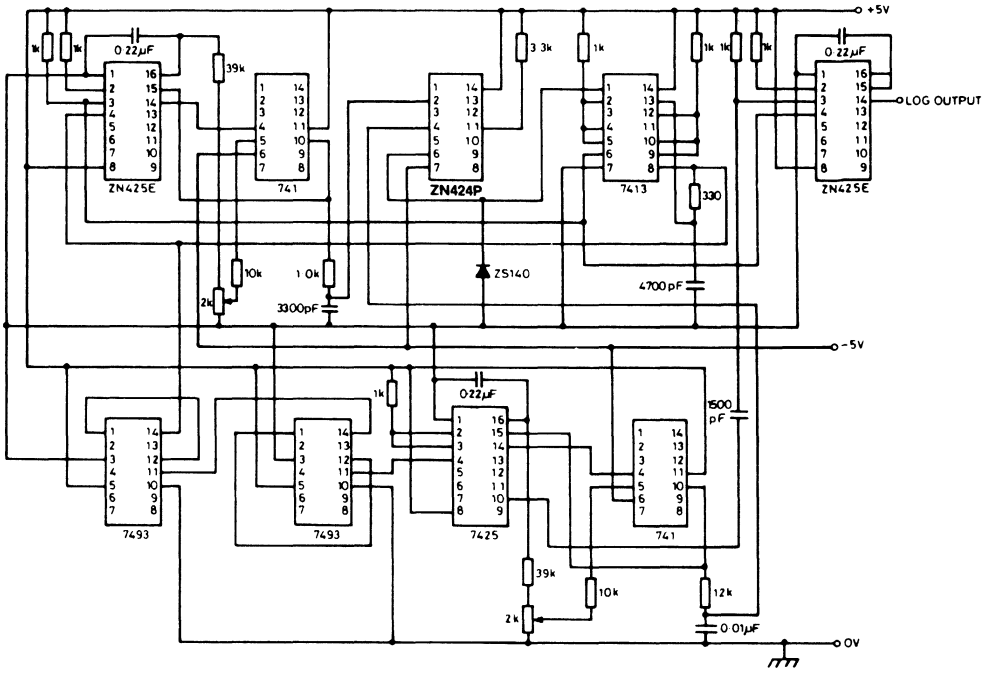


Fig. 22b Logarithmic waveform generator circuit

Microprocessor Interfacing using the ZN427/ZN428 Data Converters

Conventional analogue I/O systems for Microprocessors are generally high accuracy, high cost, hybrid module/P.C. board assemblies, available in only one fixed configuration of I/O channels, (i.e. 16 Input and 2 Output channels). This application note describes how a low cost analogue I/O system may be produced for the 6800 microprocessor using Plessey ZN427 A-D and ZN428 D-A converters with the 6820/6821 peripheral interface adaptor (PIA) I.C. This combination produces a versatile system which can be configured to the designer's particular I/O requirements, and which can also be expanded without major modifications to the hardware. The advantages of interfacing to the microprocessor via the PIA are that it provides a simple, easily expandable system, without additional address decoding and line buffering hardware, and it also simplifies timing problems associated with a direct bus interface.

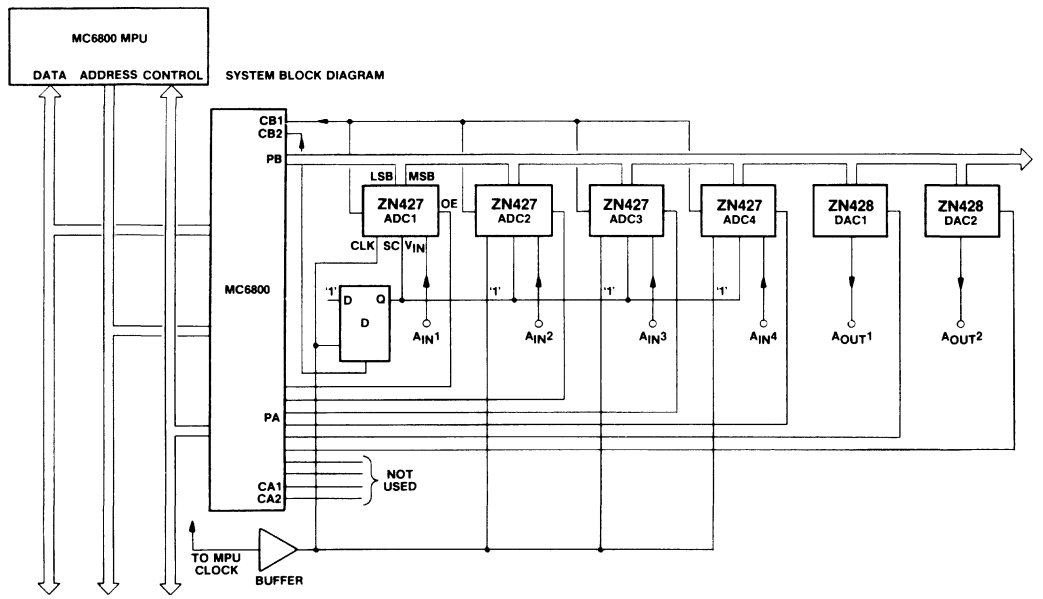


Fig. 1 System block diagram

The ZN427 A-D converter

The ZN427 is an 8-bit, successive approximation A-D converter. It features fast 15μs conversion time, three-state outputs to permit bussing on common data lines and no missing codes over the full operating temperature range. The ZN427 contains a voltage switching D-A converter, a 2.5V precision band gap reference, a fast comparator, successive approximation logic, and three-state output buffers.

Operation of the ZN427 is best described with reference to the timing diagram - Fig. 3. Conversion is initiated by a START CONVERT (SC) pulse which can be applied asynchronously with respect to the ZN427 clock providing the following criteria are met.

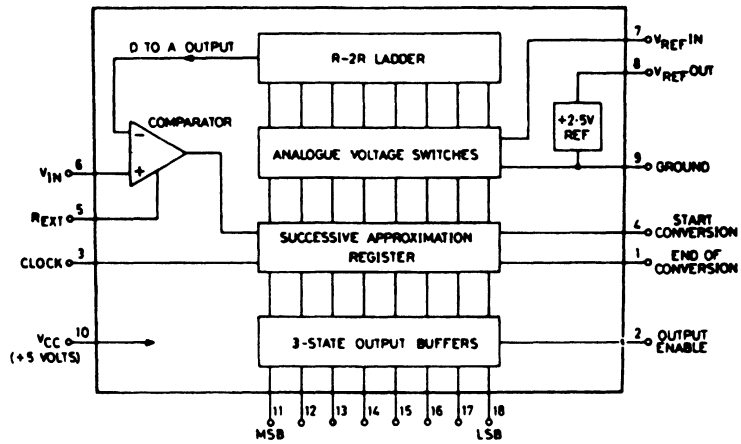


Fig. 2 ZN427 logic diagram

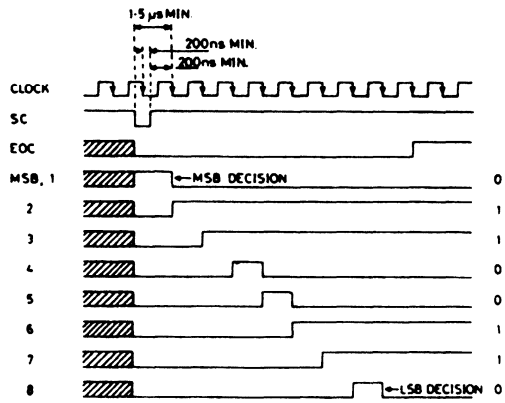


Fig. 3 Timing diagram

1. The leading edge of the SC-pulse should precede the first active (negative going) edge of the clock (after the trailing edge of the SC pulse) by at least 1.5μs to allow for MSB setting.

2. The trailing edge of the SC pulse must not occur within $\pm$ 200ns of a negative going edge of the clock.

3. As a special case of conditions (1) and (2) the SC pulse may be coincident with, and of the same duration as, a negative going clock pulse. Application of the SC pulse sets MSB to a '1' level and all other bits to a '0', which produces a voltage output from the D-A converter of $V_{REF\ IN/2}$.

This value is compared with the input voltage V_{IN}, and a decision is made on the first negative clock edge to set the MSB to '0' if $V_{REF\ IN/2} > V_{IN}$, or else to keep it at '1', Bit 2 is switched to '1' on the same clock edge, and on the next edge a decision is made about Bit 2, again by comparing the D-A output with V_{IN}. This process is repeated for all eight bits so that when the END OF CONVERSION (EOC) output goes high the digital output from the converter is a valid representation of V_{IN}. The binary output is latched until the next START pulse. The three-state data outputs are OFF (high impedance) when OUTPUT ENABLE (OE) is an '0' and are enabled when the OE input is taken to '1'.

The ZN428 D-A converter

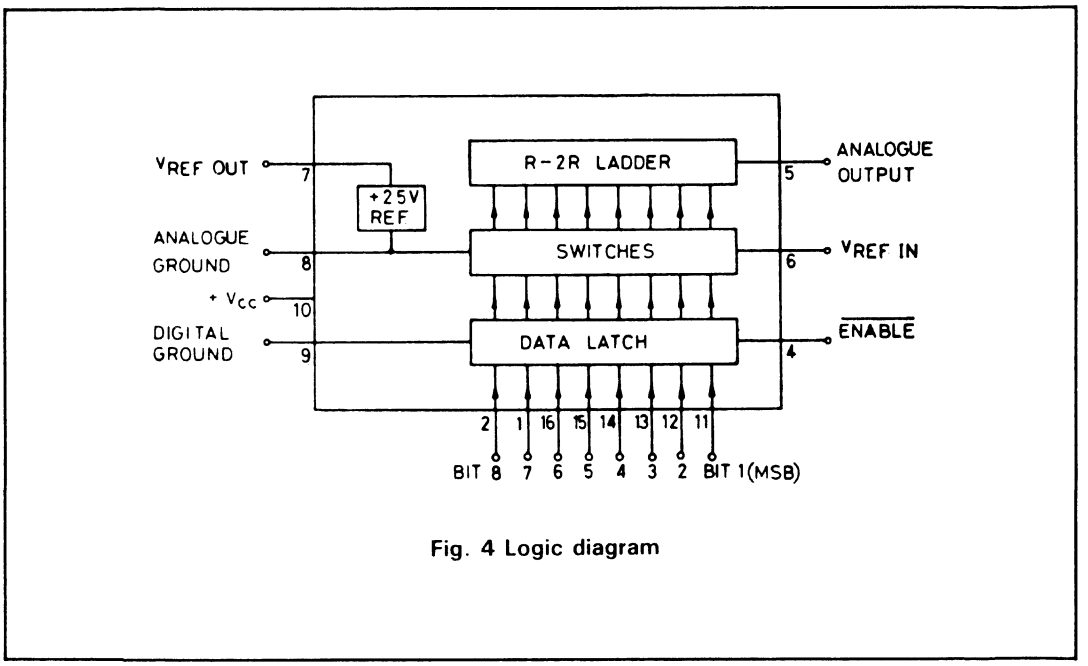


Fig. 4 Logic diagram

The ZN428 is a monolithic 8-bit D-A converter with input latches to facilitate updating from a data bus. The latch is transparent when ENABLE is at logic '0' and the data is held when ENABLE is taken to logic '1'. The ZN428 features single + 5 volt supply requirements, fast 800ns settling time and is guaranteed monotonic over the full operating range. It also contains a 2.5 volt reference the use of which is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted. The converter is of the voltage switching type and uses an R-2R ladder network. Each 2R element is connected to 0 volt or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (1 millivolt). A binary weighted voltage is produced at the output of the R-2R ladder network the nominal output range of the ZN428 being 0V to $V_{REF\ IN}$ through a 4kΩ resistance. Other output ranges can readily be obtained by using an external amplifier.

The 6800 microprocessor system

It is assumed that the reader is fully conversant with the 6800 microprocessor family, information on which can be found in the Motorola M6800 microprocessor applications manual, so only a brief description is given here.

The 6800 is an 8-bit monolithic microprocessor which forms the central control function for the 6800 microprocessor family. Fully compatible with TTL the 6800 requires only a single + 5 volt power supply, it features an instruction set of 72 instructions with 7 addressing modes and full 65k byte memory addressing capability. The microprocessor communications with its external memory and all I/O devices via an 8-bit bi-directional data bus and a 16-bit address bus.

The 6820/21 peripheral interface adaption (PIA) provides a flexible means of interfacing byte-orientated peripherals to the microprocessor, through two 8-bit bi-directional peripheral data lines and four control lines. The functional configuration of the PIA is under the full control of the microprocessor. Each of the peripheral data lines can be programmed to act either as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

The analogue I/O interface

The system described in this application note provides 4 analogue input and 2 analogue output channels - see the system block diagram Fig. 1 and the detailed circuit diagram Fig. 5. Other configurations can easily by produced - these are discussed later in this note.

The peripheral data lines PB0-PB7 of the PIA are connected to the binary data outputs of the ZN427s and the data inputs of the ZN428s to produce a common 8-bit data bus for the converters. Peripheral lines PA0-PA5 are programmed as OUTPUTS and provide individual OUTPUT ENABLE AND ENABLE signals for the ZN427 and ZN427 respectively. A common, simultaneous START CONVERT signal for the ZN427s is produced from the CB2 control line program in the SET/RESET output mode and used in conjunction with a 'D' type flip-flop. The END OF CONVERT outputs from the ZN427s are commoned together and drive the CB1 input of the PIA which can be programmed to generate a microprocessor interrupt signal. In this system configuration, the peripheral lines PA6, PA7 and the control lines CA1, CA2 are not used.

The ZN427 clock signal can be generated either asynchronously from an external source or from the microprocessor clock. If using the MC6871B microprocessor clock device (as supplied with the Motorola MEK6800D2 evaluation kit), which produces a 614.4kHz clock signal, then the ÷2 TTL output of this can be used directly. Note that the maximum lock frequency of the ZN427 is specified as 600kHz, although the device will function up to greater than 1MHz, but at reduced accuracy due mainly to the response time of the comparator. Therefore, if using a microprocessor with a clock frequency greater than 600kHz, then this can either be divided down to less than 600kHz, or it may be used directly up to approximately 1MHz if some loss of accuracy can be tolerated. The advantage of using the microprocessor clock over an external clock is that it allows an accurate calculation of the conversion time to be made in terms of the microprocessor machine cycles eliminating the need to use microprocessor interrupts.

The START CONVERT pulse is generated using a 'D' type flip-flop (½ SN74L74) in order to meet the timing requirements discussed earlier. A conversion cycle is initiated by outputting a logic '0' followed by a logic '1' from the CB2 line of the PIA. This drives the CLEAR input of the 'D' type and sets the START CONVERT (SC) input of each 427 to a logic '0' via the Q output. The first positive going clock edge after the CLEAR input is returned to a logic '1' will clock the 'D' type and set the SC input of each ZN427 at a '1' allowing the conversion cycle to proceed. Note that while the SC input of the ZN427 is at a logic '0' level the MSB output will be driven to a logic '1' and all other data outputs to a logic '0' and the conversion cycle will be held. On the 9th negative clock edge after the START pulse the END OF CONVERSION outputs will go to a logic '1' signifying the end of the conversion cycle. This can be detected by programming the PIA to set the microprocessor interrupt input on the positive going edge of the CB1 control line. The EOC outputs of up to four

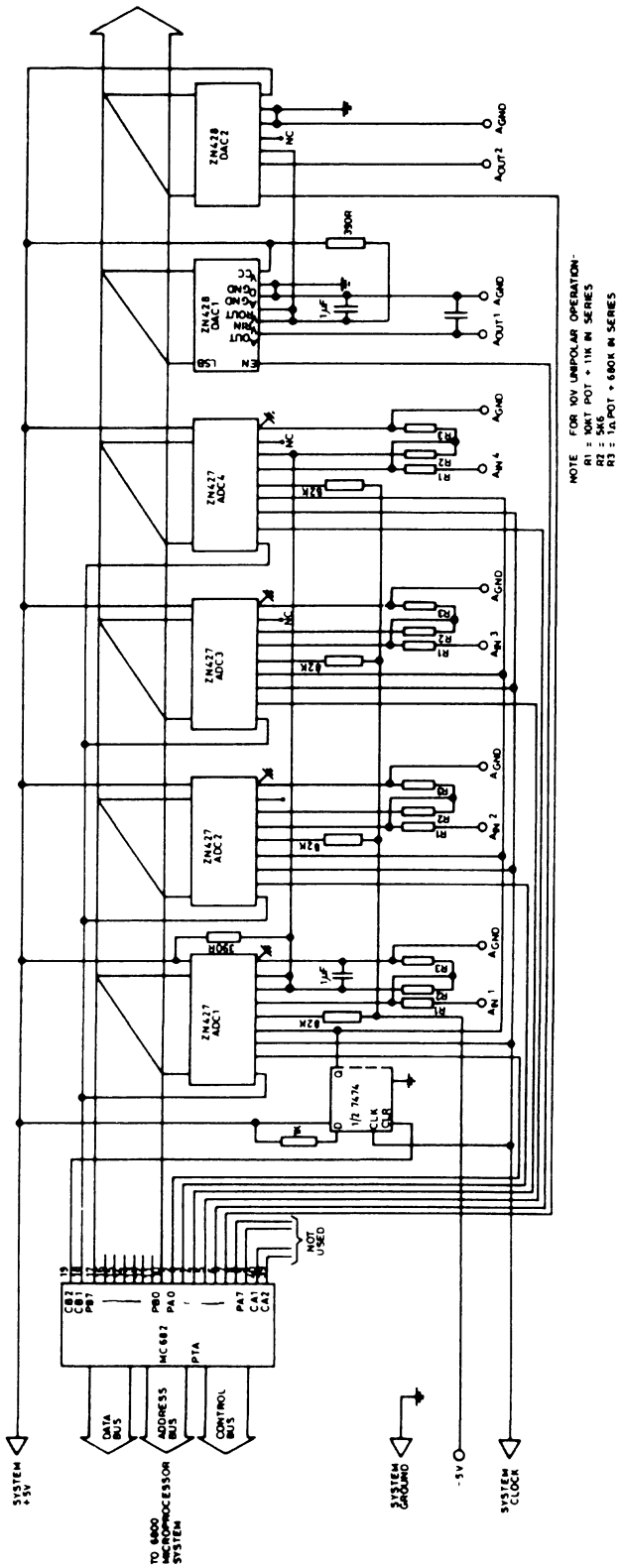

ZN428 DAC2
ZN428 DAC1
ZN427 ADC4
ZN427 ADC3
ZN427 ADC2
ZN427 ADC1
1/2 7474
MC 682
PIA
DATA BUS
ADDRESS BUS
CONTROL BUS
NOT USED
SYSTEM +5V
TO 6800 MICROPROCESSOR SYSTEM
SYSTEM GROUND
-5V
SYSTEM CLOCK
NOTE FOR 10V UNIPOLAR OPERATION:-
R1 = 10KT POT + 11K IN SERIES
R2 = 5K6
R3 = 1Ω POT + 680K IN SERIES

Fig.5

ZN427's can be 'wire-or'd' together to produce a common interrupt line as shown in Fig. 5. Alternatively, if using the microprocessor clock (at up to 1MHz), then the EOC output will always occur within 10 microprocessor machine cycles after the instruction setting the CB2 control line back to a logic '1'. A suitable fixed delay can therefore be built into the program to allow for the conversion time.

The binary output data of each ADC can be read by programming the peripheral lines PB0-PB7 as INPUTS and loading the data onto the converter bus by outputting a logic '1' on the appropriate PA peripheral line in order to enable the 3-state output buffers of the ADC. A microprocessor read instruction on the PIA peripheral register 'B' will then transfer the data to the microprocessor. Obviously the program should be so arranged that, in order to avoid bus connection problems, only one ADC is enabled at any one time.

The circuit diagram Fig. 5 shows the ZN427s connected for a unipolar input range of 0 to +10 volts. Other ranges, e.g. +5V, ±10V and ±5V, can readily be obtained by using a simple resistor network as shown in the ZN427 data sheet.

The negative supply shown for the ZN427 is from −5 volts through an 82kΩ resistor. By suitable choice of resistor value any negative supply between −3 and −30 volts may be used. For applications where only a single +5 volt supply is available, a simple diode pump circuit can be used to generate the negative supply. Further information on the negative supply and a diode pump circuit suitable for up to 5 ZN427s is shown in the data sheet.

Data is output from the system by programming the peripheral data lines PB0-PB7 as OUTPUTS and wiring the binary data from the microprocessor into the PIA peripheral register 'B'. The ENABLE input of the relevant ZN428 is driven to a logic '0' and back to logic '1' via the appropriate PA peripheral line, which will transfer the data from the converter bus to the input data latches of the ZN428. Again the programmer must ensure during an output data transfer that all the ZN427s and the other ZN428 are disabled.

The analogue outputs of the ZN428 are shown, taken directly from pins 5 and 8 which will provide an output range from 0 volts to $V_{REF\ IN}$ through a 4kΩ output resistance. A small capacitor can be connected across the output pins as shown in order to remove any "glitches" which may be present. The value of this capacitor depends on the system noise and the response time required, however for the minimum specified settling time it should not be greater than 100pF. An output buffer amplifier was omitted from the ZN428 design in order to allow optimum settling time, flexibility and lowest cost. Both unipolar and bipolar output ranges can readily be obtained by using an external amplifier, details of which are given in the ZN428 data sheet.

The ZN428 is provided with separate analogue and digital ground pins. These can normally be connected together close to the device and taken to signal ground. However for noisy systems or environments it may be advisable to keep the analogue ground pins for each individual ZN428 separate from the digital ground pin, and to connect each analogue ground to a single common earth point in the system away from sources of digital noise such as clock oscillators, digital buses, etc. The analogue output ground line or terminal should also be taken direct to this common earth point. (Note: The maximum voltage between analogue and digital grounds is limited to 200mV.).

Common reference voltage can be provided by connecting the $V_{REF\ OUT}$ pin of one converter to the $V_{REF\ IN}$ pins of up to five converters (i.e. either ZN427s or ZN428s). This useful feature saves power and gives excellent gain tracking between converters. Fig. 5 shows the four ZN427s driven from one internal reference and the two ZN428s from another.

Note that in this application the dynamic characteristic of the ZN427/428 (i.e. enable/disable delay times, etc.) should not present any problems since they are much less than the microprocessor instruction execution times and need not be considered in the programming.

Program example

A simple program which illustrates the ease of controlling the ZN427/ZN428 with the PIA is shown with the flow diagram, Fig. 6. The object of the program is to read the analogue voltage inputs to ADCs 1 and 2, calculate the mean value and output this on DAC1. A similar operation is performed on the inputs of ADCs 3 and 4 and output on DAC2.

It is assumed that the PIA has been reset which has the effect of zeroing all the PIA registers. This sets all the peripheral and control lines as INPUTS and disables the interrupts. Initially the index register is loaded with the PIA base address in order that the indexed addressing mode can be used throughout the program to address the PIA. The peripheral lines PA0-PA7 are programmed as OUTPUTS and the control registers set so that control line CB2 operates in the SET/RESET output mode and the interrupt flag bit CRB-7 is set with a positive going edge on control line CB1. All the converters are disabled by outputting 30H and the PIA lines which sets the OUTPUT ENABLE inputs of the ZN427s to a logic '0' and the $\overline{\text{ENABLE}}$ inputs of the ZN428s to a logic '1'. A dummy read is made of the B data register to clear the interrupt flag bit CRB-7.

A START signal is then generated via control line CB2 by toggling bit CRB-3 in control register B. The end of the conversion cycle is detected by testing the interrupt flag bit CRB-7 and looping at this point in the program until it goes to a '1'. (Note: The microprocessor interrupt request lines IRQA, IRQB are disabled.) The output of ADC1 is now read by driving peripheral line PA0 to a logic '1', and the data is stored in the microprocessor accumulator B, ADC2 is read in a similar way by setting PA1 line to a logic '1' and storing the data in accumulator A. The mean value of the readings is found by adding the accumulators and rotating the result right, one bit through carry, this is equivalent to dividing by 2. The result is saved in the memory location labelled 'TEMP 1'. The process is repeated on ADC3 and ADC4, enabling the ADC outputs by setting lines PA2 and PA3 in turn to a logic '1', and storing the computed result in location 'TEMP 2'.

The data direction register B is now accessed and the peripheral line PB0-PB7 changed to OUTPUTS. The data stored in 'TEMP 1' is outputted onto the converter bus and DAC1 enabled by toggling line PA4 in a logic 1-0-1 sequence, which will transfer the binary data from the bus to the DAC input latches and hence to the analogue output. A similar sequence is performed on DAC2 with the data from 'TEMP 2', using PA5 line to drive the $\overline{\text{ENABLE}}$ input. The program is terminated with a software interrupt SWI, returning to the monitor program.

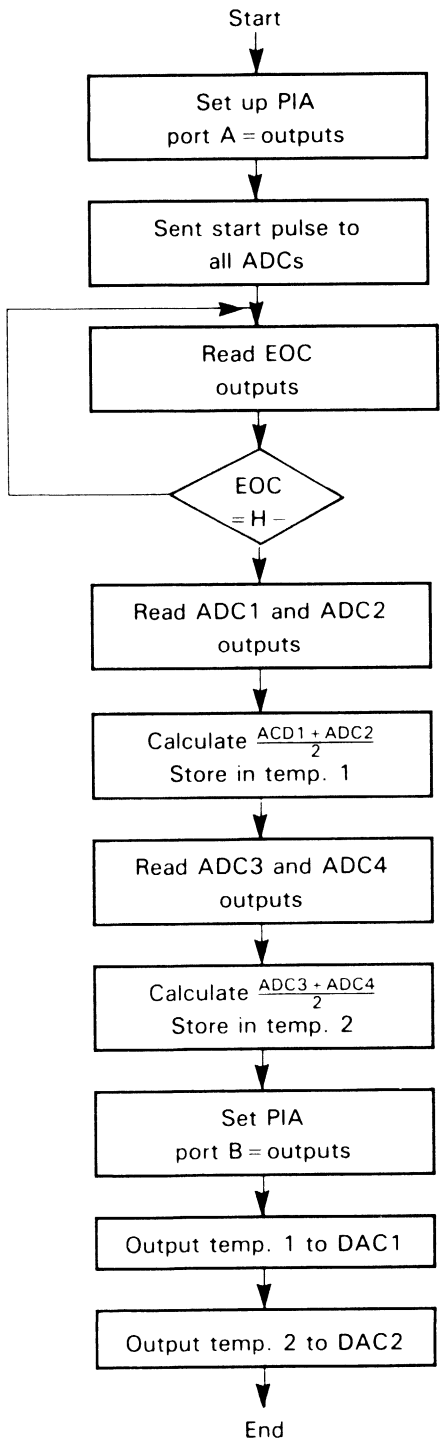


Fig. 6 Program flow diagram

PIA PORT ALLOCATIONS

PORT A

PA0	ADC1 OE input
PA1	ADC2 OE input
PA2	ADC3 OE input
PA3	ADC4 OE input
PA4	DAC1 $\overline{EN}$ input
PA5	DAC2 $\overline{EN}$ input
PA6	NOT USED
PA7	NOT USED

PORT B

PB0	BINARY DATA LSB
PB1	BINARY DATA LSB + 1
PB2	BINARY DATA LSB + 2
PB3	BINARY DATA LSB + 3
PB4	BINARY DATA LSB + 4
PB5	BINARY DATA LSB + 5
PB6	BINARY DATA LSB + 6
PB7	BINARY DATA MSB

CONTROL

CA1	NOT USED
CA2	NOT USED
CB1	COMMON EOC OUTPUT
CB2	COMMON START LINE

PIA ADDRESSES

8004	PERIPHERAL/DATA DIRECTION REG. A
8005	CONTROL REG. A
8006	PERIPHERAL/DATA DIRECTION REG. B
8007	CONTROL REG. B

Location	Object		Comment	Source statement
000	CE004		LDX 8004	Load PIA address to IX
3	86FF		LDA A FF	
5	A700		STA A 0, X	Set port A as outputs.
7	863E		LDA A 3E	
9	A701		STA A 1, X	Set control reg. A
B	A703		STA A 3, X	Set control reg. B
D	8630		LDA A 30	
F	A700		STA A 0, X	Disable converters
11	A602		LDA A 2, X	Dummy read to clear flag
13	8636		LDA A 36	
15	A703		STA A 3, X	Set CB2 low to
17	863E		LDA A 3E	generate start pulse
19	A703		STA A 3, X	Set CB2 high
1B	A603	TEST	LDA A 3, X	Read control reg. B
1D	8580		BIT A 80	Test for CRB-7 high
1F	27FA		BEQ TEST	ie End of conversion
21	8631		LDA A 31	
23	A700		STA A 0, X	Enable ADC1 O/Ps
25	E602		LDA B 2, X	Read ADC1 O/P
27	8632		LDA A 32	
29	A700		STA A 0, X	Enable ADC2 O/Ps
2B	A602		LDA A 2, X	Read ADC2 O/P
2D	1B		ABS	Add ADC1 + ADC2 readings
2E	46		RORA	Divide by 2
2F	976E		STA A Temp.1	Save in temp.1
31	8634		LDA A 34	
33	A700		STA A 0, X	Enable ADC3 O/Ps
35	E602		LDA B 2, X	Read ADC3 O/P
37	8638		LDA A 38	
39	A700		STA A 0, X	Enable ADC4 O/Ps
3B	A602		LDA A 2, X	Read ADC4 O/P
3D	1B		ABA	Add ADC1 + ADC2 readings
3E	46		RORA	Divide by 2
3F	976F		STA A Temp.2	Save y in temp.2
41	8630		LDA A 30	
43	A700		STA A 0, X	Disable ADC O/Ps
45	863A		LDA A 3A	
47	A703		STA A 3, X	
49	86FF		LDA A FF	
4B	A702		STA A 2, X	Set port B as output
4D	863E		LDA A 3E	
4F	A703		STA A 3, X	
51	966E		LDA A temp.1	
53	A703		STA A 2, X	Put x Data on bus
55	8620		LDA A 20	
57	A700		STA A 0, X	Enable DAC1 I/Ps
59	C630		LDA B 30	
5B	E700		STA B 0, X	Disable DAC1 I/Ps
5D	966F		LDA A temp.2	
5F	A702		STA A 2, X	Put y data on bus
61	8610		LDA A 10	
63	A700		STA A 0, X	Enable DAC2 I/Ps
65	E700		STA B 0, X	Disable DAC2 I/Ps
67	3F		SWI	End
006E	00		Temp.1	x data
006F	00		Temp.2	y data

Summary

The system described in this report is by no means restricted to the configuration shown. Provided that the drive capability of the system components is not exceeded, the number and configuration of ZN427s and ZN428s which can be employed is limited only by the I/O lines available from the PIA, hence providing the design engineer with a wide degree of freedom in producing the system that best fulfils his requirements.

The major loading and drive characteristics of the various system components are shown in Table 1. Buffer gates can be employed where necessary to expand the drive capability of the components such as when utilising a long bus with high capacitive loading. Note that the peripheral lines from side B are used for the converter bus since these present a high impedance when programmed as inputs. Also the 6821 PIA is preferred to the 6820 because this has a 2-TTL drive capability on both A and B side peripheral lines. As stated previously up to 4 ZN427 EOC outputs can be 'wire-or'd' together; if using more than 4, then each group can be ANDed together using a SN7409 TTL gate to produce a single interrupt line.

If required separate START signals can be generated for each ZN427 hence allowing a microprocessor read of one ADC to be in progress while the other(s) are in a conversion cycle. However this configuration does require one peripheral line and one 'D' type flip-flop per START signal line. Since only one ZN427 or ZN428 should be enabled at any one time, then it is possible to incorporate one or more decoder types of I.C. such as the SN74154, 4 line to 16 line demultiplexer/ decoder in order to expand the system. This device could be connected with the 4 data inputs connected to 4 PA peripheral lines and the decoder enable input driven by CA2 line. Use of two such I.C's would provide 32 output lines allowing an analogue I/O system with a combination of up to 32 analogue input and output channels to be produced.

As a result of the low converter cost, low external component count and flexibility of this type of system, designs based on using one converter per analogue channel will be both a practical and economical solution to microprocessor data acquisition problems. This approach should find many new applications in areas which have previously been limited by the necessity of having to use the traditional data acquisition methods involving a single, high cost hybrid A-D converter utilising a sample/hold and multichannel multiplexing techniques.

TABLE 1

MC6820	PA0 - PA7/CA2	PB0 - PB7/CB2	CA1/CB1
I_{IL}	-1.6mA max.	10μA max.	2.5μA max. (at V_{IN} = 0 to 5.25V)
I_{IH}	-100μA min.		
I_{OL}	1.6mA min	1.6mA min	
I_{OH}	-100μA min	-100μA min.	
MC6821			
I_{IL}	-2.4mA max	10μA max	2.5μA max. (at V_{IN} = 0.5... 5.25V)
I_{IH}	-200μA min		
I_{OL}	3.2mA min	3.2mA min	
I_{OH}	-200μA min	-200μA min	
ZN427			
I_{IL}	-5μA max		
I_{IH}	15μA max		
$I_{IH\ (Clock)}$	30μA max		
I_{OL}	1.6mA min		
I_{OH}	-100μA min		
I_{OHX} (Off state leakage)	2μA max		
ZN428	All inputs		
I_{IL}	-5μA max		
I_{IH}	20μA max		

NOTE Currents specified at 0.4 and 2.4V unless otherwise stated.

Interfacing the ZN427 A-D Converter with the 8085A

The growth of microprocessors has led to a demand for low cost, fast 8-bit A-D and D-A converters to interface between the real world of analogue values and the digital world of the microprocessor. Converter systems have, until recently, been mainly high cost, multiplexed, sample and hold systems usually built around a 12-bit A-D converter. The system described in this report is a low cost, expandable, one converter per channel system, based on the ZN427 8-bit A-D converter interfaced directly to the I/O Ports of the 8155 2K bit static 'RAM', which forms part of the basic 8085A microprocessor system.

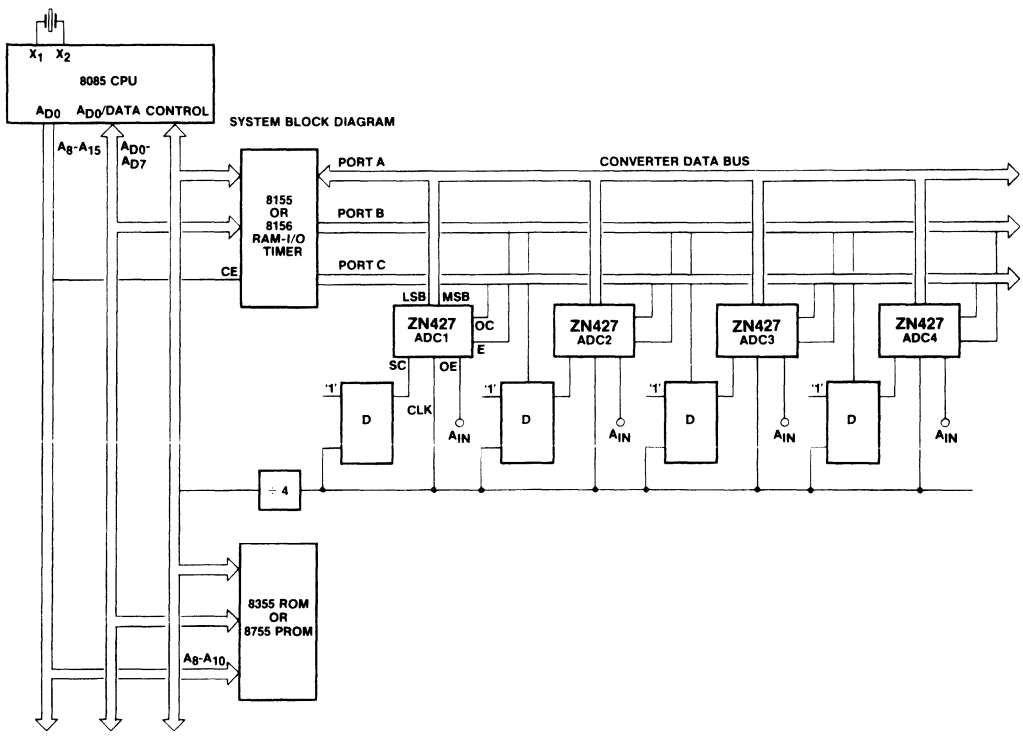


Fig. 1 System block diagram

The ZN427 A-D converter

The ZN427 is a monolithic 8-bit, successive approximation A-D converter designed for microprocessor compatibility. It features fast 15μs conversion time, three-state outputs to permit bussing on common data lines and no missing codes over the full operating temperature range. The ZN427 contains a voltage switching D-A converter, a 2.5V precision band gap reference, a fast comparator, successive approximation logic, and three-state output buffers.

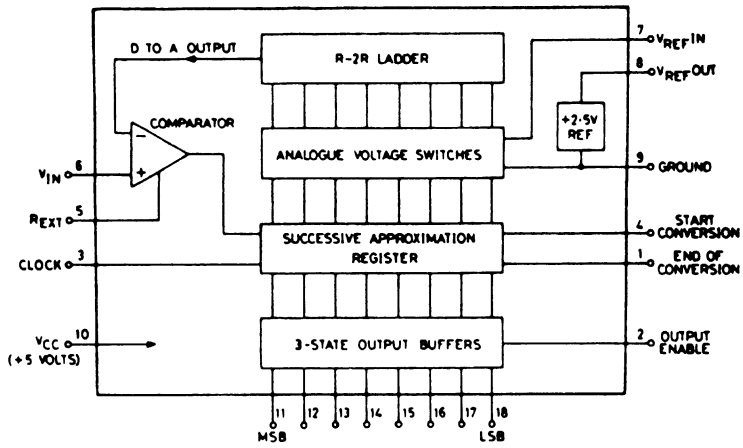


Fig. 2 ZN427 logic diagram

Operation of the ZN427 is best described with reference to the timing diagram - Fig. 3. Conversion is initiated by a start convert (SC) pulse which can be applied asynchronously with respect to the ZN427 clock providing the following criteria are met.

1. The leading edge of the SC-pulse should precede the first active (negative going) edge of the clock (after trailing edge of the SC pulse) by at least 1.5μs to allow for MSB setting.

2. The trailing edge of the SC pulse must not occur within $\pm$ 200ns of a negative going edge of the clock.

3. As a special case of conditions (1) and (2) the SC pulse may be coincident with, and of the same duration as, a negative going clock pulse. Application of the SC pulse sets MSB to a '1' level and all other bits to a '0', which produces a voltage output from the D to A converter of $V_{REFIN/2}$. This value is compared with the input voltage V_{IN}, and a decision is made on the first negative clock edge to set the MSB to '0' if $V_{REFIN/2} > V_{IN}$, or else to keep it at '1'. Bit 2 is switched to a '1' on the same clock edge, and on the next edge a decision is made about bit 2, again by comparing the D/A output with V_{IN}. This process is repeated for all eight bits so that when the END OF CONVERSION (EOC) output goes high the digital output from the converter is valid representation of V_{IN}. The binary output is latched until the next START pulse. The three-state data outputs are OFF (high impedance) when OUTPUT ENABLE (OE) is a '0' and are enabled when the OE input is taken to a '1'.

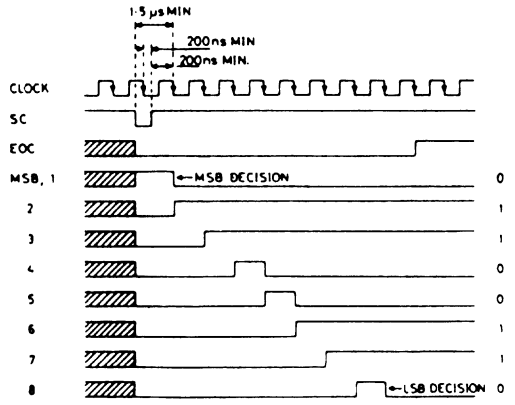


Fig. 3 Timing diagram

The 8085A microprocessor system

It is assumed that the reader is totally familiar with the 8085A microprocessor system, information on which can be obtained from the MCS-85 users manual, so only a brief description is given here.

The 8085A is a complete 8-bit parallel central processing unit. A minimum component 8085 microcomputer system can be built from just three chips - the 8085A CPU, a 8355 or 8755 ROM or PROM, and a 8155 or 8156 RAM/TIMER/I-O chip. The 8155/8156 provides, in addition to 2k bits of Static RAM, two programmable 8-bit I/O Ports, one programmable 6-bit I/O Port and a programmable 14-bit binary timer counter. (The difference between the 8155 and the 8156 is that on the 8155 the CHIP ENABLE is active LOW, and on the 8156 it is active HIGH).

The ZN427 interface

This application note describes how up to 4, ZN427 ADCs can be connected to the I/O ports of one 8155 RAM to provide 4 analogue input channels to the microprocessor system. Since most 8055 based systems include the SDK-85 system design kit will incorporate one or more 8155s, then the addition of analogue input channels would involve minimum additional hardware and design effort. An advantage of using the 8155 I/O ports is that no additional address decoding or bus demultiplexing and buffering hardware is necessary.

For existing systems, if spare I/O ports are available then analogue inputs can easily be added without any major modifications to the hardware. Also the expansion of the number of input channels to a system by addition of extra 8155s should be easily implemented since this device is directly bus compatible with the 8085A.

The 8155 I/O ports are allocated as shown in the logic diagram, Fig. 1. Port A is programmed as INPUTS and provides an 8-bit data bus which connects to the three-state binary data outputs of each ZN427. port B is programmed as OUTPUTS, the lower 4-bits provide the start convert and the upper 4-bits provide the output enable signals to each ZN427. The END OF CONVERT output of each ZN427 is connected to a port C pin, which are programmed as INPUTS to provide the individual BUSY FLAGS for each ZN427. Note that only 4- of the 6-bits available from port C are used.

The ZN427 clock can be supplied either from an external source or from the 8085A CLOCK OUTPUT. Since the 8085A clock will normally be at 3MHz, it will be necessary to divide this down by at least a factor of 4. This is achieved in the circuit, see Fig. 6, by means of a dual JK flip-flop (7473) connected as a 2-bit binary counter. (Note: This will provide a clock frequency of 750kHz which is a little higher than the ZN427 clock frequency spec. minimum of 600kHz. However, for most practical applications the loss in accuracy due to this will be minimal.) An external clock could be used for the ZN427 but the advantage of using the microprocessor clock is that it allows an accurate calculation of the ZN427 conversion time to be made in terms of the microprocessor CLOCK CYCLES (or 'T' states).

(Note: To avoid confusion, future reference to clock will mean the ZN427 clock signal unless specifically stated otherwise.)

The START CONVERT pulse is generated using a 'D' type flip-flop (½ 7474) in order to meet the timing requirements discussed earlier. A conversion cycle is started by outputting a '0' followed by a '1' from the appropriate port B output to the CLEAR input of the 'D' type which sets the SC input of the ZN427 to '0'. The first positive going clock edge after the CLEAR input is returned to a '1' clocks the 'D' type and sets the SC input to '1'. This sequence is illustrated in the start pulse timing diagram, Fig. 4.

On the 9th negative clock edge after the start pulse the END OF CONVERT output goes to a '1' signifying the end of the conversion process, this can be detected by an I/O read on port C. However, when generating the ZN427 clock from the microprocessor clock as shown, the EOC output will always occur within 35 microprocessor clock cycles after the OUT instruction returning the SC to a '1'. In this case it is not necessary to poll the EOC outputs, the ZN427 data outputs can be read after a suitable fixed delay in the program. For application where process time is at a premium or if immediate response is required to an EOC output, a microprocessor interrupt can be generated by connecting the EOC output direct to one of the 8085A restart inputs. The EOC outputs of two 4-ZN427s can be 'wire-OR'd' to produce a common interrupt line. Usually, however, the fast conversion time of the ZN427 (15μs) will make it not worth-while to employ microprocessor interrupts since the conversion time takes less than 6/7 typical microprocessor instructions.

The binary output data is applied via the converter data bus to port A of the 8155 by driving the OE output to a '1' from the appropriate port B bit. Obviously the program should be arranged so that the outputs of only one ZN427 are enabled at any one time, in order to avoid bus contention problems. Note that in this application the output enable and disable switching times (which are specified at 250ns

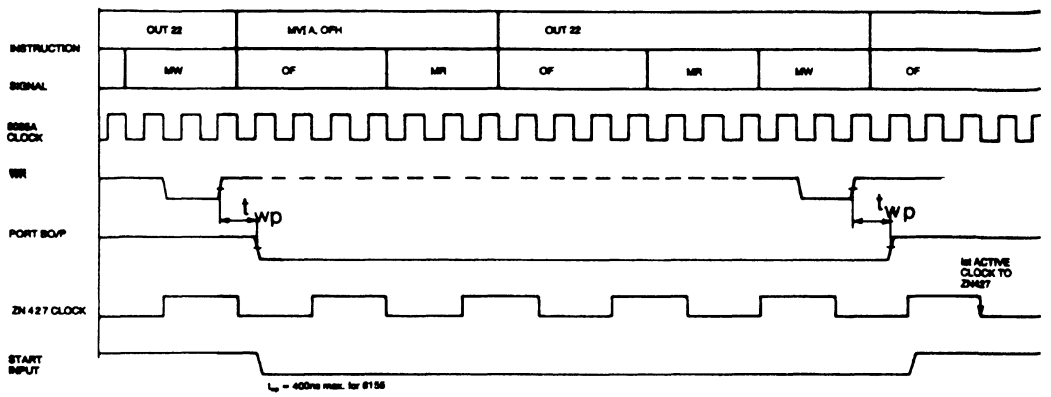


Fig.4 Start pulse timing diagram

max.), need not be considered since they are much less than the instruction execution times.

The circuit diagram, Fig. 6 shows the ZN427s connected for a unipolar input range of 0 to +10V. Other ranges, e.g. +5V, ±10V, and ±5V can be readily obtained by using the appropriate resistors as shown in the ZN427 data sheet. Note also that the reference, $V_{REF\ IN}$, of up to five ZN427s may be driven from one internal reference. This useful feature saves power, discrete components, and gives excellent gain tracking between the converters.

In the circuit the negative supply to the ZN427s is through an 82k resistor from −5V. By suitable choice of resistor any negative supply of −3 to −30 volts may be used. For applications where only a positive 5 volt supply is available, a simple diode pump circuit suitable for up to 5-ZN427s is shown in the ZN427 data sheet.

Program example

A simple program is given together with the flow diagram in Fig. 5, which illustrates the ease of controlling and reading the ZN427 with the 8155 I/O ports.

Following the flow diagram it is seen that after initialisation of the stack pointer the I/O ports of the 8155 are defined - ports A and C as INPUTS, port B as OUTPUTS. A simultaneous START CONVERT pulse is sent to all the ADCs by outputting logic '0' followed by logic '1' to the lower 4-bits of port B. The EOC outputs of the ADCs are then read via port C and tested for a logic '1' to check if the conversion process has finished. The microprocessor will loop on this part of the program until the EOC output of all the ADCs go to '1'. When this occurs the program proceeds by enabling the outputs of each ADC in turn and reading the binary data via port A. The ADC outputs are enabled in turn by outputting a logic '1' to each of the upper 4-bits of port B (keeping the other 3-bits at '0' and the lower 4-bits at a '1'). The data from each ADC is stored in consecutive memory locations, starting at the address labelled 'DATA'. The H and L register pair hold the memory address at which data is to be saved; these are incremented for each read of the ADC.

This program could easily be modified to act as a sub-routine for another main program. As mentioned previously a fixed delay could be substituted for the program loop which tests the EOC outputs. Also instead of generating a simultaneous START pulse separate START signals may be sent to each ADC at different times in a control cycle.

Summary

The system described in this report should be suitable for most applications since it allows complete control of each individual ADC. However, the configuration can easily by changed for particular requirements, - a few ideas are briefly described below.

1. If a simultaneous START pulse is adequate, then the START CONVERT inputs of the ZN427s can be commoned together and driven via one 'D' type from one port output.

2. The EOC outputs of up to 4-ZN427s can be commoned and either taken to one port input or used as a microprocessor interrupt signal.

3. Adoption of methods 1 and/or 2 above would use 8155 Port bits and hence allow more ZN427s to be connected to each 8155.

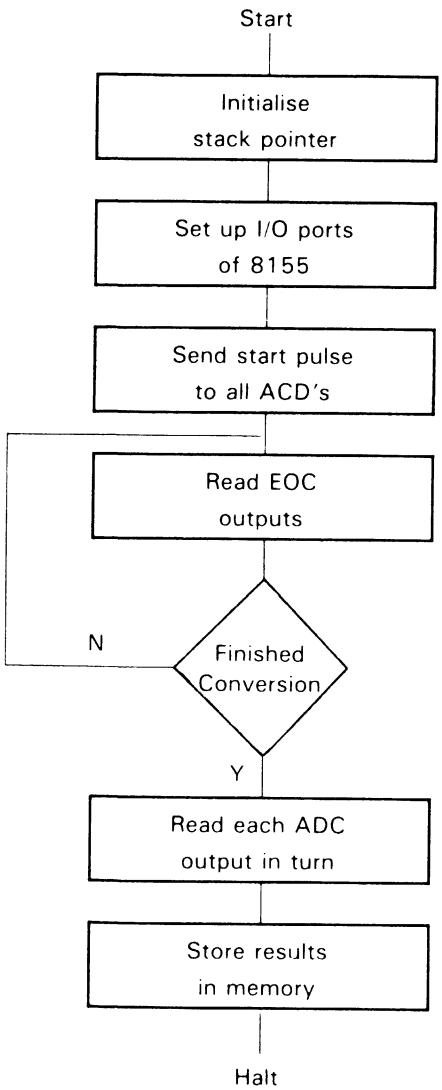
4. Instead of generating the START pulse from the 8155 it could be asynchronously produced externally by a process timer, photo transistor or proximity detector circuit etc., the only timing requirement being that the pulse width fed to the CLEAR input of the 'D' type is at least half a clock period. (i.e. 640ns with a 320ns microprocessor clock) or 1.5μs, whichever is smaller.

5. If D-A channels as well as A-D are required in one system then ZN428, 8-bit D-A converters can be mixed on the same converter data bus as the ZN427. This will allow a designer to tailor a system to his specific A-D and D-A requirements.

It is hoped that after reading this application note, the reader will have a much better insight into the operation and versatility of the ZN427, and into how it can easily be interfaced to a microprocessor system.

In order to avoid duplication only the relevant ZN427 characteristics were discussed in this report. For a full description and specification of the ZN427 please refer to the data sheet.

Fig.5 Program flow diagram



8155 PORT ALLOCATIONS

PORT A

PA0	BINARY DATA LSB
PA1	BINARY DATA LSB + 1
PA6	BINARY DATA MSB - 1
PA7	BINARY DATA MSB

PORT B

PB0	ADC1 SC INPUT
PB1	ADC2 SC INPUT
PB2	ADC3 SC INPUT
PB3	ADC4 SC INPUT
PB4	ADC1 OE INPUT
PB5	ADC2 OE INPUT
PB6	ADC3 OE INPUT
PB7	ADC4 OE INPUT

PORT C

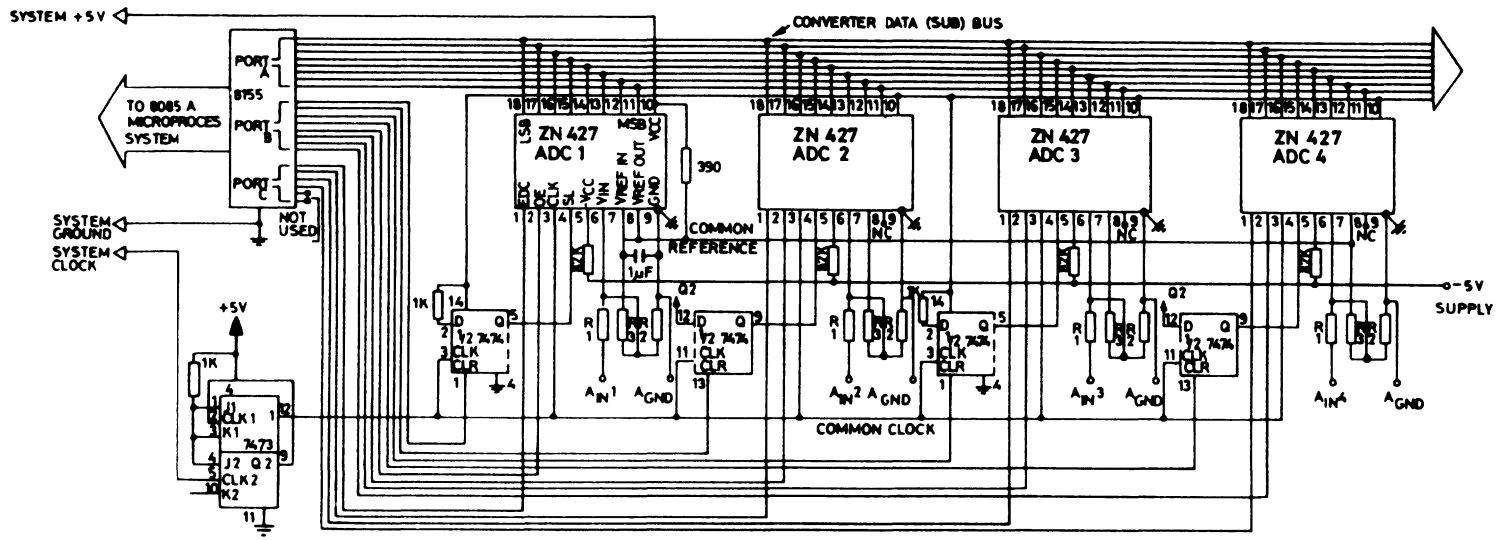
PC0	ADC1 EOC OUTPUT
PC1	ADC2 EOC OUTPUT
PC2	ADC3 EOC OUTPUT
PC3	ADC4 EOC OUTPUT

I/P PORT ADDRESSES

20	COMMAND/STATUS REG
21	RAM PORT A
22	RAM PORT B
23	RAM PORT C

ZN427 - 8085A PROGRAM EXAMPLE

Location	Object		Source statement	Comment
2000	31C820		LXI SP, 20C8	Initialise stack pointer
2003	3E02		MVI A, 02H	Define I/O ports
2005	D320		OUT 20	
2007	3E00		MVI A, 00H	
2009	D322		OUT 22	Send start to ALL ADC's
200B	3EOF		MVI A, OFH	
200D	D322		OUT 22	
200F	060F		MVI B OFH	
2011	DB23	LOOP:	IN 23	Read EOC s
2013	AO		ANA B	Strip upper 4 bits
2014	B8		CMP B	Test if ALL EOC s
2015	C21720		JNZ LOOP	are A '1'
2018	213B20		LXI H, DATA	
201B	3EIF		MVI A, 1FH	
201D	D322		OUT 22	Enable ADC 1
201F	DB21		IN21	Read ADC 1
2021	77		MOV M, A	Save in Loc., DATA
2022	23		INX H	Increment pointer
2023	3E2F		MVI A 2FH	
2025	D322		OUT 22	
2027	DB21		IN21	Read ADC 2
2029	77		MOV M, A	Save in Loc. DATA + 1
202A	23		INX H	
202B	3E4F		MVI A 4FH	
202D	D322		OUT 22	
202F	DB21		IN 21	Read ADC 3
2031	77		MOV M,A	Save in Loc. DATA + 2
2032	23		INX H	
2033	3E8F		MVI A 8 FH	
2035	D322		OUT 22	
2037	DB 21		IN 21	Read ADC 4
2039	77		MOV M, A	Save in Loc. DATA + 4
203A	76		HLT	
203B		DATA:		
203C				
203D				
203E				



NOTE: FOR 10V UNIPOLAR OPERATION
R1 = 10K POT + 11K IN SERIES
R2 = 5,K6
R3 = 1M POT + 680K IN SERIES

Fig.6

Interfacing the ZN428 D-A Converter with the 8085A

This report describes a simple, low cost, expandable multichannel D-A system based on the ZN428, 8-bit D-A converter interfaced directly to the I/O ports of the 8155, 2K bit static RAM, which forms part of the basic 8085 microprocessor system.

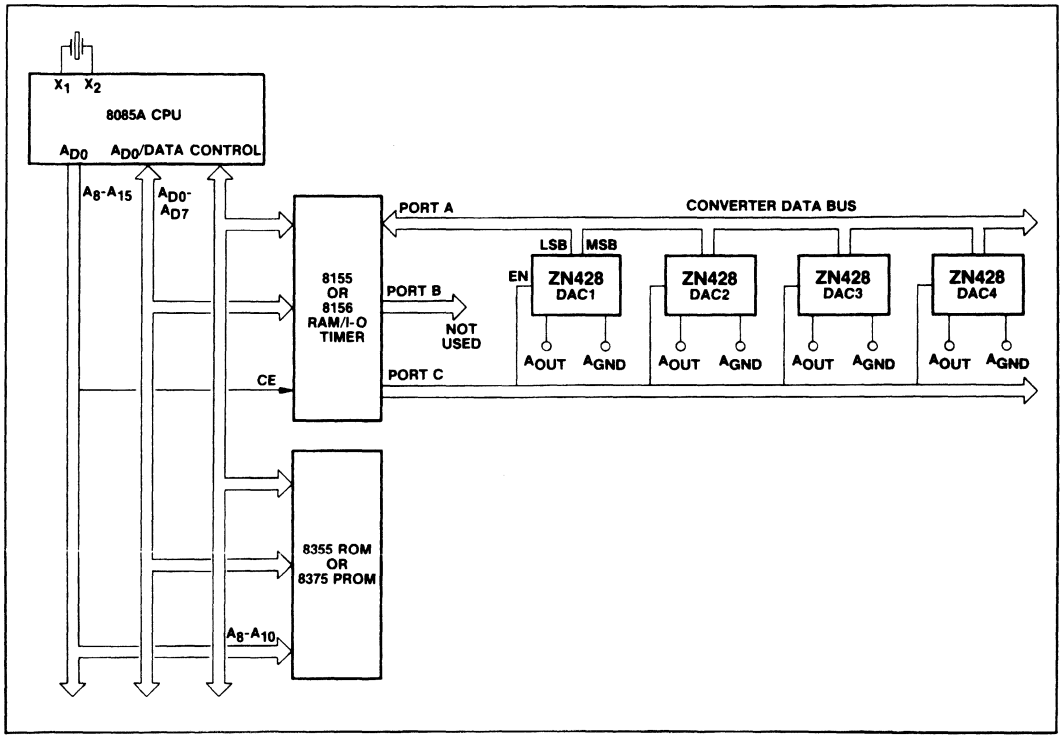


Fig. 1 System block diagram

The ZN428 D-A converter

The ZN428 is a monolithic 8-bit D-A converter with input latches to facilitate updating from a data bus. The latch is transparent when ENABLE is at logic '0' and the data is held when ENABLE is taken to logic '1'. The ZN428 features single + 5 volt supply requirements, fast 800ns setting time and is guaranteed monotonic over the full operating range. It also contains a 2.5 volt reference the use of which is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.

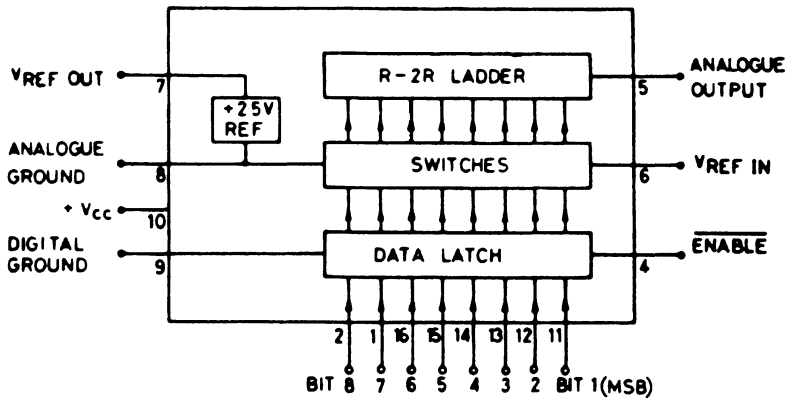


Fig. 2 ZN428 logic diagram

The converter is of the voltage switching type and used R-2R ladder network. Each 2R element is connected to the 0 volt or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (1 millivolt). A binary weighted voltage is produced at the output of the R-2R ladder network the nominal output range of the ZN428 being 0 volt to $V_{REF\ IN}$ through a 4kΩ resistance. Other output ranges can readily be obtained by using an external amplifier.

The 8085A microprocessor system

It is assumed that the reader is totally familiar with the 8085A microprocessor system, information on which can be obtained from the MCS-85 users manual, so only a brief description is given here.

The 8085A is a complete 8-bit parallel central processing unit. A minimum component 8085A microcomputer system can be built from just three I.C.s-the 8085A CPU, an 8355 or 8755 ROM or PROM, and a 8155 or 8156 RAM/TIMER/I-O I.C. The 8155/8156 in addition to 2K Bits of Static RAM, provides two programmable 8-bit I/O ports, one programmable 6-bit I/O port and a programmable 14-bit binary timer counter. (The difference between the 8155 and the 8156 is that on the 8155 the CHIP ENABLE is active LOW, and on the 8156 it is active HIGH.)

The ZN428 interface

This application note describes how one or more ZN428 DACs can be connected directly to the I/O ports of an 8155 RAM to provide analogue output channels from the microprocessor system.

Since most 8085 based systems, including the SDK-85 system design kit, will incorporate one or more 8155s then the addition of analogue output channels can be made with the minimum of extra hardware and design effort. An advantage of using the 8155 I/O ports is that no additional address decoding or bus multiplexing and buffering hardware is necessary. For existing systems, if spare I/O ports are available then analogue outputs can easily be added without major modifications to the hardware. Also expanding the number of output channels by means of addition of extra 8155s should be easy to implement, since the 8155 is directly bus compatible with the 8085A. Fig. 3 shows 4-ZN428s connected to the I/O ports of one 8155. Port A is programmed as OUTPUTS and provides a common 8-bit data bus which is connected to the binary data inputs of each ZN428. The $\overline{\text{ENABLE}}$ inputs of each of the ZN428s are connected to separate pins on port C which is also programmed as OUTPUTS. Note that in this configuration only 4 of the 6 port C pins are used and port B is also unused.

The reference voltage of all converters, is provided by connecting the $V_{REF\ OUT}$ pin of one ZN428 to the $V_{REF\ IN}$ pins of all the ZN428s as shown. This useful feature saves power, components and gives excellent gain tracking between converters. Up to five ZN428s may be driven from one internal reference in this way.

The circuit, Fig. 3, shows the outputs of the ZN428s taken directly from pins 5 and 8. This will provide an output range of 0V to $V_{REF\,IN}$ through a 4kΩ output resistance. A small capacitor can be connected across the output pins as shown in order to remove any 'glitches' which may be present. The value of this capacitor depends on the noise in the system and the response time required, however, for the minimum settling time it should not be greater than 100pF. The output buffer amplifier was omitted from the ZN428 in order to allow greater system speed, flexibility and lowest cost. Both unipolar and bipolar output ranges can readily be obtained by using an external amplifier, details of which are given in the ZN428 data sheet.

The ZN428 is provided with separate analogue and digital ground pins. These can be connected together close to the I.C. pins. However, for noisy systems or environments it may be better to keep the analogue ground pins for each individual ZN428 separate from the digital ground, and to connect each analogue ground to a single common earth point in the system, away from sources of digital noise such as clock oscillators, digital buses etc. The analogue ground output line or terminals should also be taken direct to this common earth point. (Note: The maximum voltage between analogue and digital grounds is limited to 200mV.)

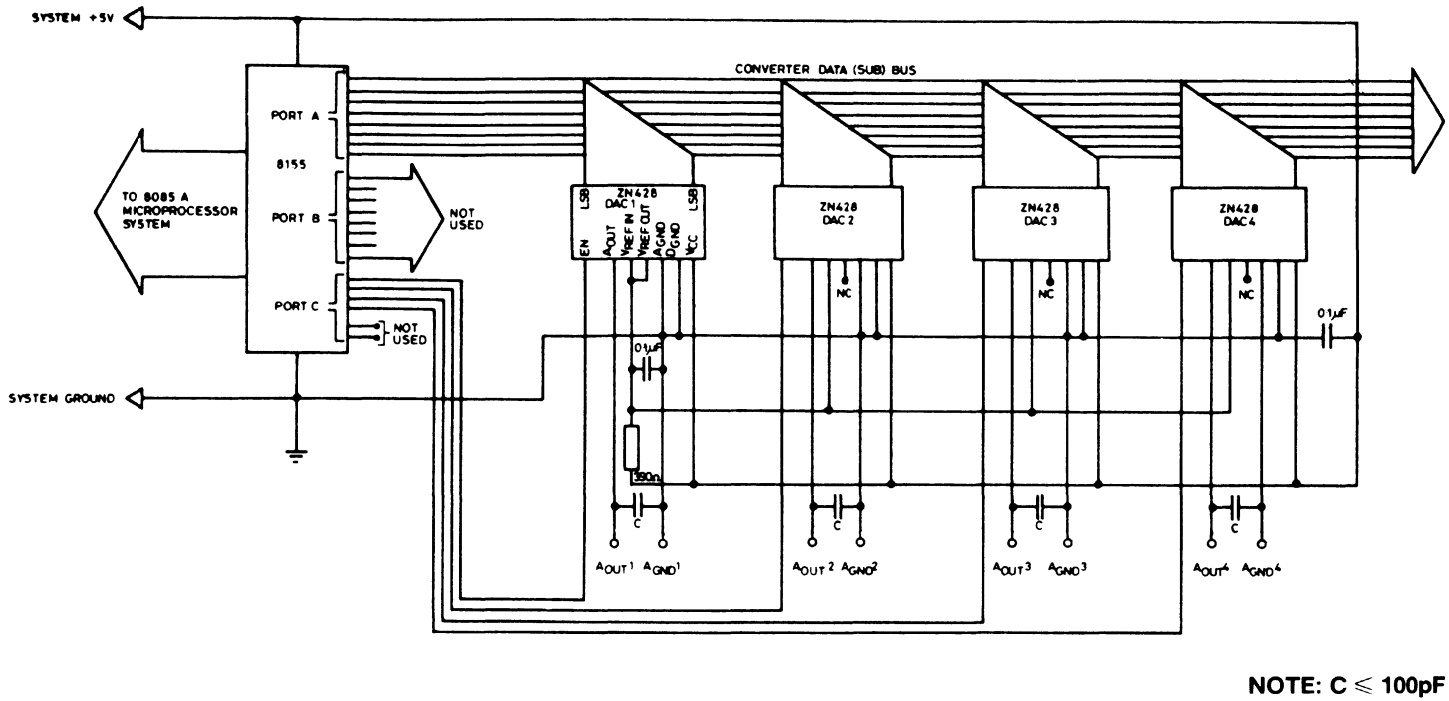
Data is fed to a converter simply by outputting the binary data onto the common bus from port A of the 8155. The appropriate output from port C is then driven to a logic '0' level then back to a logic '1'. This will transfer the binary data on the bus into the input latches of the ZN428. The $\overline{\text{ENABLE}}$ inputs of converters which are not being updated are held at logic '1'. The data from port A can now be changed and the next converter updated as and when required as determined by the controlling program of the microprocessor. Note that in this application the data set-up and data hold times and enable pulse widths need not be considered since they are much less than the microprocessor instruction execution times.

Program example

A simple program is given together with the flow diagram in Fig. 4, which illustrates the ease of controlling the ZN428 in conjunction with the 8155 I/O ports.

The object of the program is to read the binary data from four successive memory locations and to output this data sequentially to each of the four DACs. In practice this program would probably act as a sub-routine outputting data derived from some external source and operated on by the main program.

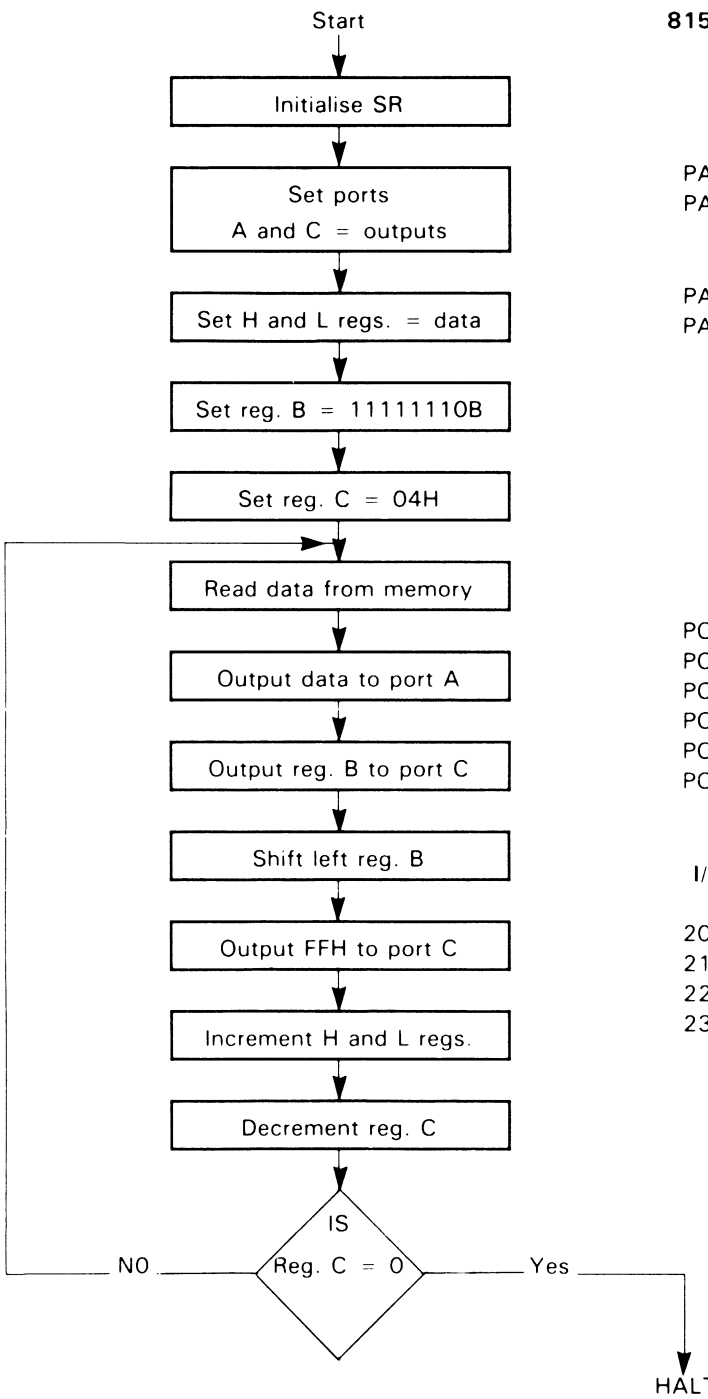
With reference to the flow diagram Fig. 4 it is seen that after initialisation of the stack pointer the I/O ports A and C are defined as OUTPUTS. The H and L register pair are loaded with the starting address in memory of where the data to be outputted is stored. Register B determines which ADC is to be enabled, this is set initially to 11 111 110; while register C, which acts as a loop counter is set to 4. Data is then read from memory into the accumulator using the H and L registers in the register indirect addressing mode. This data is outputted onto the converter data bus via port A by sending the contents of the accumulator directly to the 8155 with the 'OUT' instruction. DAC 1 is now enabled by transferring the contents of register B to the accumulator and outputting this via port C. The accumulator contents are rotated one bit left before being transferred back to register B, ready to enable the next DAC. Next $\overline{\text{ENABLE}}$ is removed by outputting all 1's via port C, H and L are incremented to address the next data byte and register C is decremented and tested for zero. In this case register C will contain 03 and the program will branch back to the address labelled 'LOOP' via a conditional jump instruction, and the data byte will be read into the accumulator. Since register B was shifted one bit left the new data will be loaded into DAC 2 on this cycle of the loop. The program cycles round the loop 4 times, reading the data from memory and outputting it to each DAC in turn until register C is decremented to zero, at which point the program halts.



NOTE: C ⩽ 100pF

Fig.3

Fig. 4 Program flow diagram



8155 PORT ALLOCATIONS

PORT A

PA0	BINARY DATA LSB
PA1	BINARY DATA LSB + 1
PA6	BINARY DATA MSB – 1
PA7	BINARY DATA MSB

PORT B

NOT USED

PORT C

PC0	DAC1 $\overline{\text{ENABLE}}$ INPUT
PC1	DAC2 $\overline{\text{ENABLE}}$ INPUT
PC2	DAC3 $\overline{\text{ENABLE}}$ INPUT
PC3	DAC4 $\overline{\text{ENABLE}}$ INPUT
PC4	NOT USED
PC5	NOT USED

I/O PORT ADDRESSES

20	COMMAND/STATUS REG
21	RAM PORT A
22	RAM PORT B
23	RAM PORT C

ZN428 - 8085A PROGRAM EXAMPLE

Location	Object		Source statement	Comment
2000	31C8204		LXI SP. 20C8	Initialise SP
2003	3E0D		MVIA, 0D	Define I/O ports
2005	D320		OUT 20	
2007	212020		LXI H, DATA	Set H & L = data
200 A	06FE		MVI B, FEH	
200 C	0E0 4		MVI C, 04H	
200 E	7E	LOOP:	MOV A,M	Read data
200 F	D321		OUT 21	Put Data on bus
2011	78		MOV A,B	
2012	D323		OUT 23	Set $\overline{\text{Enable}}$ low
2014	07		RLC	Rotate left for next DAC
2015	47		MOV B,A	
2016	3EFF		MVI A, FF	Set $\overline{\text{Enable}}$ high
2018	D323		OUT 23	
201A	23		INX H	
201B	0D		DCR C	
201C	C2 0E 20		JNZ Loop	Jump IF C = 0
201F	76		HLT	
2020	–		DATA:	
2021				
2022				
2023				

Summary

The system described in this report should be satisfactory for most applications, however, this configuration is by no means rigid, but is only intended as one example to demonstrate how easily the ZN428 can be used with the 8085A microprocessor system. A few ideas and notes are briefly described below, and it is hoped that these will help the design engineer to produce the most efficient system for his particular requirements.

1. The 8155 I/O ports can be allocated as dictated by system requirements and availability. In the example all of port A and four of the six port C I/O pins are used. Port B could have been used equally as well either for the converter data bus or to provide the $\overline{\text{ENABLE}}$ signals.

2. If I/O port pins are limited and only one DAC needs to be enabled at any one time, then a decoder I.C. (i.e. 8205, 1 out of 8 binary decoder) can be used to drive the $\overline{\text{ENABLE}}$ inputs. For example 4 I/O port pins, 3 for the address code and 1 for the decoder enable would drive 8 DAC ENABLE inputs.

3. In order to update 2 DACs simultaneously but with different data, then the binary inputs of one (or more) DACs could be connected to port A and the other DAC to port B. The relevant data could then be output on Ports A and B and then the ENABLE inputs of both DACs driven to logic '0' together, either by commoning the two inputs to one port C or by using separate I/O pins from port C but programming both bits to go low together.

4. The number of ZN428s which can be connected to a common data bus is limited only by the bus capacitance and the drive capability of the 8155 I/O Ports. Note the low inputs currents of the ZN428 –
$I_{IH} = 20\mu A$ at 2.4V, $I_{IL} = -5\mu A$ at 400mV.

5. When the ZN428 $\overline{\text{ENABLE}}$ input is held at logic '0' the input latches are held open and the data is transferred directly to the ladder switches. Therefore, if repeatedly updating only one DAC the $\overline{\text{ENABLE}}$ input can be held at logic '0' instead of returning to logic '1' after each update.

6. If A-D channels as well as D-A are required in one system, then ZN427, 8-bit A-D converters can be mixed on the same converter data bus as the ZN428. This will allow the design engineer to tailor a system to his specific A-D and D-A requirements.

It is hoped that after reading this application note the reader will have a much better insight into the operation and versatility of the ZN428, and into how it can easily be interfaced to a microprocessor system. In order to avoid duplication only the relevant characteristics of the ZN428 were discussed in this report. For a full description and specification of the ZN428 please refer to the data sheet.

Direct Bus Interfacing using the ZN427/ZN428 Data Converters

This application note introduces two converters and describes how they can easily be interfaced directly to most of the popular types of microprocessor with particular reference to the 6800 and 8085A.

The ZN427 A-D converter

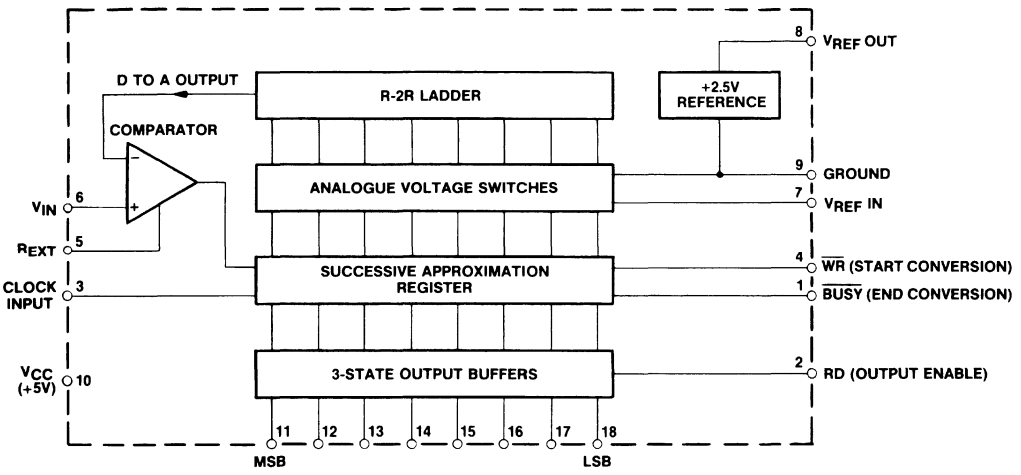


Fig. 1 ZN427 logic diagram

The ZN427 is an 8-bit, successive approximation A-D converter (ADC).

It features three-state output buffers to permit bussing on to common data lines, fast 15μs conversion time and no missing codes over its full operating temperature range. The ZN427 contains a voltage switching D-A converter, a fast comparator, successive approximation logic, three-state output buffers and a 2.5 volt precision bandgap reference.

The use of the on-chip reference is pin optional to retain flexibility, an external fixed or varying reference for ratiometric operation may, therefore, be substituted. Only a few passive external components are required. For basic operation these are an input resistor, a reference current resistor and stabilising capacitor, and a resistor from the R_{EXT} pin 5 to the negative supply rail.

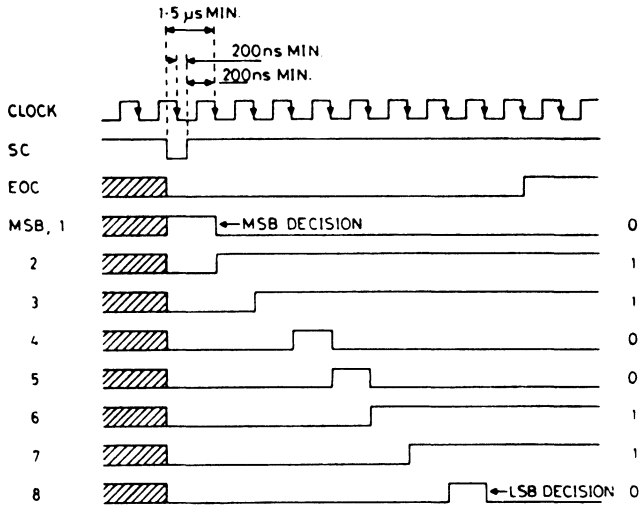


Fig. 2 ZN427 timing diagram

The conversion cycle is initiated by a negative going pulse applied to the START CONVERSION (SC) input, this sets the END OF CONVERSION (EOC) output to a logic '0' indicating that the converter is busy, see Fig. 2. On the ninth negative going clock edge after the start pulse the EOC output goes back to logic '1' signalling that the cycle is complete. The binary output data is latched until the next start pulse. The three-state data outputs are switched OFF (high impedance state) when the OUTPUT ENABLE (OE) input is at a logic '0', and they are enabled when the OE input is taken to a logic '1'.

The ZN427 D-A converter

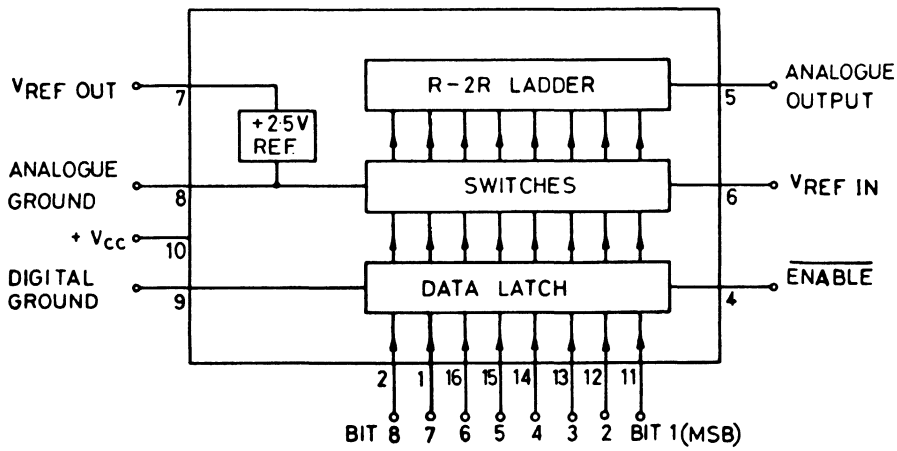


Fig. 3 ZN428 logic diagram

The ZN428 is a monolithic 8-bit D-A converter (DAC), with input latches to facilitate updating from a microprocessor data bus. The latch is transparent when the ENABLE (EN) input is at a logic '0' and the data is held when EN is taken to a logic '1'.

The ZN428 features single +5V supply requirements, fast 800ns settling time and is guaranteed monotonic over its full temperature range. It contains a pin optional 2.5V precision bandgap reference identical to the ZN427. The converter is of the voltage switching type and uses an R-2R ladder network. Each 2R element is connected to 0 volt or $V_{REF\ IN}$ by transistor logic switches especially designed for low offset voltage (< 1 millivolt). A binary weighted voltage is produced at the output of the R-2R ladder network, the nominal range being 0 - $V_{REF\ IN}$ volts with a 4kΩ resistance. Other output ranges can readily be obtained by the use of an external amplifier allowing complete versatility in its application.

The ZN427 microprocessor bus interface

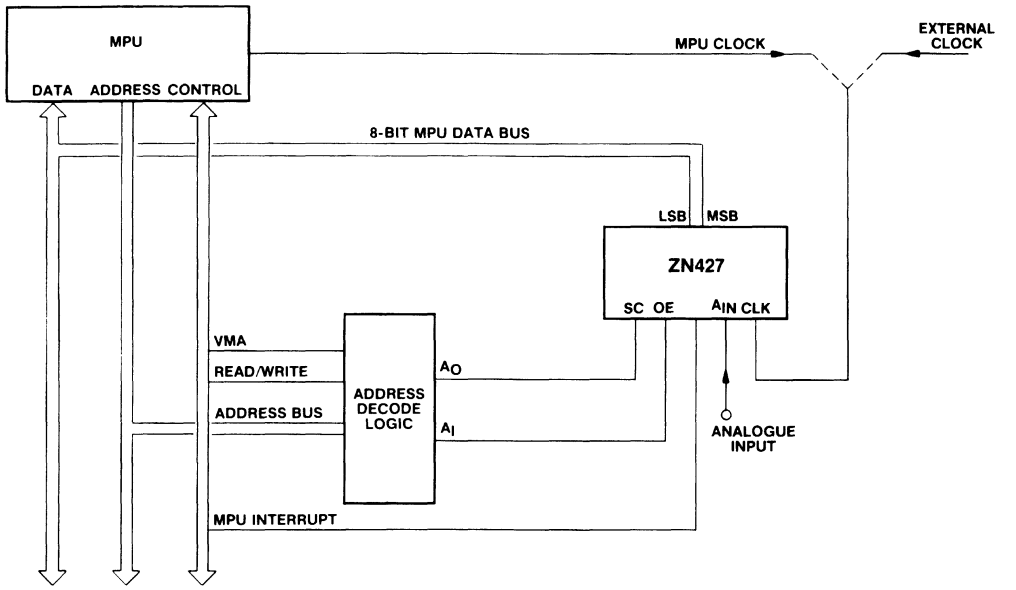


Fig. 4

Peripheral devices can be connected to a microprocessor system by two basic methods. The first and usually the simplest from the point of view of design effort required is to use a peripheral interface I/O device usually found as a support IC in most of the MPU families. With this method the peripheral device is simply connected to the I/O lines of the peripheral interface device and generally no considerations have to be made in terms of bus buffering, bus timing or address decoding.

The second method is to connect the peripheral device directly to the microprocessor data bus. This method is termed "memory mapped I/O" which as its name implies is to make each peripheral I/O function appear to the MPU as a normal memory location, in which case the MPU cannot tell whether it is addressing memory or I/O. This allows the full set of memory reference instructions to be used for I/O data transfer, but it does imply that the peripheral device must be capable of responding at least as fast as the MPU memory and hence it should be compatible with the bus timing characteristics. The disadvantages of memory mapped I/O are that it usually requires additional address decoding logic, and also, since the I/O device will be addressed as memory, then there will consequently be fewer addresses available for actual memory.

It is with this second method of interfacing that this application note is primarily concerned.

A variation of memory mapped I/O, sometimes known as "I/O mapped I/O" is available on some MPUs which overcomes the last disadvantage referred to. This allows a defined range of memory address also to be used for I/O by means of separate I/O instructions. A special control line is required to inform the memory and I/O device whether the address of the current READ or WRITE cycle refers to memory or to I/O. This technique however does restrict the freedom of the programmer to the use of these I/O instructions which normally only operate on data in the microprocessor accumulator.

Fig. 4 shows the basic memory mapped interface for the ZN427 where the 8 binary outputs of the ADC are connected directly to the MPU data bus. The control inputs, START CONVERSION and OUTPUT ENABLE are shown driven from address decoder logic, the function of which is to drive the appropriate input when the address which has been allocated to that particular input is present on the address bus and the control bus signals indicate a valid memory read or write operation. Note that the level of address decode logic used must ensure that the three-state data outputs of the ZN427 are disabled at all times except when the actual ADC data is required on the data bus, otherwise bus contention problems may occur with other devices using the bus. The END OF CONVERSION outut can be connected directly to an MPU interrupt to signal the completion of the conversion cycle by the ADC. The ZN427 clock can be driven either from the MPU clock or from an external source. If however the former method is employed, it may simplify the design of the interface with regard to the timing criteria of SC input. (This is covered in more detail later.)

The ZN428 microprocessor bus interface

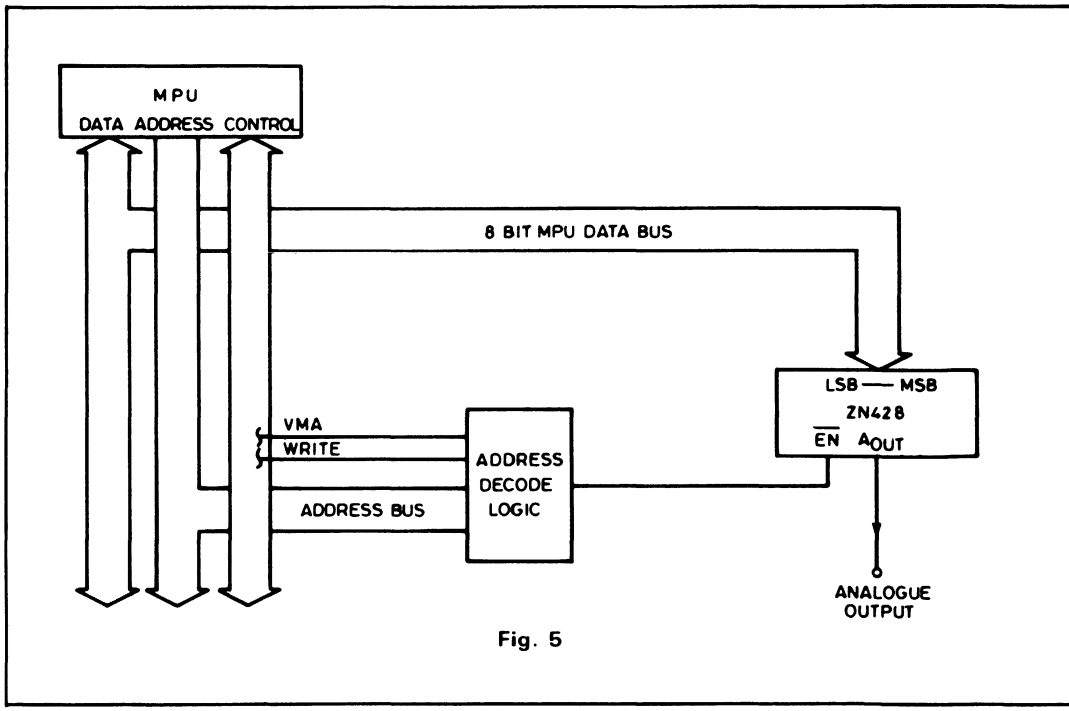


Fig. 5

The ZN428 data inputs can be directly connected to an MPU data bus when in the memory mapped configuration, this is illustrated in Fig. 5. For this application the address decode logic has only to generate the $\overline{\text{ENABLE}}$ signal for the DAC. This is accomplished by gating the MPU WRITE signal with the decoded address signal in order that when a memory write instruction to the DAC address location is executed, then a negative going pulse is applied to the EN input which will transfer the binary code from the data bus to the ZN428 input latches.

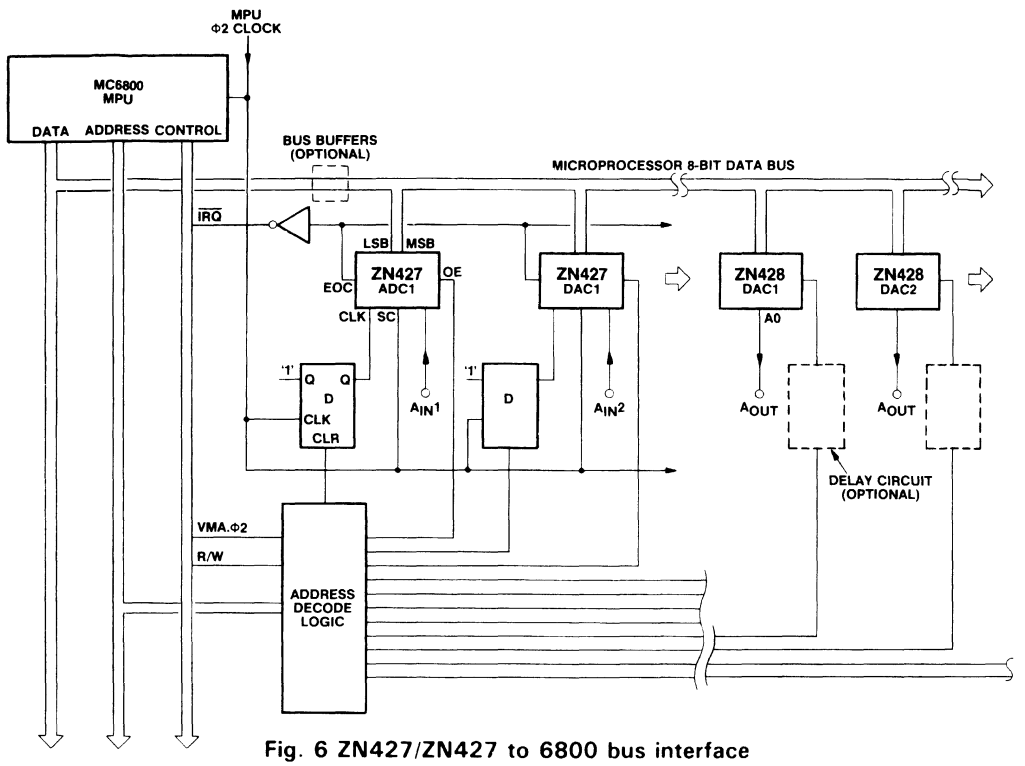


Fig. 6 ZN427/ZN427 to 6800 bus interface

With the ability of the ZN427 and ZN428 to be bus compatible it is possible to produce a complete analogue I/O system, specifically configured to the designer's own requirements with the converters connected directly to the MPU data bus. Such a system is illustrated in Fig. 6 build around a 6800 MPU.

The 6800 is an 8-bit monolithic microprocessor which forms the central control function for the 6800 microprocessor family. Fully compatible with TTL logic the 6800 requires only a single +5 volt power supply, it features a set of 72 instructions with 7 addressing modes and full 65K byte memory addressing capability. The microprocessor communicates with its external memory and all I/O peripherals over an 8-bit bi-directional data bus and a 16-bit address bus. (Full data on the 6800 microprocessor is readily available from its manufacturers and their distributors).

The number of ZN427s and ZN428s which can be hung on the data bus is not limited, the only restrictions being the total load presented to the data bus and the number of decoded address lines available. The loading and drive characteristics of the converters are summerised in Table I. Optional bi-directional bus buffers are shown in the diagram, these can be used to expand the system. Use of these will be dependent on the total number of converters used, other peripheral and memory devices on the data bus, and other loading factors such as physical length of bus required.

ZN427		ZN428	
Parameter	Specification	Parameter	Specification
I_{IL}	$-5\mu A$ max.	I_{IL}	$-5\mu A$ max.
I_{IH}	$15\mu A$ max.	I_{IH}	$20\mu A$ max.
I_{IH} (Clock)	$30\mu A$ max.		
I_{OL}	1.6mA min.		
I_{OH}	$-100\mu A$ min.		
I_{OHX} (Off state leakage)	$2\mu A$ max.		

(NOTE: Currents specified at 0.4V and 2.4V).

Table 1 Loading characteristics of the ZN427 and ZN428

The level of address decoding will depend on the overall MPU system design. This can range from merely using the upper address lines directly with no hardware decoding to provide the control lines for the converters - which rapidly depletes the number of address locations available for memory, through to full address decoding where all 65K addresses can be utilised. The address decode hardware can usually be produced from a few TTL gates in association with an address decoder I/C such as the 74154. In order to avoid addressing problems it is necessary on the 6800 to qualify the decoded address with the valid memory Address (VMA) and $\phi 2$ clock signals. The READ/WRITE control line can also be utilised to permit a single decoded address to control each ZN427, i.e. WRITE instruction to the specific address would generate the SC signal and a READ instruction of the same address would enable the converter outputs and read the data. The function of the 'D' type flip-flops shown in the diagram is to ensure that the timing criteria of the SC pulse are met. The requirements for this are that the SC pulse should start at least $1.5\mu s$ before the first active (negative going) clock edge after the SC pulse, and that the trailing edge of the SC pulse must not occur within $\pm$ 200ns of a negative going clock edge, see Fig. 2. By careful design of the address decode logic when deriving the converter clock from the MPU it is possible to produce the correct timing for the SC pulse and to dispense with the 'D' type flip-flops.

The other advantages of using the MPU clock is that it allows an accurate calculation of the ZN427 conversion time to be made in terms of the MPU machine cycles. Again with reference to Fig. 2 it can be seen that the conversion cycle always takes less than 10 clock cycles after the end of the SC pulse. Hence instead of using the EOC output to drive MPU $\overline{IRQ}$ input a simple programme delay loop can be substituted. Note that the EOC outputs of up to five ZN427s can be 'wire-anded' together to form a common interrupt line.

The clock frequency of the standard 6800 is 1MHz which can be used directly to drive the ZN427's if a small loss of accuracy can be tolerated. The 6871B MPU clock generator is produced in a version with a 614.4kHz clock signal. This is only marginally higher than the specified ZN427 clock rate of 600 kHz and the $\phi 2$ TTL output of this can be used directly for the converter clock if full accuracy is essential.

With the 6800 it may be necessary to delay the decoded address enable signal to the ZN428 converters if glitch free operation is desired. This is due to the fact that during a write operation on the 6800 the address and address qualifying control signals become valid before the data bus signals are valid, thereby enabling the DAC before the data is established on the data bus.

The analogue output can be taken directly from the ZN428 output pin which provides a nominal output range from zero volts to $V_{REF\ IN}$ with a 4kΩ output resistance. For most applications higher output ranges or drive will be required. This can easily be accomplished on the ZN428 by the addition of an external buffer amplifier which can be chosen for the specific characteristics required. The ZN428 is provided with separate analogue and digital ground pins which should normally be connected together close to the I.C. For noisy systems or environments an improvement may be obtained, in some cases, by running the two ground pins to supply ground separately, taking the analogue ground of each ZN428 to a single common earth point in the system away from the sources of high noise such as clock oscillators, digital buses, etc. Note that the maximum voltage between the analogue and digital ground pins should not be allowed to exceed 200mA.

Both the ZN427 and ZN428 contain a nominal 2.5V internal bandgap voltage reference. Use of this on-chip reference is pin optional to retain flexibility and an external reference can be substituted which allows ratiometric operation over the range of typically 1.5 to 3V. The on-chip reference is capable of supplying the reference voltage for up to five ZN427s and ZN428s. This useful feature saves power, discrete components and gives excellent gain tracking between the converters in a system. The tail current for the comparator on the ZN427 is derived via an external resistor from a negative supply. By suitable choice any negative supply of between −3 and −30 volts may be used. Since the negative current is only of the order of 65 microamps per converter then for applications where only a positive supply is available a simple diode pump circuit can be used.

With a memory mapped interface the full range of memory reference instructions are available to the programmer in order to control the converters, and programming becomes a relatively simple matter of reading and writing data to the addresses allocated to the converters. For example, for the ADCs a conversion cycle could be initiated by a store accumulator command (STA A) to address location ALOC 1, where ALOC 1 is the address of the ADC to be accessed. The contents of the MPU accumulator 'A' at this time are irrelevant since we only want to generate a memory write cycle to produce a pulse at the SC input. Now one can either enable the MPU interrupt and wait for the EOC output to generate an interrupt signal if this is the method used or alternatively a simple programme delay loop can be entered to produce a delay of $\geqslant 9$ converter clock cycles (i.e $\geqslant 15\mu s$ if a 600kHz clock is used). Upon receipt of an interrupt or completion of the delay a load accumulator command (LDA A) can be performed on address ALOC 1. This will read the binary data from the converter into the MPU accumulator 'A'. It is even simpler to programme the DACs. All one needs to do is to load the value to be outputted to say accumulator 'A' in binary format. A store accumulator command (STA A) is then programmed to address location ALOC 2, where ALOC 2 is the address allocated to the DAC. Upon execution of this the data will be transferred from the accumulator via the data bus to the DAC input latches and be present at the DAC output in analogue form within 1.25 microseconds of the enable pulse.

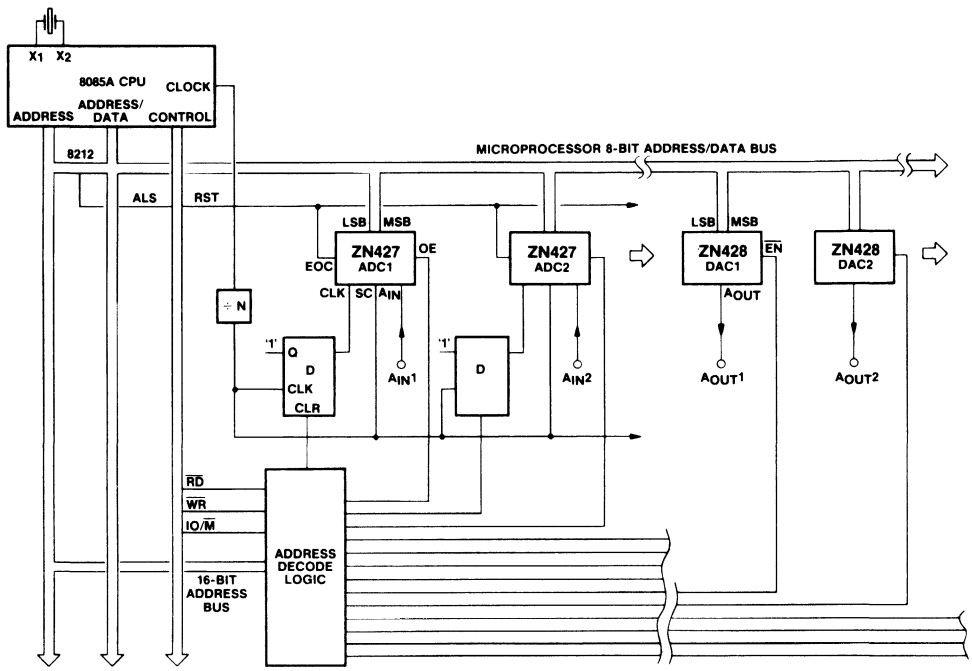


Fig. 7 ZN427/ZN428 to 8085 bus interface

An analogue I/O system for the 8085A microprocessor is shown in Fig. 7. This is similar to the 6800 system but the following exceptions should be noted.

The 8085A is another popular 8-bit microprocessor. However, unlike the 6800 this MPU uses a multiplexed data bus whereby the lower 8 address bits A0-A7 are time shared with the 8 data bits. The address bus contains the upper 8 bits A8-A15. If the lower 8 address bits are to be used for address decoding then it is preferable to de-multiplex the bus using an 8 bit latch, such as the 8212, strobed with the address latch enable (ALE) signal from the MPU. The 8085A offers either memory mapped I/O or I/O mapped I/O by means of a separate control line (IO/$\overline{M}$). This allows use of the 'IN' and 'OUT' instructions to control I/O data transfers and the retention of the full 65K memory locations. If using this method then it is unnecessary to de-multiplex the address/data bus, since only the lower 256 addresses are used for I/O transfers, and the address in the lower 8 bits is mirrored into the upper 8 address bits during this operation.

The standard 8085 clock frequency is 3MHz. Hence it is necessary to divide the output from the 8085A CLK output pin down by a factor of at least 4 to produce an acceptable ZN427 clock. Because of this it is more difficult to synchronise the decoded address signals with the ZN427 clock in order to meet the start pulse timing criteria, and one will usually have to incorporate the 'D' type flip-flops as indicated to generate the SC pulse.

Note that with the 8085A the common EOC line can be used directly to generate an interrupt via one of the 3 restart interrupt inputs. The decoded address input to the ZN428s $\overline{EN}$ input can also be used without any additional delay since, with this MPU the bus data is valid during the time that the WRITE signal is established.

Again programming is very straightforward. With a memory mapped I/O configuration the data transfer commands - move (MOV), load (LDA) and store (STA) can be used to control data transfers between the converters and the MPU. If an I/O mapped I/O configuration is adapted then the input (IN) and output (OUT) commands are used to transfer data between MPU accumulator and the converters.

Summary
The analogue I/O systems described in this report are intended only as a guide to illustrate to design engineers the ease and versatility with which these two converters can be used to produce analogue I/O channels for popular 8-bit microprocessors. As a result of the low cost, low external component count and flexibility of these converters, designs based on the 'one converter per channel concept' will be both a practical and economical solution to microprocessor data acquisition problems. This approach should find many new applications in areas which have previously been limited by the necessary usage of traditional data acquisition methods involving a single high cost hybrid ADC utilising sample and hold and multichannel multiplexing techniques.

A Serial Interface for the ZN427 A-D Converter

In many data acquisition applications it is advantageous to situate the A-D converter close to the transducer and to transmit the digital data in serial form back to the data collection centre of the system. The serial data link uses less conductors and provides better noise immunity than a parallel data bus. This application note describes a RS-232C compatible serial data interface for the ZN427 8-bit A-D converter using an industry standard 6402 UART. A simplified block diagram is shown in Fig. 1.

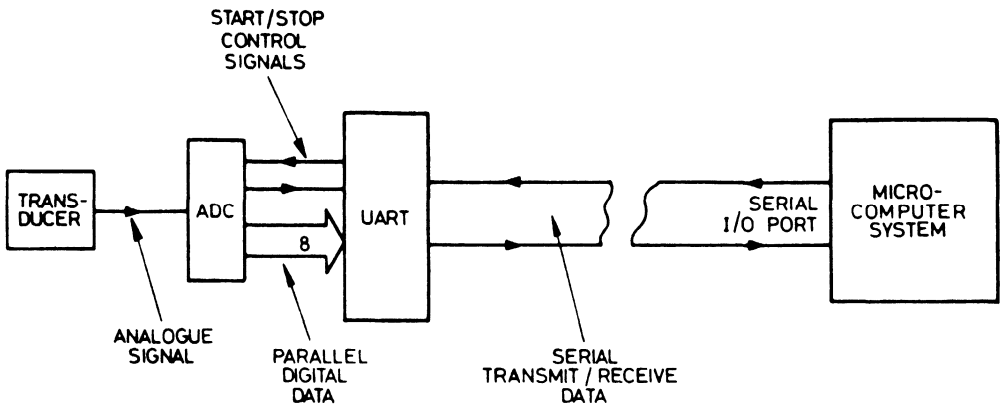


Fig. 1 Serial data interface

In order to initiate a conversion cycle a character is transmitted by the microcomputer. Upon receipt of this character by the UART its DR (data received) output goes to a high level which generates a start pulse for the A-D converter triggering a conversion cycle. At the end of the cycle the EOC (end of convert) output is used to load the converted data into the UART which performs a parallel to serial conversion and transmits the data back to the microcomputer.

The ZN427 is an 8-bit successive approximation A-D converter. It features three-state output buffers to permit bussing onto common data lines, fast 10μs conversion time and no missing codes over the full operating temperature range.

The ZN427 contains a voltage switching D-A converter, a fast comparator, successive approximation logic, three-state output buffers and a 2.5V precision bandgap reference. A logic diagram of the converter is shown in Fig. 2. Only a few passive external components are required. For basic operation these are an input resistor, a reference current resistor and stabilising capacitor, and a limiting resistor for the negative supply current. This will provide a nominal input voltage range of 0 to $V_{REF\,IN}$. Other input ranges both unipolar and bipolar can be obtained by connecting a simple resistor network to V_{IN} (pin 6) as illustrated in Figs. 3a and 3b. Further information on the ZN427 can be found in the data sheet.

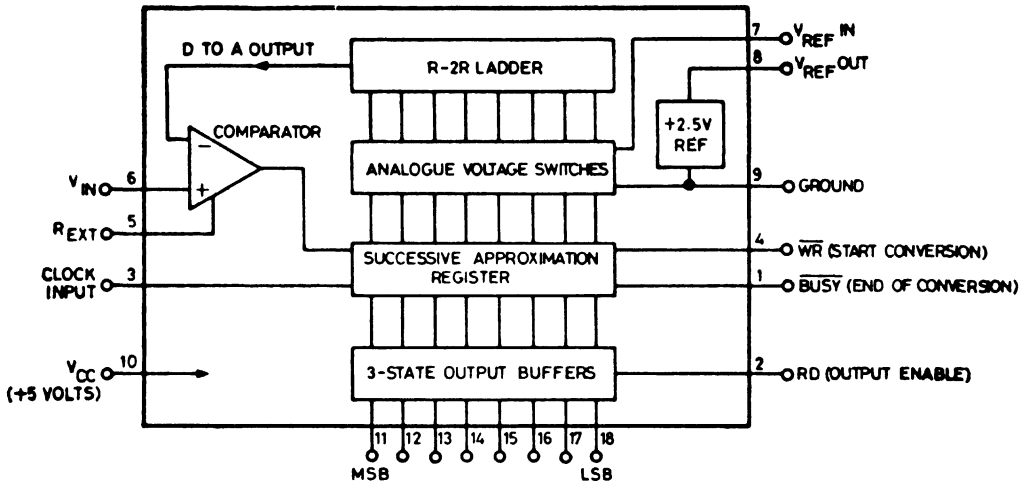


Fig. 2 System diagram

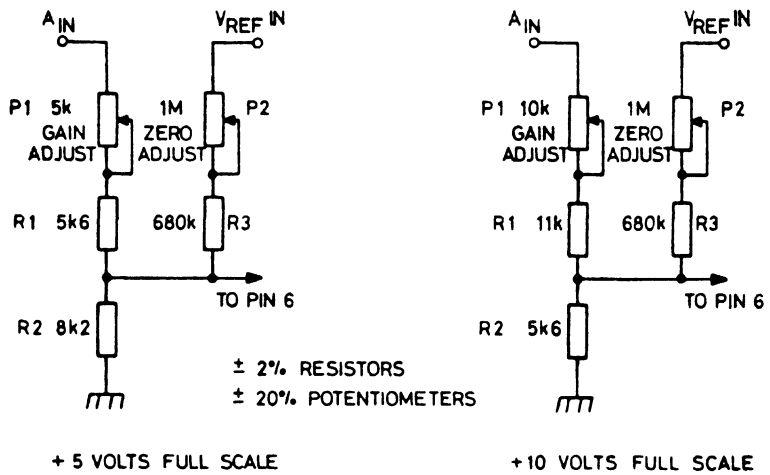


Fig. 3a Unipolar operation - component values

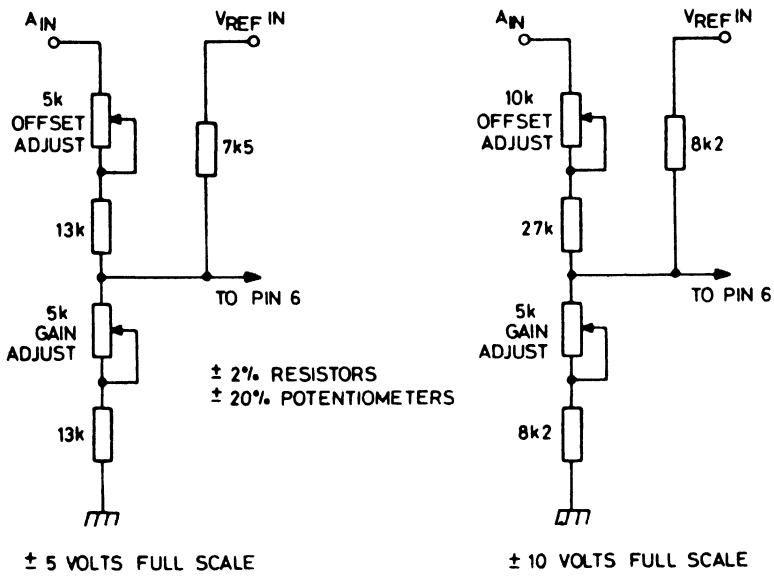


Fig. 3b Bipolar operation - component values

A detailed circuit diagram of the converter interface is shown in Fig. 4.

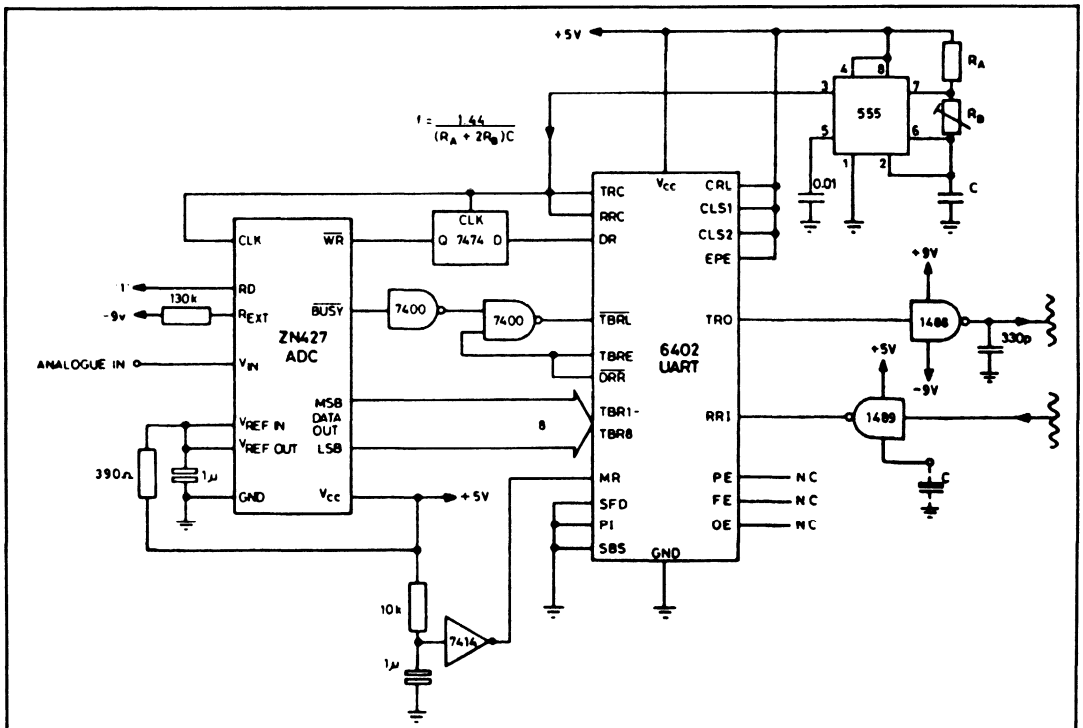


Fig. 4 ZN427 UART interface

The DR output of the UART is connected to the 'D' input of the 7474 latch, the 'Q' output of which drives the $\overline{WR}$ (start convert) input of the ADC. The use of this ensures that the timing of the $\overline{WR}$ pulse with respect to the converter clock input is correct. On the ninth negative clock edge after the $\overline{WR}$ pulse the $\overline{BUSY}$ output goes to a high level signalling that the conversion cycle is complete. This low to high transition is used to load the data into the UART via the TBRL (transmitter buffer register load input). The signal is gated with the TBRE (transmitter buffer register empty) signal which holds the TBRL input high until the UART transfers the data to its transmitter register. If TBRL were allowed to return low before TBRE went high the converter data would be overwritten since the TBR (transmitter buffer register) is a transparent latch. The TBRE signal is also used to drive the DRR (data received reset) input which clears the DR output to a low level allowing another character to be received.

The waveforms associated with this operation are shown in Fig. 5. A simple oscillator using a 555 I.C. is shown which generates both the ADC clock and the transmit/receive clocks for the UART. The external clock is 16 times the data rate, the signal being divided internally by the UART. If a more stable data rate is an important factor then the 6403 UART, which is functionally similar but which uses a crystal oscillator as the timing source, may be substituted. In this case the ADC clock would still be generated by the 555 since it is not necessary for the converter and UART clocks to be synchronised. The UART control inputs CLS1, CLS2 (character length select); PI (parity inhibit); EPE (even parity enable); SBS (stop bit select) are hard wired for whatever data format is wanted.

The MR (master reset) input is driven via a 7414 Schmitt trigger I.C. from a R-C delay circuit to generate the recommended reset pulse after power-up.

The 1488 and 1489 I.C's shown buffering the UART TRO (transmitter register output) and RRI (receive register input) pins are RS-232C compatible line drivers and receivers.

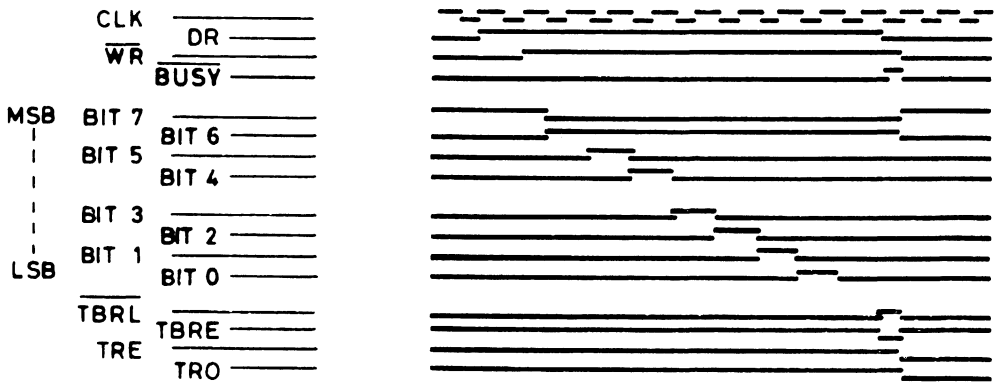


Fig. 5 ZN427 UART interface waveforms

In some applications incorporating microcomputers with RS-232S serial I/O ports no additional interfacing at the data collection centre end will be necessary. However if only a parallel I/O port is provided than another UART to convert the serial data back to parallel will be needed. An interface for the PET microcomputer which connects to the Parallel User Port on connector J2 is shown in Fig. 6. This uses the eight I/O data lines. PA0-PA7 and two control lines CA1 and CB2 which originate from a 6522 versatile interface adaptor I.C. The data lines PA0-PA7 are connected to the RBR (receive buffer register) outputs of the UART. The CA1 input is driven by the UART DR output and is operated in the latched mode which stores the received data within the VIA on a positive transistion of this pin. In order to initiate a new reading from the ADC the remaining control pin CB2 is used. This is connected to the UART inputs DRR and TBRL. When programmed to produce a negative pulse the DR output is reset and a character is transmitted to the converter UART to start a new conversion cycle.

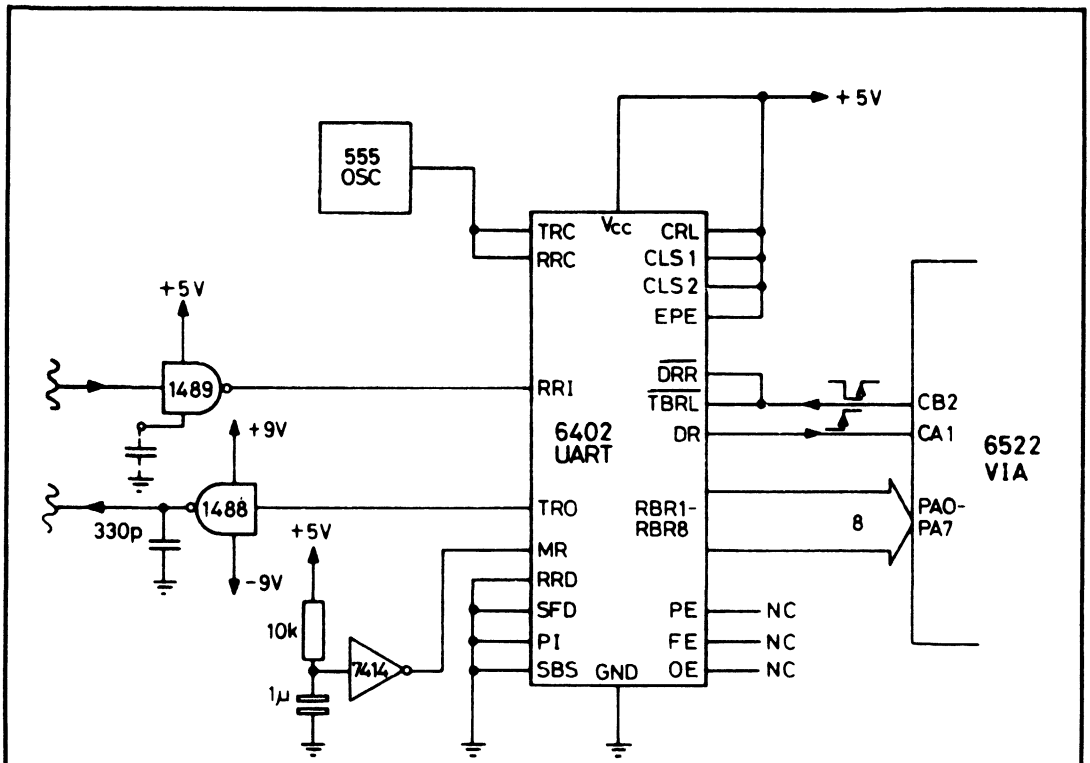


Fig. 6 6522 VIA UART interface

A simple program example in PET basic is shown below.

PROGRAM EXAMPLE

```
 10 REM UART INTERFACE REV. 3
 20 REM SET PORT A TO INPUTS
 30 POKE 59459, 0
 40 REM DISABLE CA1 INTERRUPT
 50 POKE 59470, 2
 60 REM SET PCR TO 111XXXX1
 70 POKE 59468, PEEK (59468) OR 225
 80 REM SET ACR TO XXX000X1
 90 POKE 59467, PEEK (59467) AND 227 OR 1
100 REM CLEAR CA1 FLAG IN IFR
110 A = PEEK (59457)
120 REM PULSE CB2 LOW-HIGH
130 POKE 59468, PEEK (59468) AND 31 OR 192
140 POKE 59468, PEEK (59468) OR 225
150 REM WAIT FOR + TRAN ON CA1
160 REM TEST CA1 FLAG IN IFR
170 IF (PEEK (59469) AND 2) THEN 190
180 GOTO 170
190 REM READ IRA AND CLEAR CA1 FLAG
200 A = PEEK (59457)
210 PRINT A
220 GOTO 120
```

Initially the appropriate VIA internal registers are set up then a negative going pulse is produced on the CB2 pin. This starts a conversion sequence and when the new data is received the CA1 input goes high, latching the data in the VIA, and setting the CA1 flag bit in the interrupt flag register. This flag is tested by the program and when set the data is read and printed out. CB2 is again pulsed low and the sequence repeated.

For 6502 based microcomputer systems where all I/O lines of a 6522 VIA are available the CA2 pin can be used in the read handshake mode in place of the CB2 pin, simplifying the program. Also the status flag of the UART can be monitored by other I/O port lines for error checking purposes.

Microprocessor Interfacing using the ZN432 10-Bit Data Converter

This application note describes a monolithic 10-bit accurate analogue to digital (A-D) converter integrated circuit and explains the different techniques of interfacing this to common 8-bit microprocessors using the minimum of external discrete components and standard TTL logic elements.

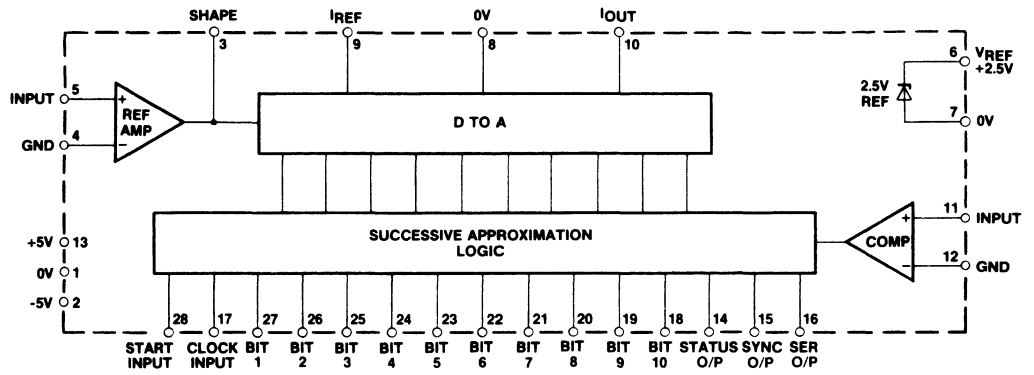


Fig. 1 ZN432 logic diagram

The ZN432 A-D converter

The ZN432 is a 10-bit A-D converter produced in monolithic form by a silicon bipolar process. The converter is of the successive approximation type and includes an on-chip precision reference, reference amplifier, comparator, successive aprroximation logic and a D-A converter. The D-A converter operates on the unit current source principal with a current switching array using a

matrix of diffused resistors. As a result of incorporating several design and layout innovations and the use of highly developed processing and photomask techniques, 10-bit accuracy is obtained without the need for post diffusion trimming operations. Only a few external components are required, including two capacitors, to shape the internal reference and reference amplifier outputs, and several resistors which define the input voltage range of the converter, which can be either unipolar or bipolar whichever range is required by selecting suitable external resistors. The ZN423 is available in 3 temperature ranges, including full military temperature range, and in either 8, 9 or full 10-bit accurate versions, packaged in a 28 lead hermetically sealed ceramic D.I.L. encapsulation.

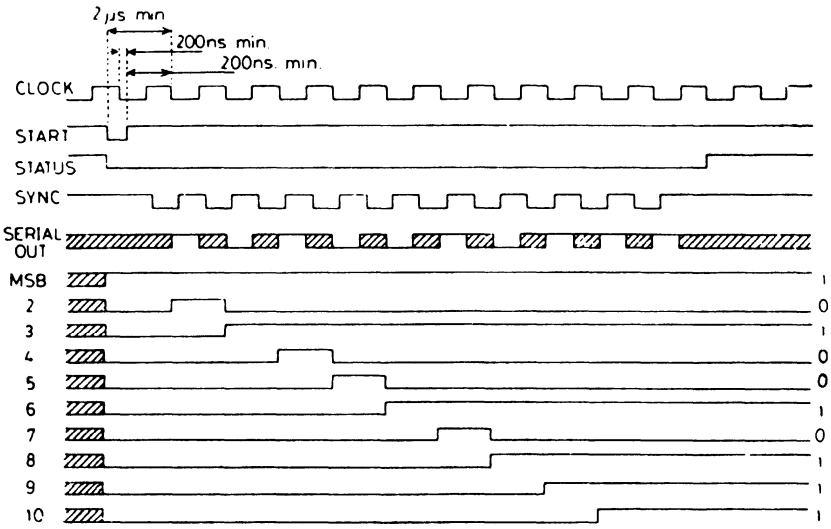


Fig. 2 Timing diagram

The operation of the converter can best be described by reference to the timing diagram, Fig. 2. Conversion is initiated by a negative going START pulse which sets the MSB to a logic '1' and all other bits to a logic '0'. The STATUS output is also set to a logic '0' at this time indicating that the converter is busy. The leading edge of the START pulse should occur at least 2μs before the 1st active negative going edge of the clock and the trailing edge of the START pulse must not occur within $\pm$ 200ns of a negative going clock edge. On the next negative going clock edge a decision is made on whether to set the MSB back to a logic '0' if the input current is less than the D to A output or, if not, it is left at a logic '1'. Bit 2 is switched to a logic '1' on the same clock edge and on the next negative edge a decision is made about bit 2, again by comparing the input current with the internal D to A output. This process is repeated for all 10 bits so that when the STATUS output goes to a logic '1' on the 11th negative clock the digital output from the converter is a valid representation of V_{IN}. A SERIAL DATA output is also provided on the ZN432, this data is outputted during the conversion cycle and is valid on the positive going edge of the pulses on the SYNCH output.

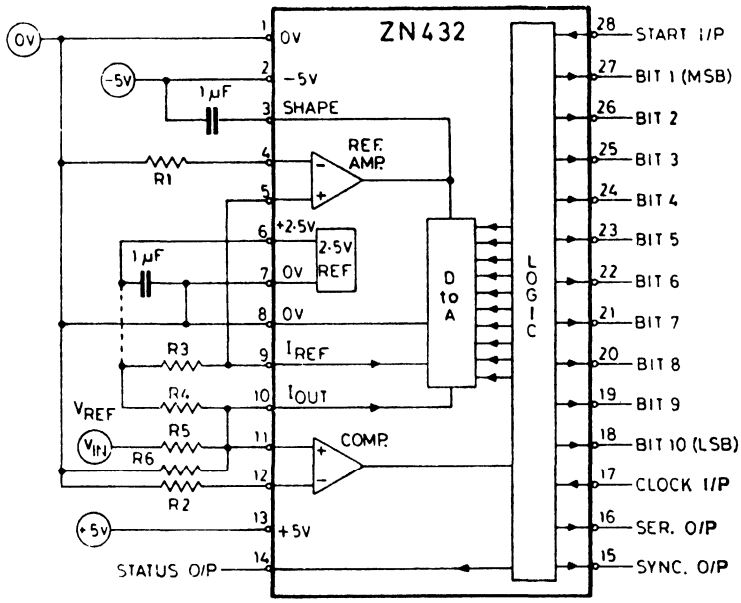


Fig. 3 Typical external components

A diagram showing typical external components for the ZN432 is shown in Fig. 3. The capacitor on pin 3 is used to stabilise the reference loop whilst that on pin 6 is for stabilisation and decoupling of the voltage reference output. Resistors R1 and R2 control the bias current of the reference amplifier and compartor, R3 defines the D-A reference current, R4 and R5 set the input voltage range and R6 is selected to obtain a suitable D-A time constant. For setting up, R3 will adjust the converter gain and R4 the offset. As an example, the resistor values for a ± 10 volt input range are:

R1 = 5kΩ	R4 = 2.5kΩ
R2 = 1.25kΩ	R5 = 10kΩ
R3 = 5kΩ	R6 = 3.33kΩ

Resistors R3, R4 and R5 affect gain and offset and hence high stability types should be used whereas the nearest preferred values may be chosen for R1, R2 and R6. Refer to the ZN432 series data sheet for more information on the selection of external components.

Interfacing data converters to microprocessors

Peripheral devices can be interfaced to microprocessor systems by two basic methods. The first and simplest is to use a general purpose I/O device, (also known as peripheral interface adapters, versatile interface adaptors or programmable peripheral interfaces, etc.). Most microprocessor systems on the market usually include one or more of these components in their microprocessor systems family. They normally consist of one or more data ports, usually of 8 bits which can be programmed to function either as inputs or outputs. With some devices the complete port has to be programmed to function either as all inputs or all outputs, but the more useful I/O devices allow the individual pins of each port to be programmed separately as inputs or outputs. In addition most devices also feature several control lines for the purposes of generating handshake signals with peripherals and generating microprocessor interrupts etc.

The second interface method is to connect the peripheral device directly to the microprocessor data bus. This method is termed memory mapped I/O which as its name implies, is to make each peripheral I/O function appear to the microprocessor as a normal memory location. This allows the full set of memory reference instructions to be used for I/O data transfer, but also implies that the peripheral device must be capable of responding at least as fast as memory, and hence it should be compatible with the MPU bus timing characterisitics. With 10-bit converters a problem exists when using this method in that the 8-bit data bus is not wide enough to handle the converter data as a single word. It is therefore necessary to split the data into two words usually of 8 and 2 bits which are fed to the data bus in two separate bytes by means of appropriate gating on the converter outputs. Naturally when using a 16-bit microprocessor this problem does not arise, as converter data can then be read as a single word on the data bus. The disadvantages of memory mapped I/O are that it usually requires additional address decoding logic and also, since the I/O will be addressed as memory, there will consequently be fewer addresses available for actual memory. A variation of memory mapped I/O commonly referred to as I/O mapped I/O or isolated I/O is available on some microprocessors which overcomes this last disadvantage. This allows a defined range of memory addresses to be used also for I/O by means of separate input and output instructions. A special control output is used to tell the memory I/O devices whether the address of the current read or write cycle refers to memory or to I/O. This technique, does, however, restrict the freedom of the programmer to the use of these input/output instructions which usually operate only on data in the microprocessor accumulator.

So far we have dealt with interfacing to the ZN432 using the parallel binary outputs, alteratively the serial output can be used in applications which demand that the number of lines to the converter need to be kept to a minimum. Two schemes are briefly described here although other variations are possible. The first would be to connect the serial output to one I/O pin of an I/O device and to use the status output to generate microprocesor interrupts via one of the I/O device control inputs, thereby reading the serial data from the I/O device on the positive going edge of each pulse on the status output. The other method is to use a microprocessor with a direct serial input port such as the 8085A. This would either involve synchronising the converter clock to a sub-multiple of the microprocessor clock and programming the microprocessor to read the data at the correct time, or by again using the status output to generate an interrupt. Unfortunately both these methods restrict the maximum converter clock period to a minimum of at least several instruction execution times i.e. the time needed to interrupt the microprocessor, read the data and store it in memory. Another option open to the designer would be to use a cascadeable shift register with three-state outputs (i.e. a TTL 74LS395A) at the microprocessor and to convert from 10-bit serial to parallel data which would then be applied direct to the data bus in 2 words via the three-state outputs.

A ZN432 I/O interface

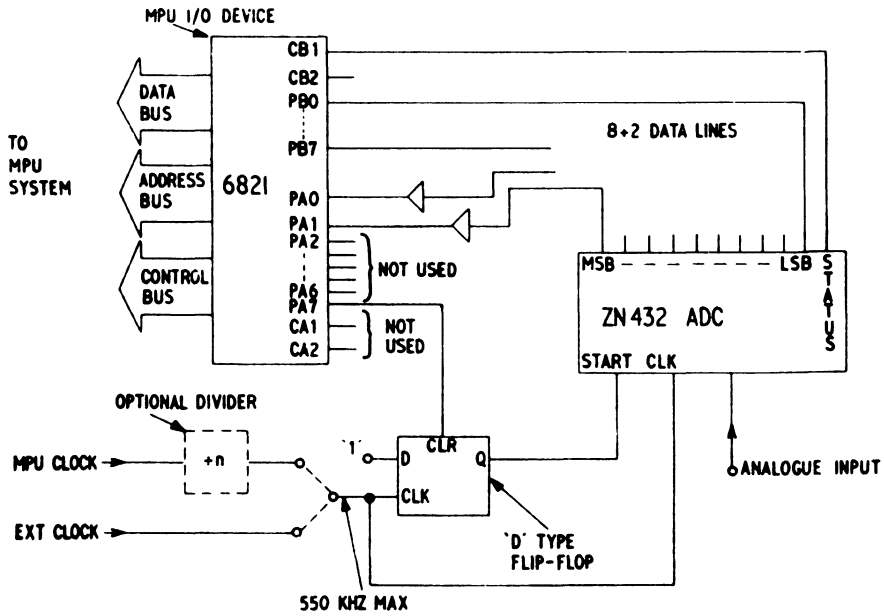


Fig. 4 ZN432 - 6800 I/O interface

Fig. 4 illustrates one configuration of interfacing the ZN432 to an I/O device; in this case the 6821 peripheral interface adaptor (PIA) device of the 6800 microprocessor family.

The PIA provides a flexible means of interfacing byte orientated peripherals to the microprocessor through two 8-bit bi-directional peripheral data lines and four control lines. The functional configuration of the PIA is under the full control of the microprocessor. Each of the peripheral data lines can be programmed individually to act either as an input or an output and each of the four control lines may be programmed for one of several control modes.

The diagram shows all 8 lines from port B and two lines from port A connected to the binary outputs of the ZN432. These lines are programmed as inputs and allow the microprocessor to read the converted data by the execution of a microprocessor read peripheral data operation. Note the use of the two buffers on data lines PA1 ad PA2, these are necessary due to the higher input current of the port A inputs.

The converter clock can be supplied either from the microprocessor clock or from the external source. Use of the microprocessor clock is preferrable since this allows a precise calculation to be made of the conversion time in terms of microprocessor machine cycles. If, however, the microprocessor clock is greater than the maximum converter clock rate of 550kHz then it must be divided down to an acceptable level.

The 'D' type flip-flop is used to generate the start pulse for the converter from the PA7 line, programmed as an output. The function of this flip-flop is to ensure that the start pulse timing criteria with respect to the clock are met as explained earlier.

The STATUS output from the ZN432 is connected to CB1 control line. This can be programmed to set the interrupt flag bit-7 in control register B of the PIA, on occurance of a positive transition of the CB1 input signal. The contents of this register can be read by the mciroprocessor and the state of this bit tested to determine the completion of the conversion

cycle. Alternatively the PIA can be programmed to generate a direct microprocessor interrupt from the status signal on CB1. In this case, an interrupt routine in the program would be accessed on completion of a conversion and this would transfer the converter data via the PIA to defined storage locations in microprocessor registers or memory. This method is really only necessary if maximum utilisation of microprocessor time or converter data throughput is required. For situations where this is not critical the converter clock can be synchronised to the microprocessor clock as previously described, and a delay loop built into the program to allow for the conversion time. Since this is only 20μs when running at the maximum clock rate a delay loop of only a few instructions will be sufficient to produce adequate delay.

A typical program to control the converter may be organised as follows:

Initially the PIA would be set-up with PB0-PB7, PA0 and PA1 as inputs, PA7 as an output and control register B set to generate a microprocessor interrupt on a positive transition of the CB1 input. Note that the remaining lines PA2-PA7, CA1, CA2 and CB2 are unused. A logic '0' followed by a logic '1' is then written to PA7; this clears the 'D' type and sets the START input, via the Q output, to a logic '0'. On the first positive going clock edge after PA7 returns to logic '1' the Q output is clocked to a logic '1' allowing the ZN432 conversion cycle to proceed. (Note that it is not important if the START input is held low for several clock cycles, it will simply hold the converter with the MSB at a logic '1' and all other bits at a '0'). On the 11th negative clock edge after the start pulse the STATUS output goes to a logic '1' indicating that the ZN432 had finished the conversion. This postive transition activates the $\overline{IRQ}$ line of the 6800, via the PIA, causing an interrupt. The 6800 stops execution of the current program sequence and begins an interrupt sequence. This involves saving the microprocessor register contents on the stack and setting the Interrupt Mask Bit so that no further interrupts will be serviced. The microprocessor is then directed to a vectoring address and branches to an interrupt routine in memory. This routine will read the converter data, via the PIA by addressing ports A and B in turn and will then either store the data away in memory for future use, or will test the data and act accordingly on the results. Reading the data on port B of PIA also has the affect of clearing the interrupt flag bit. Resumption of the interrupted program sequence can now be made by execution of a return from interrupt (RTI) instruction.

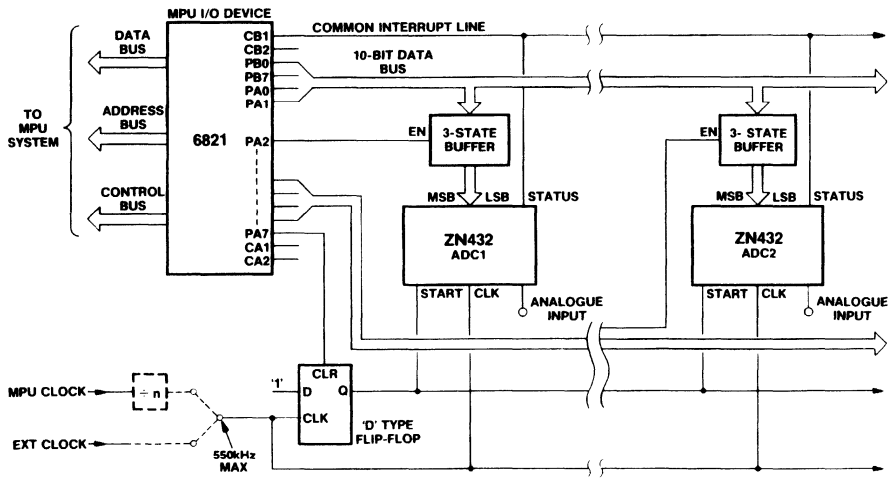


Fig.5 Multiple ZN432 6800 I/O interface

The configuration illustrated in Fig. 5 shows a suggested scheme for interfacing several ZN432's to an I/O device. This arrangement is similar to that previously described but in this circuit three-state buffers are used to interface each ZN432 to a common 10-bit bus from the PIA. The previously redundant lines PA2-PA6 are now used to provide the enable signals for the three-state buffers. Note that the buffers of only one converter should be enabled at any one time otherwise false data will be read from the PIA.

The STATUS output of the ZN432 has a resistive pull-up load allowing typically up to 4 outputs to be 'wire-anded' together to form a common interrupt line. With the particular configuration shown a common start signal for all the converters is produced, again from PA7 via the 'D' type flip-flop. Application of this signal would start all the converters simultaneously and a positive transistion on the CB1 line would signify that all the converters had finished. Data from each converter would then be read by enabling the three-state buffers via lines PA2-PA6 in turn.

A ZN432 Bus interface

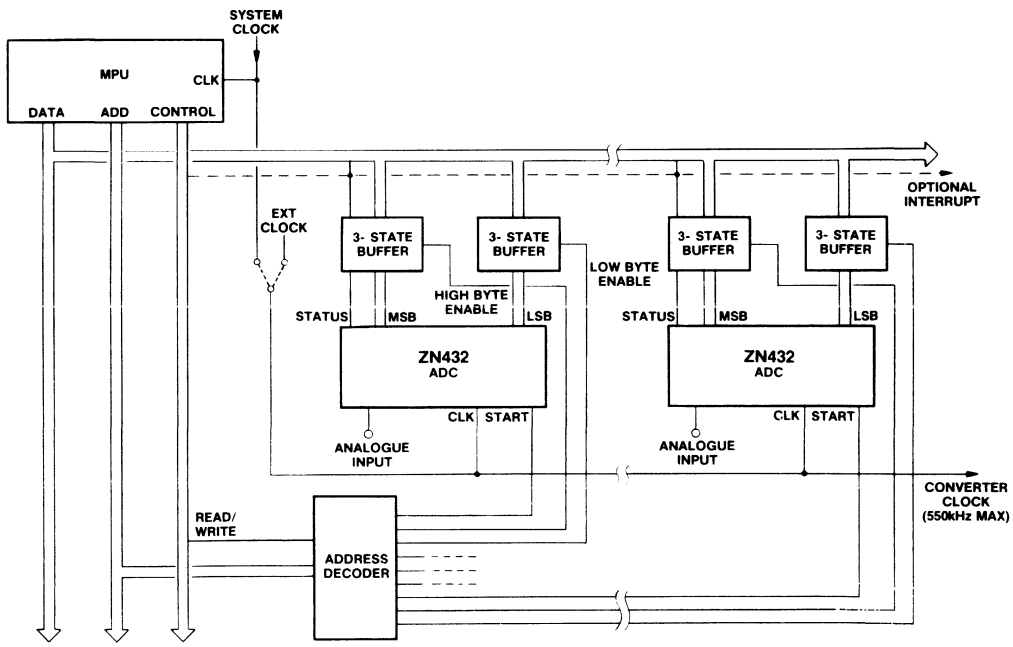


Fig.6 Multiple ZN432 microprocessor bus interface

The most versatile way of interfacing to a microprocessor is to go directly onto the data bus. Fig. 6 illustrates this concept with the ZN432 where three-state buffers are again used but this time connected directly to the date bus of an 8-bit microprocessor such as the 6800. Since it is only an 8-bit bus the converter data has to be read in two words by enabling the buffers per converter in two groups as indicated by the high and low byte enable lines per converter. One suggested scheme would be to transfer the output data as shown in Table 1. (Note that in converter terminology bit 10 is the least significant bit (LSB).

Table 1

Data bus lines	Low byte	High byte
D7	Bit 3	–
D6	Bit 4	–
D5	Bit 5	–
D4	Bit 6	–
D3	Bit 7	–
D2	Bit 8	(Status)
D1	Bit 9	Bit 1 (MSB)
D0	Bit 10 (LSB)	Bit 2

The STATUS output can be read on the data bus with the high data byte or alternatively these outputs can be 'wire-anded' or gated together to produce a common interrupt signal.

The start pulse and high and low byte enable signals are generated from a logic block labled 'address decode logic'. The function of this is to drive the appropriate input when the address, which has been allocated to that particular input, is present on the address bus and the control bus signals indicate a valid memory read or write operation. Note that the level of address decoding used must ensure that the three-state buffers are disabled at all times except when the actual converter data should be on the bus, otherwise bus contention problems, with other devices using the bus may occur. A convenient means of address utilisation for the system in Fig. 6 is shown in Table 2, which allocates two consecutive addresses to each converter.

Table 2

Address	MPU read	MPU write
XXX 0	High byte enable ADC1	Start ADC1
XXX 1	Low byte enable ADC1	Start ADC1
XXX 2	High byte enable ADC2	Start ADC2
XXX 3	Low byte enable ADC2	Start ADC2
XXX 4	High byte enable ADC3	Start ADC3
etc.	etc.	etc.

(XXX = unique address for particular MPU system.)

A write instruction to either address will then start that converter. On completion of the conversion, detected either by interrupt, testing of the status bit, or fixed program delay, the converter data can be read by a double byte load instruction which will load the data into two consecutive RAM memory locations or into a 16-bit microprocessor register, (i.e. instruction LDX - load index register of the 6800, loads the more significant byte of the index register from the byte of memory at the address specified by the program and loads the less significant byte of the index register from the next byte of memory at one plus the address specified by the program).

Note that the 'D' type flip-flop is not shown in Fig. 6. With a direct microprocessor clock it is possible to design the address decode logic so that the timing criteria of the start pulse with respect to the clock input is complied with.

Summary

Numerous different microprocessors are currently available and each microprocessor based control system will have its own individual data acquisition requirements. It is impossible in a paper of this type to cover all possible permutations of microprocessor/converter interfaces, but adoption of one of the two basic methods described here should be possible with most 8-bit microprocessors, allowing the design engineer to produce the most efficient data acquisition system to meet his design objectives. The ZN432's versatility and ease of use, coupled with its wide operating temperature range and TTL compatibility, will allow it to be used in a diverse range of applications where 10-bit accuracy is necessary.

Further information on the device characteristics and gain selection components, etc., is given in the ZN432 series data sheet.

Introduction to the ZN433 10-Bit Tracking ADC and How to Evaluate Design Performance

The Plessey Semiconductors ZN433 is a monolithic 10-bit tracking A-D converter and as its name implies, it is capable of following changing analogue inputs. It uses an UP/DOWN counter, a D-A and a window, comparator as shown in the schematic diagram (Fig.1). A window comparator is similar to a normal comparator except that, at the input, there is a 'dead band' or 'window' within which the output will not change state. This window is normally ±½ LSB wide.

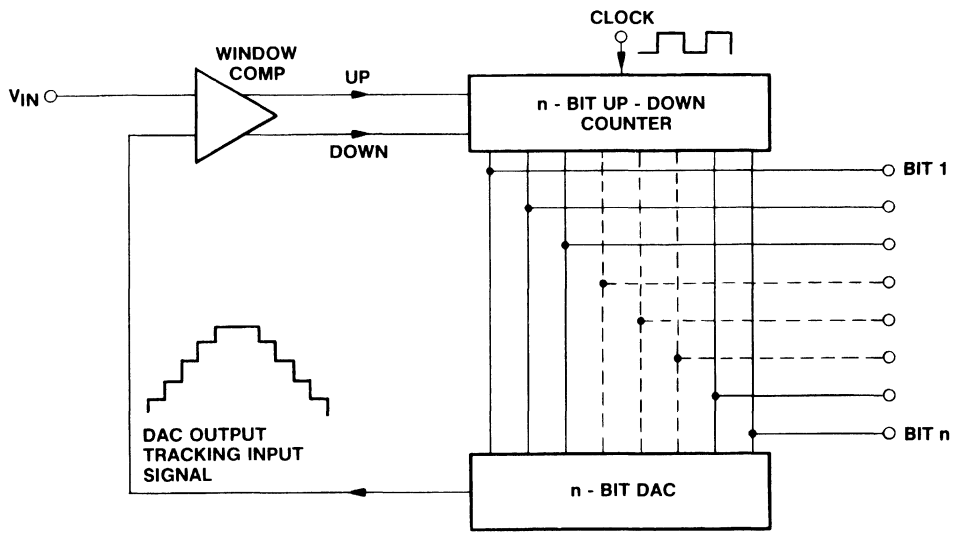


Fig.1 Tracking ADC

When the DAC output is less than the analogue input the comparator instructs the counter to count up and the DAC output thus increases. If the DAC output is greater than the analogue input the comparator causes the counter to count down, thus decreasing the DAC output. When the DAC output is equal to the analogue input ±½ LSB, the input is within the 'window' of the comparator and the counter is stopped. This is illustrated in Fig.2.

A tracking converter can have speed advantages over the staircase and compare and successive approximation type of converters, since the counter of the latter two can only count up and must therefore be reset between conversions.

If the rate of change of the analogue input is always less than 1LSB per clock period then a tracking converter will acquire and track accurately the input voltage and the conversion time will be one clock period. The staircase and compare converter would have to reset its counter to zero and then count up again until the new count is reached. A successive approximation converter would take at least n-½ clock pulses, where n is the number of bits.

As an extreme example consider an analogue input that changes from VFSO to (VFSO-1LSB). The staircase and compare converter will require $2^n - 1$ clock pulses for the first conversion and $2^n - 2$ clock pulses for the second conversion.

The tracking converter on the other hand, will require $2^n - 1$ clock pulses for the first conversion but only 1 clock pulse for the second conversion. This is illustrated in Fig.3.

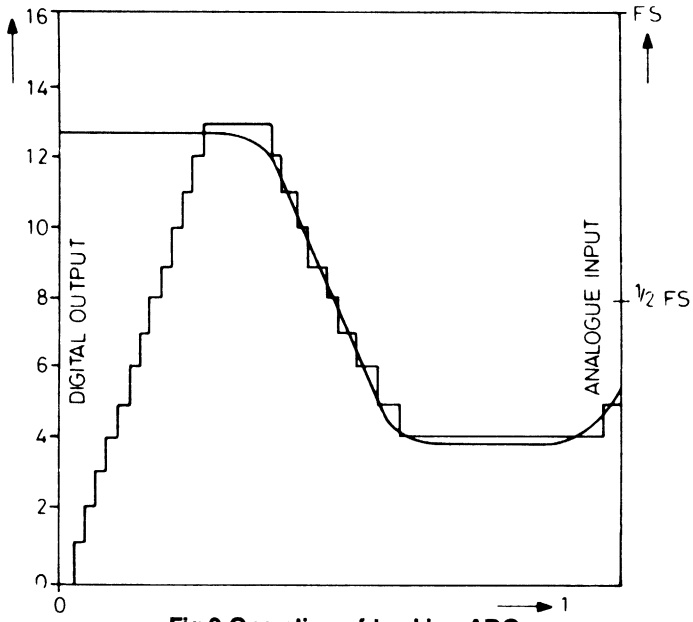


Fig.2 Operation of tracking ADC

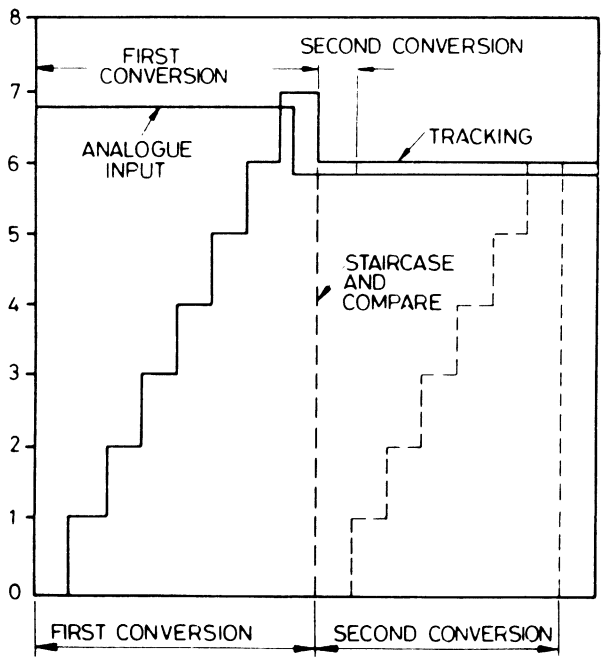


Fig.3 Comparison of ramp and compare and tracking ADCs

In general it can be said that a tracking converter will follow signals whose rate of change is less than ± 1 LSB/clock period. If this condition is met there is no need to use a sample and hold circuit on the analogue input.

The Plessey ZN433 has a maximum clock rate of 1MHz. It is capable of generating parallel or serial output data. The data can be latched (by pin 28) and read out serially or in parallel as required. If desired the outputs can also be disabled by applying a low to send data (pin 17).

The evaluation board is designed to be versatile in demonstrating the properties of the ZN433. The outputs can either drive LED's via inverting buffers and give a visual indication of the output states, or be connected to a bus via non-inverting tristate buffers. The outputs and $\overline{\text{ENABLE}}$ of these buffers are connected to a 20-way speedbloc connector (allowing data to be read as 1 or 2 bytes) as are the control pins for the ZN433 (allowing data latching and serial data manipulation).

The ZN433 can be driven from either an external or on-board clock.

The analogue input and power supplies enter via a 9-way D-type connector.

HOW THE ZN433 WORKS

The chip basically comprises a 2-5V reference, a reference amplifier, a D-A converter, an UP/DOWN counter controlled by a window comparator, and a data latch/shift register (see Fig.4).

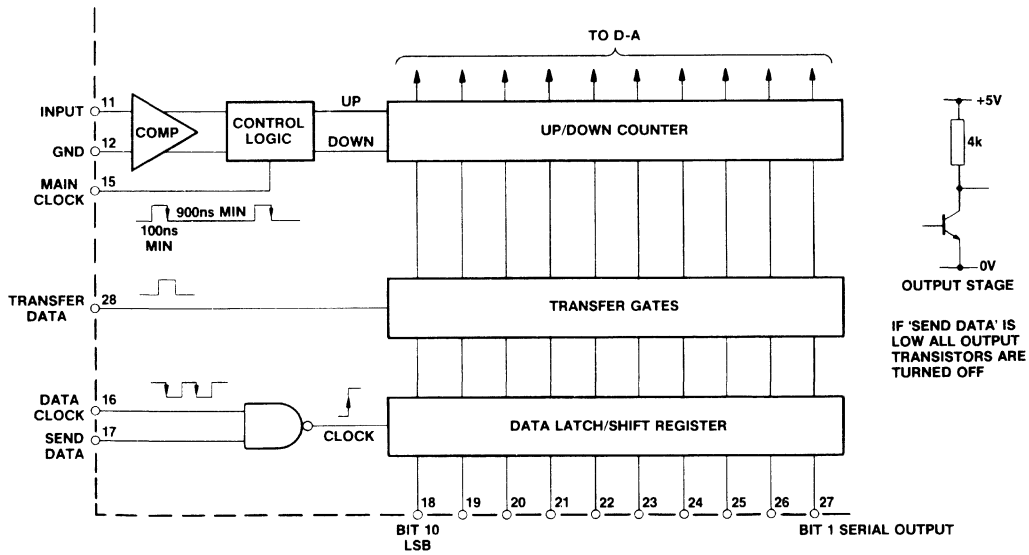


Fig.4 System diagram of ZN433

At the heart of the device is the current source array (CSA) D-A converter (see Fig.5). The unit current in each source is controlled by the output of the reference amplifier (approximately 1.7V). If the logic input is higher than V_{bias} the current is switched to the 0V line, if not, the current is switched to the current summing line.

The bits are weighted by their number of current sources. Bit 1 has 16 current sources, bit 2 has 8, bit 5 has 1. Bits 6-10 current sources have a divide by 16 current divider. Bit 6 has 8 sources, bit 9 has 1. Bit 10 also has 1 but at half the unit current by using twice the resistor value for the emitter resistor. (This enables overall reduction in chip size due to the use of smaller resistors). Hence all the bits have correct weighting. The current sources for the different bits are interleaved to reduce any errors due to temperature gradients and process variations etc.

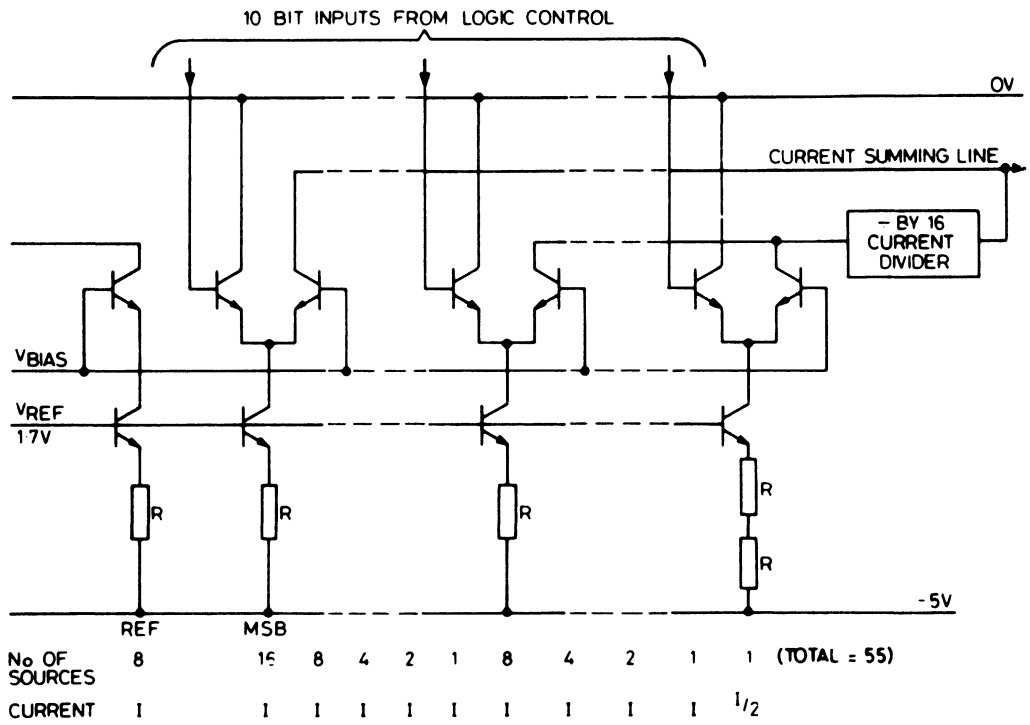


Fig.5 Circuit diagram of current source array (CSA)

There are 8 reference current sources distributed along the array. The reference amplifier controls these and also all the current sources for the bits.

The logic to control the current switching comes from the counter. The counter is instructed to COUNT UP, COUNT DOWN or HOLD by the window comparator. The 'window' is 1LSB wide.

If the input is within ± ½LSB of the digital outputs then the comparator output will instruct the counter to HOLD the count. This means the output will not hunt or exhibit hysteresis. If the input is not within ± ½LSB then the counter will count UP or DOWN as dictated by the comparator.

The counter outputs are connected to the data latch/shift register via transfer gates which are controlled by the transfer data pin (pin 28). If pin 28 is held permantely high then the counter outputs will appear directly at the bit outputs. Data can be latched by taking transfer data high (150nS min.) after the main clock negative going edge and low again before the next main clock negative going edge (50nS min. pulse width).

Data is latched on the negative going edge of the transfer data pulse. Once the data is latched it can be read out serially, from the MSB pin, by applying a data clock to pin 16 (1MHz max., min. pulse width 100nS). Also the outputs can be turned off at any time by applying a low to send data (pin 17). This means that the outputs of a few ZN433's can be wireAND-ed and each device selected individually for reading. However this may cause the V_{OL} of the selected device to exceed the normal TTL low level due to the extra sink current from the additional pull-up resistor(s) on the other device(s). If this presents a problem then the outputs can be connected to logic with a higher input threshold e.g. CMOS.

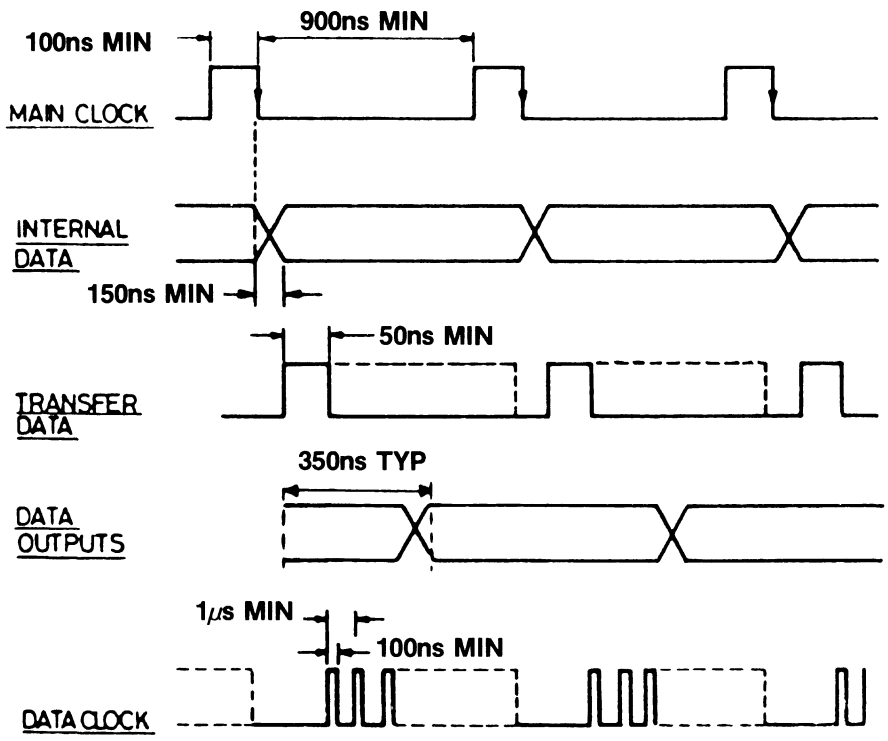


Fig.6 Timing diagram

EXTERNAL COMPONENT CONNECTIONS

Basically the only external components required for the ZN433 to function are two 1 microfarad capacitors and 6 resistors (or less). The basic connections are as shown in Fig.7.

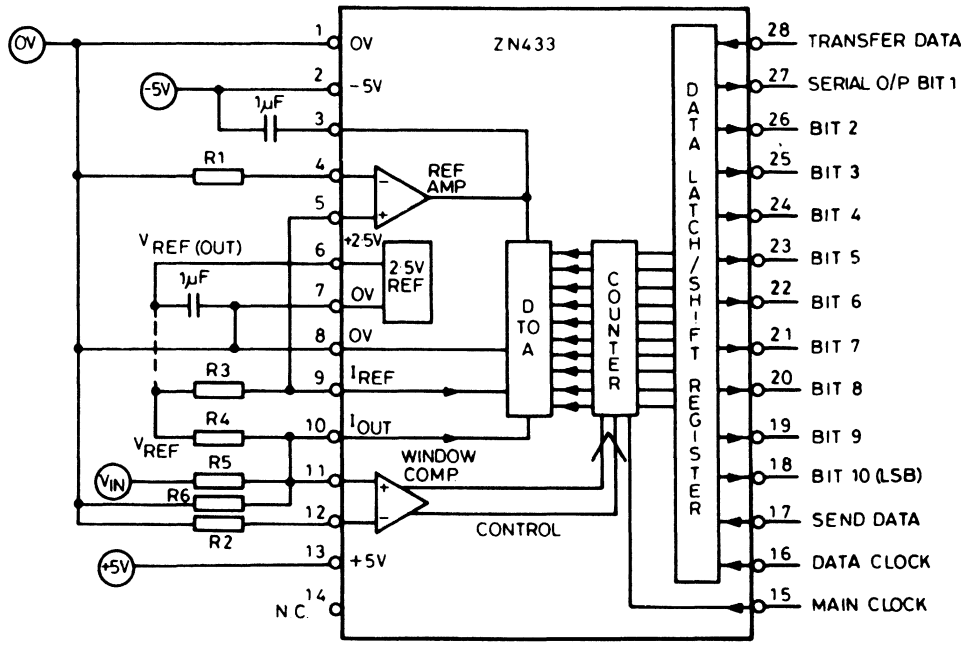


Fig.7 Basic component connections

R1 and R2 tie the inverting inputs of the reference amplifier and the window comparator to ground. The resistance seen by the non-inverting inputs should be equal to that seen by the inverting inputs for low offset and good temperature performance.

R3 sets the reference current which should be 1mA. R4 is only needed when using a bipolar input voltage and is chosen to offset I_{out} as required. R5 is chosen to give a full-scale current of 4mA or if a bipolar voltage is used, a current swing of 4mA. R6 is chosen such that the resistance seen at the non-inverting input of the window comparator is the same as that seen at the inverting input. If a different reference voltage is used and hence a different R3, R1 should still be chosen to be equal to R3. R2 will always be 625ohms.

Resistors R3, R4 and R5 can affect offset and gain and thus require to be of high quality.

The two 1 microfarad capacitors are connected to stabilise the voltage reference and the output of the voltage reference amplifier.

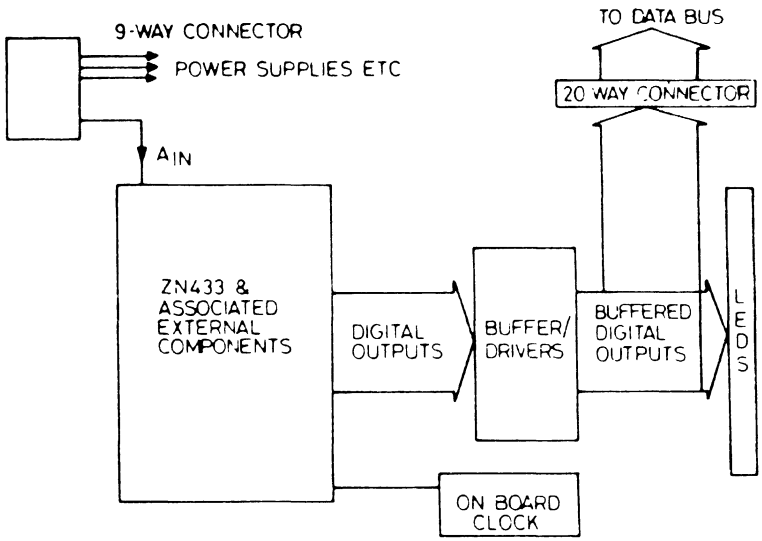


Fig.8 Schematic diagram of evaluation board

The board basically consists of the ZN433 and associated components, an optional on board clock and buffer/drivers to drive either LED's or data bus lines. Inverting buffers are used to drive the LED's and non-inverting buffers are used to drive the bus lines via the 20-way connector. The supplies enter via the 9-way D-type connector.

The outputs from the buffers connect to both the LED's (via resistors) and the 20-way connector. If the LED's are not required they can be omitted and likewise if it is not required to connect to a bus, the 20-way connector can be omitted.

The supply tracks on the board have been made as large as possible in order to minimise any errors due to voltage drops.

The outputs of the ZN433 go to two 16 pin I.C. sockets. In these sockets can be placed either two 16 lead non-inverting buffer/drivers or two 14 lead inverting buffers. At first it may seem odd putting a 14 lead device in a 16 pin socket. The reason is that the 16 pin devices have two pins for controlling the tristate outputs. These are used for connections to a bus.

Obviously these 2 extra control pins are not required when driving LED's hence the use of 14 lead devices. The pin assignments for the two different devices are shown in Figs. 9 and 10.

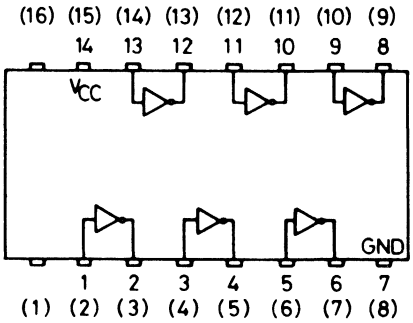


Fig.9 Pinning for 7404, 7405 or 7406
(The numbers in brackets represent the corresponding socket pin numbers)

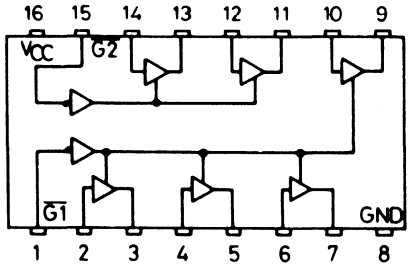


Fig.10 Pinning for 74367

It can be seen that the 14 lead device can be placed in the 16 pin socket as shown and the inputs and outputs of the buffers will be the same for both devices. When the 14 pin device is used the socket pins 15 and 16 must be linked to provide its V_{CC}. As previously stated the outputs go to both the 20-way connector and to the LED's via resistors. By applying the appropriate control waveforms to pins 1 and 15 of the 74367 tristate buffers when certain outputs are connected together, data can be read in two successive bytes on an 8-bit bus.

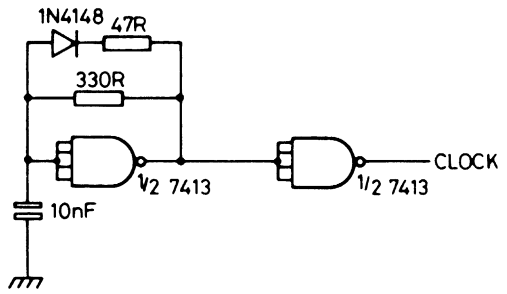


Fig.11 On-board clock generator

The main clock can be generated on board using a TTL dual Schmitt trigger circuit as shown in Fig.11. With the component values given in Fig. 11the frequency is approximately 0.5MHz and the waveform as shown in Fig.12.

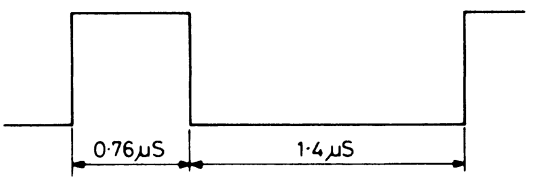


Fig.12 On-board clock waveform

On the negative going edge of the clock the counter is instructed to count UP, DOWN or HOLD. The counter drives the D-A which needs 900ns to settle to the 10-bit accuracy required.

The window comparator compares the D-A output with the Analogue input. The positive going edge of the clock then latches the comparator outputs which subsequently set the counter. The clock must stay high for a minimum of 100ns.

Providing the clock low period is at least 900ns and the high period at least 100ns as stated, the duty cycle doesn't matter. This means that below about 550kHz the clock can be symmetrical because the low period will always be at least 900ns.

If the on-board clock is not required, the clock components can be omitted and the ZN433 can be driven from an external clock. This can enter via the 20-way Speedbloc connector or can enter the board just below the LED's. Here a round BNC connector can either be secured to the board digital ground track directly or be mounted on a bracket which connects to the digital ground track. Connection can then be made to the clock line. Alternatively, the clock input can be soldered to terminal pins at these points.

The maximum analogue input frequency that the ZN433 can track accurately is related to the clock frequency and also the input signal amplitude. The outputs can only change 1 LSB at a time and so the input signal must not change by more than 1 LSB/clock period.

At its maximum rate of change, the ZN433 would take 2^{10} or 1024 clock cycles for its outputs to ramp up from zero (or -full-scale) to +full-scale. Likewise 1024 clock cycles would be needed to ramp back down. Thus 2048 clock cycles are needed for a full-scale change from zero (or -f.s.) to +f.s. and back again. This corresponds to one cycle of a full-scale triangular wave. With a 1MHz clock applied, the ZN433 can accurately track an input signal which changes less than 1 LSB/μs. This means that it can track a full-scale triangular wave input up to a frequency of

$$\frac{1}{2048\mu s} = 488Hz$$

The maximum full-scale sinewave frequency is about 311Hz - due to the fact that the rate of change is not constant but is greatest around zero, hence the maximum slew rate is encountered here.

The maximum frequency that can be tracked is increased when the input signal amplitude is reduced e.g. a half full-scale sinewave input can be tracked up to a frequency of 622Hz etc. However this does mean that resolution is effectively reduced.

The complete circuit diagram for the circuit board is shown in Fig.13. The resistor numbers are the same as used in the diagram on page 2 of the data sheet, where applicable. Resistors R3A and R3B make up the resistor R3 in the data sheet. R3A allows the gain to be adjusted. R4A, R4B and R4C make up resistor R4 in the data sheet and R4B allows the zero offset to be adjusted. R4C is only used when R4 is supposed to be infinite but offset is still required. Otherwise R4A is used with R4B to provide the adjustment, R4C being omitted.

BOARD USED WITH LED DISPLAYS

Primarily to give a visual indication of the state of the outputs during device evaluation. In this configuration the 14 lead inverters are used with pin 1 of the device in pin 2 of the socket etc. Pin 16 of the socket has to be linked to pin 15 of the socket to supply V_{CC} to the inverters.

For parallel output data, transfer data (pin 28), data clock (pin 16) and send data (pin 17) must all be taken high through links (J4, J5 and J6). If serial output data is required then these pins are used to control the latching and movement of the data (see data sheet). They can be accessed via the 20-way connector.

If serial data is not required, this connector can be omitted.

BOARD USED FOR CONNECTION TO A BUS SYSTEM

The 20-way connector allows the ZN433 outputs to be latched and subsequently read via three-state outputs. Hence the 16 lead non-inverting buffers are used (74367's). The LED's and their resistors need not be connected. However (if they are connected, the LED's will be off when the buffer outputs are high or are in the high impedance state!

The outputs of the buffers connect directly to the 20-way connector and so do their control pins to enable them to be turned off as required. Also connected to the 20-way connector are: the ZN433 clock, the transfer data and data clock to allow manipulation of serial data, the send data to turn off all the outputs thus sending them high.

The bit outputs are arranged so that if pin 1, IC2 is linked to pin 1, IC3 (with J12) then bits 3 to 8 will be under the control of this common connection. These $\overline{\text{ENABLE}}$ pins correspond to 10b and 6b on the 20-way connector. Bits 1 and 2 are controlled by pin 15, IC2 (10a) and bits 9 and 10 are controlled by pin 15, IC3 (5b). The outputs are enabled when the $\overline{\text{ENABLE}}$ pins are taken low and are in the high impedance state when the $\overline{\text{ENABLE}}$ pins are taken high.

This arrangement allows the outputs to be read as two words with either bits 1 to 8 and bits 9 and 10 or bits 1 and 2 and bits 3 to 10 as the two words. This is illustrated in Table 1. Also, as can be seen in Table 1, all the outputs can be disabled or enabled at the same time.

20-way connector pins			Outputs selected
10a	5b	10b and 6b linked	
L	L	L	All bits
L	H	L	Bits 1 to 8
H	L	H	Bits 9 and 10
L	H	H	Bits 1 and 2
H	L	L	Bits 3 to 10
H	H	H	No bits

Table 1

BOARD USED WITH EXTERNAL CLOCK

Here the on board clock components can be omitted. Using an external clock enables the ZN433 to be run at any desired frequency within its range. This would be useful if it is wished to synchronise the ZN433 with some other system.

The use of an external clock would probably give better results than the on board clock because the latter tends to generate a lot of noise.

OFFSET AND GAIN SETTING PROCEDURE

The offset and gain are adjusted by R4B and R3A respectively. These are placed near the edge of the board for easy adjustment. The value of the fixed and variable resistor in each case is such that together their values can be adjusted to around the value stated in the data sheet i.e. R3A + R3B = R3, R4A + R4B = R4 (remember R4C is only used when R4 = ∞). The value of the variable resistors is dependant on how fine the adjustment is required to be, but the combination must be chosen to allow sufficient adjustment. The resistors must be of high stability.

Unipolar operation

R4B is used to adjust the zero, it should be adjusted so that for an input of ½LSB, the LSB just flickers between '0' and '1' with all the other bits at '0'. R3A is used to adjust the gain. This should be adjusted so that for an input of full-scale – 1½LSB, the LSB just flickers between '0' and '1' with all the other bits at '1'.

The setting of one control may affect the other so the above procedure should be repeated until both settings are satisfactory.

Bipolar operation

Again R4B adjusts the offset but this time the input is – (full-scale – ½LSB). Again the LSB is required to flicker between '0' and '1' with all the other bits at '0'.

R3A adjusts the gain as above. For an input of full-scale – 1½LSB, R3A is adjusted until the LSB just flickers between '0' and '1' with all the other bits at '1', as for unipolar operation.

The procedure should again be repeated until both settings are satisfactory.

9-WAY CONNECTOR

Pins 2 and 7 are not connected. The wipers of R3A and R4B connect to the voltage reference which is brought out to pin 1. This allows an external reference to be used. The external reference and the internal reference share the same decoupling point on the analogue ground - as they will not both need it at the same time. A capacitor decoupling the external reference can thus be positioned 90° anti clockwise to C5 (the internal reference decoupling capacitor). The internal reference (pin 6) on the ZN433, can be connected to the wipers of R3A and R4B via a link (J2).

The analogue input enters via pin 6. The analogue and digital grounds connect to pins 4 and 8 respectively, and may either be connected together near the chip (using J3) or brought out separately depending on which will give the best results for a particular application.

The – 5V and + 5V supplies connect to pins 3 and 5 respectively and the + 5V auxiliary supply is connected to pin 9. If desired this auxiliary supply can be linked to the + 5V supply (with J1) and used for example to power an external transducer.

Note: The above pin connections apply when the 9-way PCB connector is a socket and will be different if a plug is used.

USING THE BOARD WITH DIFFERENT INPUT VOLTAGE RANGES

Whatever maximum analogue input voltage is used I_{ref} should always be about 1mA and I_{out} full-scale should always be about 4mA. Thus in order to accommodate different input voltage ranges and different reference voltages, the resistors associated with these currents must be changed. How these resistors are calculated and a table of calculated values, for various input voltages, are given in the data sheet.

BOARD LINKS

Optional:

J1 – Links the board +5V to the auxiliary +5V on the 9-way connector to provide a +5V auxiliary output.

J2 – Applies the internal reference to the ZN433 and thus configures the board for operation with the on chip 2.5V reference.

J3 – Connects the analogue and digital grounds together near the ZN433 - may be desirable in some applications.

J4 – Ties transfer data (pin 28) high making the output data latch transparant. Used when the data does not need to be latched.

J5 and J6 – Tie send data and data clock high. Used when the outputs do not need to be turned off, and when serial output data is not required.

J9 and J13 – Connect +5V to the 14 lead inverters, if they are chosen to drive the LED's.

J12 – Links 6b and 10b (on the 20-way connector) together to allow either pin to control bits 3 to 8.

J14 – Links on board clock output to ZN433 clock input, when the on board clock is required.

Mandatory:

J7 and J8 – Provide the ground connections for IC2 and IC3.

J10 – Links bit 2 output from IC2 to the 20-way connector and the relevant LED feed resistor.

J11 – Connects +5V to IC3 socket - pin 16.

ICs				**Capacitors**		
IC1	=	ZN433		C1	=	100μF electrolytic - axial
IC2	=	7404 or 74367		C2	=	100μF electrolytic - axial
IC3	=	7404 or 74367		C3	=	0.1μF disc ceramic
IC4	=	7413		C4	=	1μF tantalum bead
Resistors				C5	=	1μF tantalum bead
				C6	=	0.1μF disc ceramic
R1	=	2.4K		C7	=	0.1μF disc ceramic
R2	=	620R		C8	=	10nF ceramic
R3A	=	1K 20 turn trimpot		C9	=	100μF tantalum bead
R3B	=	1.8K	Depending	**Miscellaneous**		
R4A	=	100K	on input	D1-D10	=	LED's
R4B	=	1M 20 turn trimpot	voltage	D11	=	1N4148
R4C	=	100K	range	IC2 socket	=	16 pin DIL socket
R5	=	620R		IC3 socket	=	16 pin DIL socket
R6	=	∞		IC4 socket	=	14 pin DIL socket
R7-R16	=	330R		**Connectors**		
R17	=	330R		9-way connector	=	D-type sub miniature
R18	=	47R		20-way connector	=	Speedbloc system
				Round chassis mounting connector	=	BNC type

Table 2 Component list

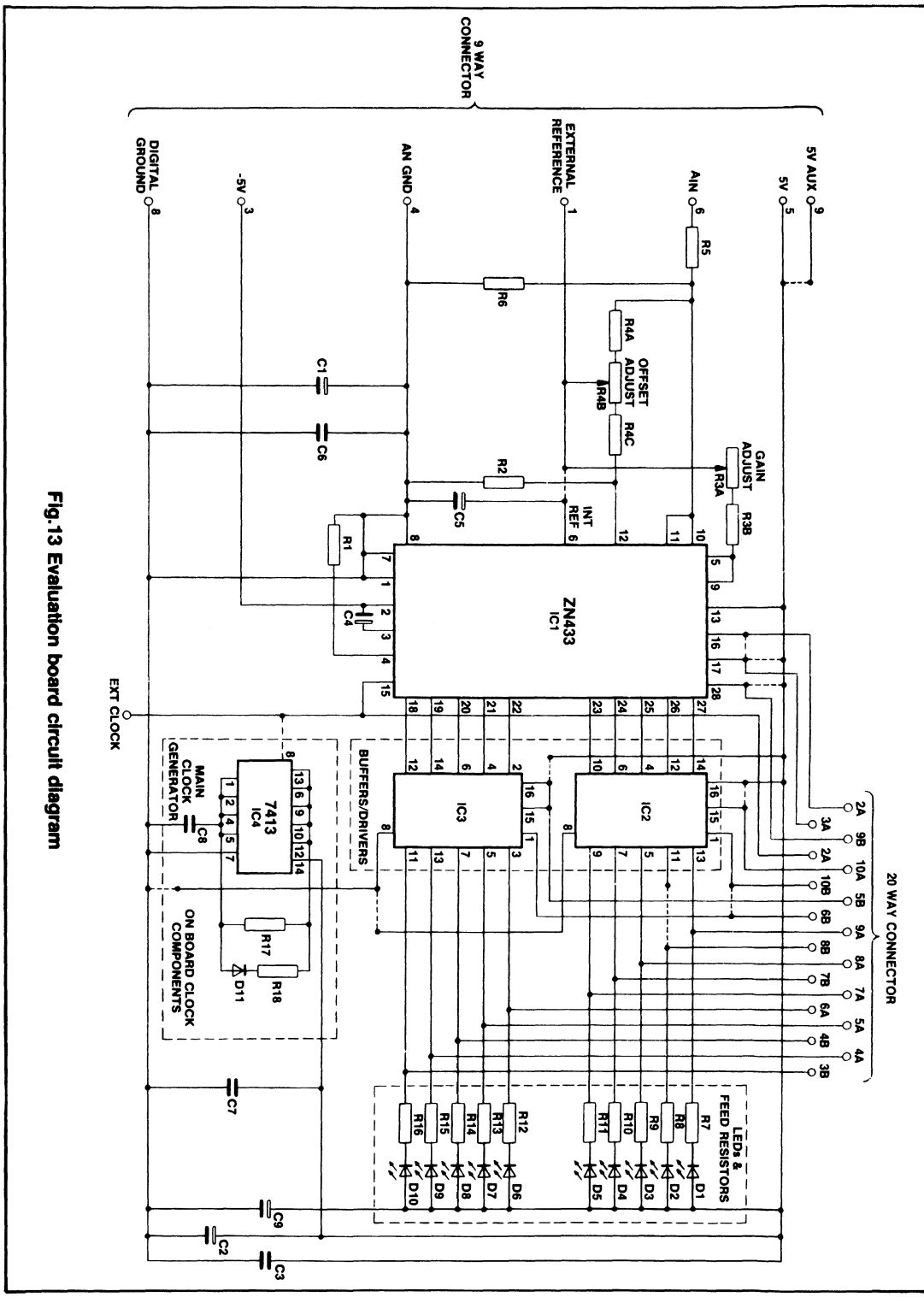


Fig.13 Evaluation board circuit diagram

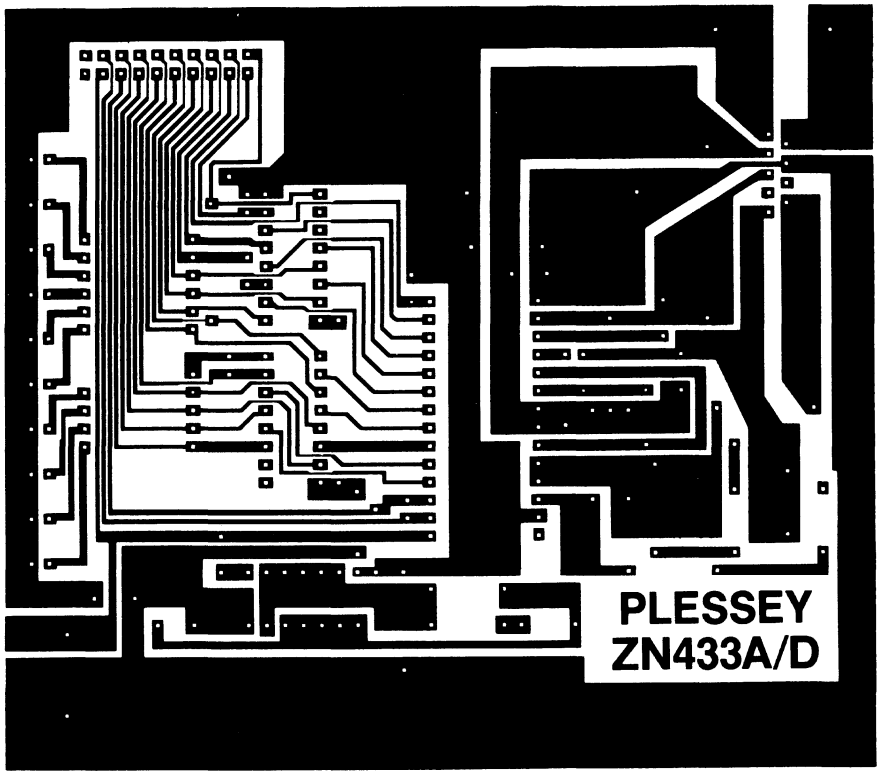


Fig.14 PCB copper side (1:1)

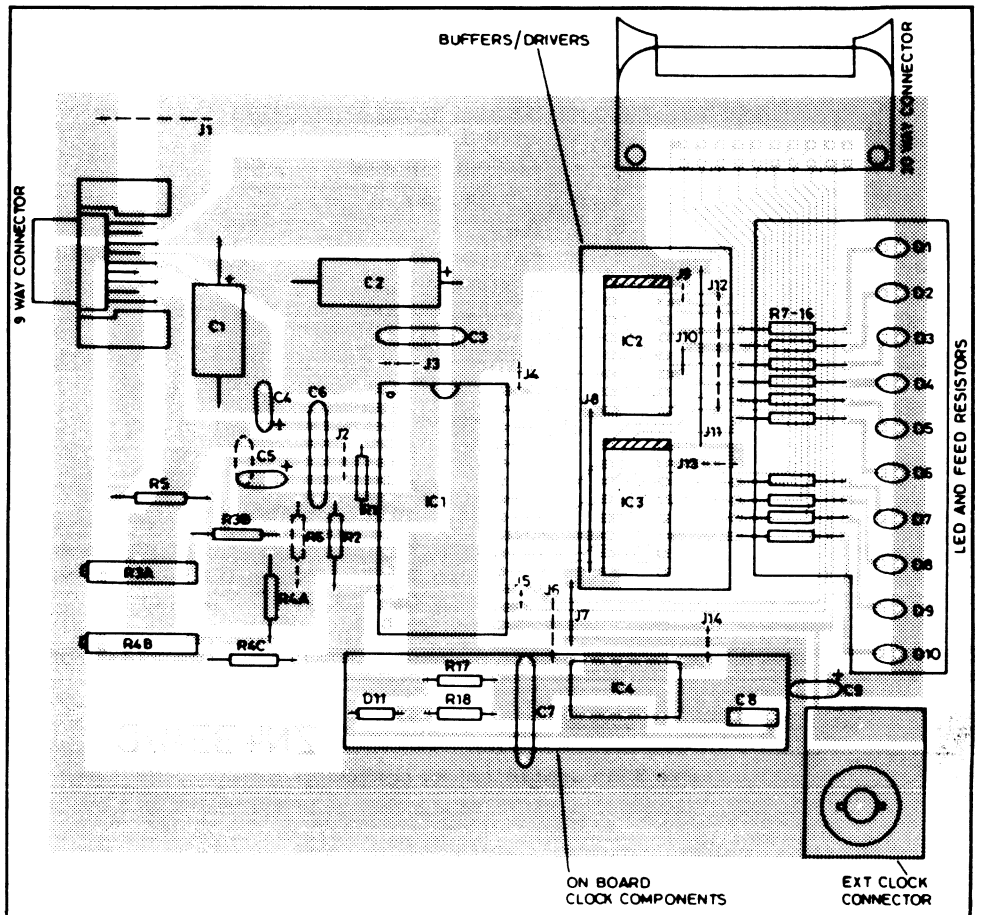


Fig.15 Component layout - actual size

9-way D-type socket

1	=	External reference
2	=	NC
3	=	− 5V Supply
4	=	Analogue ground
5	=	+ 5V supply
6	=	A_{IN}
7	=	NC
8	=	Digital ground
9	=	Auxiliary + 5V

20-way, speedbloc plug

1a	=	NC	1b	=	NC
2a	=	Main clock	2b	=	Data clock
3a	=	Send data	3b	=	bit 10
4a	=	bit 9	4b	=	bit 8
5a	=	bit 7	5b	=	IC 3, output $\overline{\text{enable}}$ 2
6a	=	bit 6	6b	=	IC 3, output $\overline{\text{enable}}$ 1
7a	=	bit 5	7b	=	bit 4
8a	=	bit 3	8b	=	bit 2
9a	=	bit 1	9b	=	Transfer data
10a	=	IC 2, output $\overline{\text{enable}}$ 2	10b	=	IC 2, output $\overline{\text{enable}}$ 1

Table 3 Pin assignment for connectors

Interfacing the ZN439 with the 6500 Family of Microprocessors

The object of this report is to present the techniques involved in interfacing the ZN439 to the 6500 family of microprocessors. The circuit designs were all proven on a 6502 development system but apply equally to all the other microprocessors in the family. Direct bus and port interfacing will be considered for single and multiple converter applications. In both cases polling and interrupt driven examples will be given, highlighting the features which make the ZN439 ideally suited to interfacing to todays microprocessors. Circuit diagrams, as well as flow diagrams and sample programs will be included to give the system designer a full appreciation of what is required.

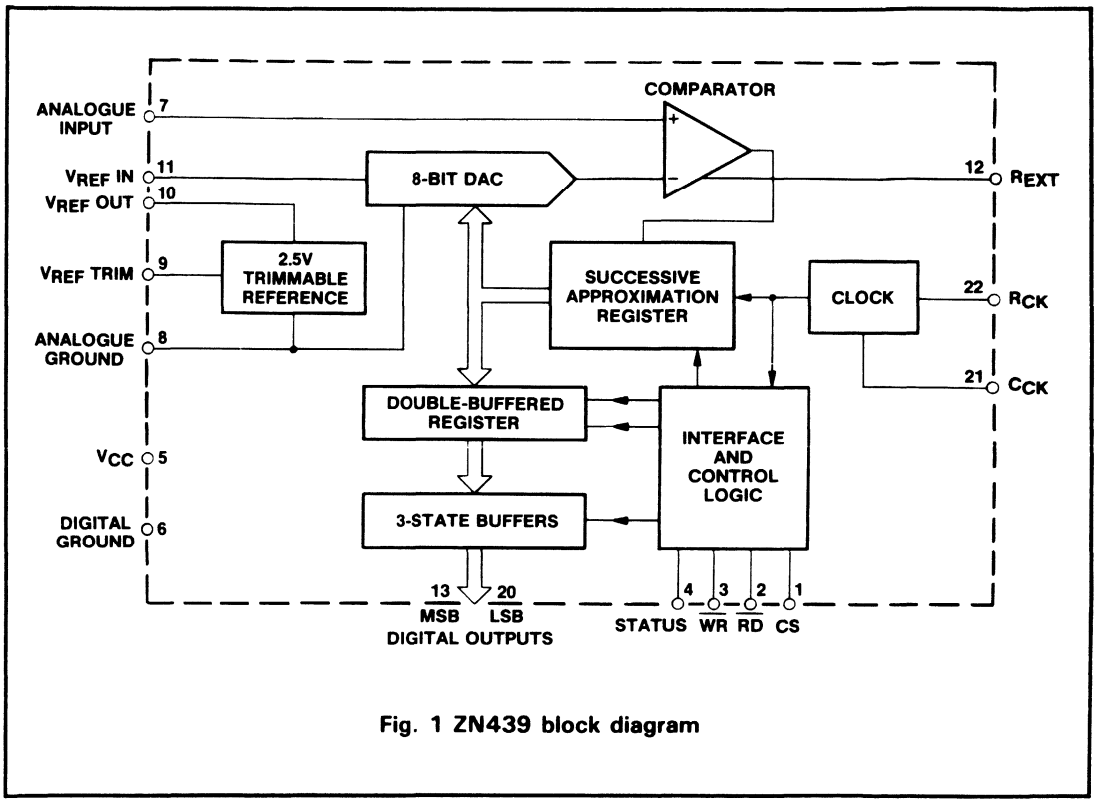


Fig. 1 ZN439 block diagram

THE ZN439 A-D CONVERTER

The ZN439 is an 8-bit successive approximation converter which has been designed to allow simple interfacing to microprocessors. All active circuitry is contained on-chip including clock generator, trimmable 2.5V bandgap reference, control logic and a double buffered register with three-state outputs. The main feature of this device is the use of a double buffered register which allows the outputs to be read at any time irrespective of the conversion status. A block diagram of the device is shown in Fig. 1.

CIRCUIT DESCRIPTION

The ZN439 utilises the successive approximation technique to produce an 8-bit digital output. Upon receipt of a negative going pulse on the $\overline{WR}$ input the status output and the MSB input to the DAC go high while the remaining DAC inputs are taken low. The resulting analogue output from the DAC is compared with the unknown analogue input signal by the comparator. If the input signal is larger, the MSB remains high and if not it is taken low. On the second clock pulse this sequence is repeated for the next most significant bit. This process is continued until all the 8 bits have been compared. On the 8th negative clock edge, status goes low to indicate the end of conversion and providing the $\overline{RD}$ input is high the double buffered register is updated with the new data. For this reason the $\overline{RD}$ input cannot be tied low as this would prevent the double buffered register from being updated. The status output will remain low until either:

a) Another start convert pulse is applied to the $\overline{WR}$ input.
b) The data is read from the converter by applying a read pulse to the $\overline{RD}$ input.

The resetting of the status output by the application of a read pulse makes the device ideally suited to interrupt operation. At the end of a conversion the status output goes low which causes an interrupt within the system. The interrupt service routine will involve reading data from the converter which will take the status output back high and thus remove the interrupt.

The device can also be made to continuously convert by tying the $\overline{CS}$ and $\overline{WR}$ inputs low. In this mode after a conversion is complete the status output goes low and remains low for one clock cycle. Another conversion is then automatically initiated and the status output is taken high. As with the interrupt mode of operation the status output will be taken high prematurely if a read pulse is applied to the $\overline{RD}$ input.

Finally the $\overline{CS}$ input can be used for decoding purposes to enable the device. When the $\overline{CS}$ input is high any $\overline{RD}$ or $\overline{WR}$ signals are locked out and hence ignored by the converter control logic. Timing diagrams for the interrupt and continuous conversion modes of operation are shown in Fig. 2. For further information on this device refer to the ZN439 data sheet.

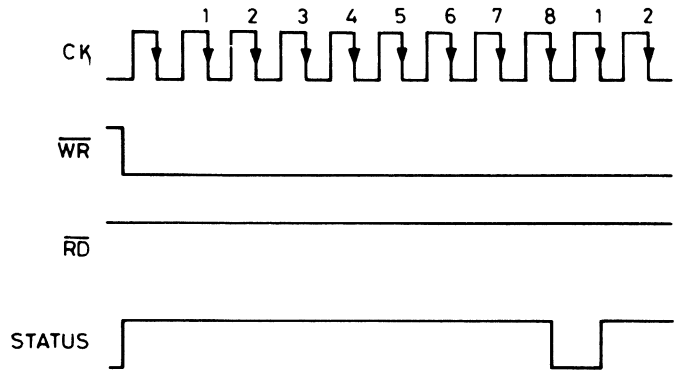


Fig. 2a Continuous conversion without read

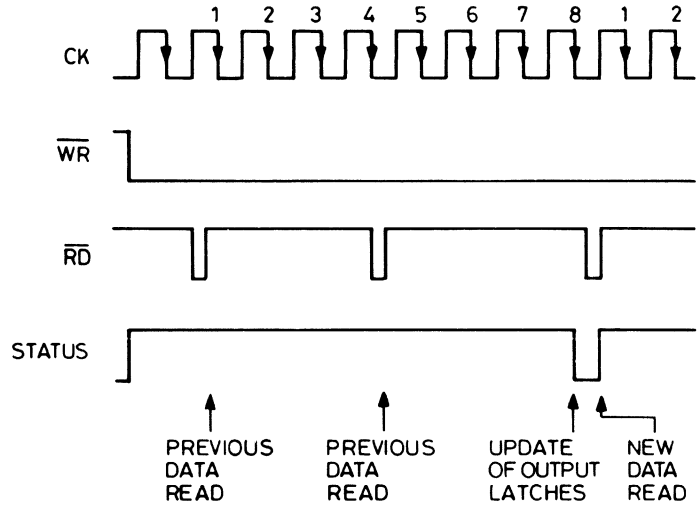


Fig. 2b Continuous conversion with read

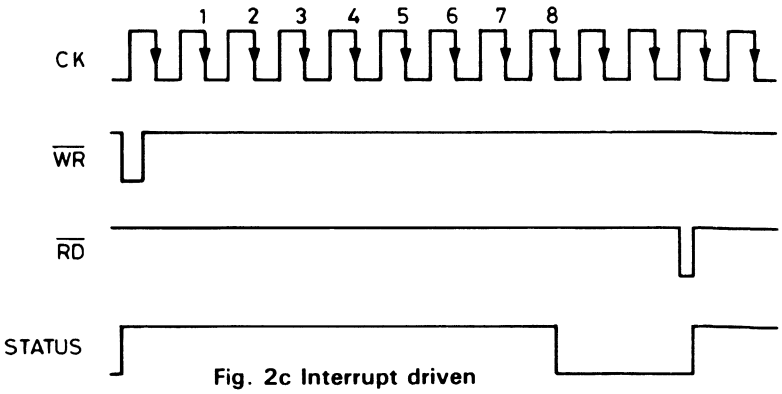


Fig. 2c Interrupt driven

Fig. 2 ZN439 timing diagrams

DIRECT BUS INTERFACING

The 6500 family of microprocessors

The 6500 family consists of 10 NMOS microprocessors. All are bus and software compatible and provide options of addressable memory, interrupt input, on-chip clock oscillators and drivers. There are three speed versions 1MHz, 2MHz and 3MHz which with pipeline architecture provides very fast instruction execution. The series has recently been increased by the introduction of three CMOS microprocessors available in four speed options 1MHz, 2MHz, 3MHz and 4MHz. Each has a 64K byte address range, an improved instruction set, lower power consumption, two hardware enhancements but are all bus and software compatible with the NMOS devices.

A full description of the architecture and instruction set of these microprocessors is beyond the scope of this report. It is therefore assumed that the designer will be familiar with these details. For further information please refer to the 6500 and 65C00 microprocessor data available from the manufacturers or their distributors.

ROM type operation

The most important feature of the ZN439 is the ability to read valid data at any time independent of the conversion status. This makes the device ideally suited to ROM type operation. By using a minimal amount of address decoding the ZN439 can be located within the system memory map in the same manner as a ROM. The decoded enable line is connected to the $\overline{RD}$ input of the ZN439. Therefore whenever the microprocessor reads data from this address the $\overline{RD}$ input is taken low and the ZN439 places valid data onto the bus. The $\overline{WR}$ and $\overline{CS}$ lines are tied low so that the ZN439 cycles continuously. In this manner any data read is guaranteed to be at worst 5μs old, assuming a clock speed of 1.6MHz. A block diagram showing the connections required is given in Fig. 3.

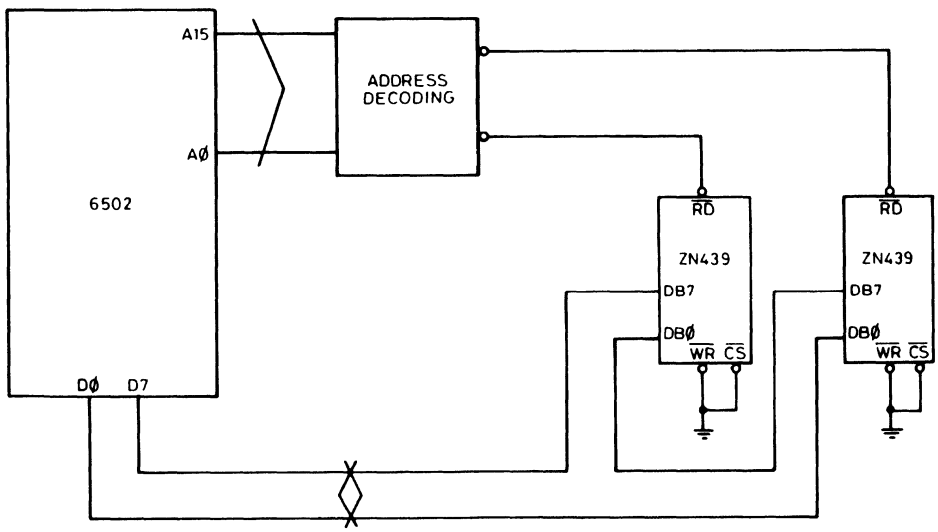


Fig. 3 Direct bus interfacing

Interrupt driven operation

If the data from the converter is to be read infrequently the designer may prefer the device to be interrupt driven. In this mode of operation a low going start convert pulse is applied to the $\overline{WR}$ input. At the end of conversion the high to low transition of the status output is used to generate an interrupt. This is done by buffering the status output with an open collector buffer whose output is connected to the microprocessor $\overline{IRQ}$ input. Data is read from the ZN439 during the interrupt service routine. The action of reading the data sets the status output back high and so removes the interrupt. A block diagram is shown in Fig. 4.

It should be noted that after power up the status output will go low thus pulling the $\overline{IRQ}$ line low. Therefore a 'dummy' ZN439 data read should be performed to set the status line high and remove the interrupt. This will prevent erroneous data being read once the microprocessor has enabled interrupts after power up.

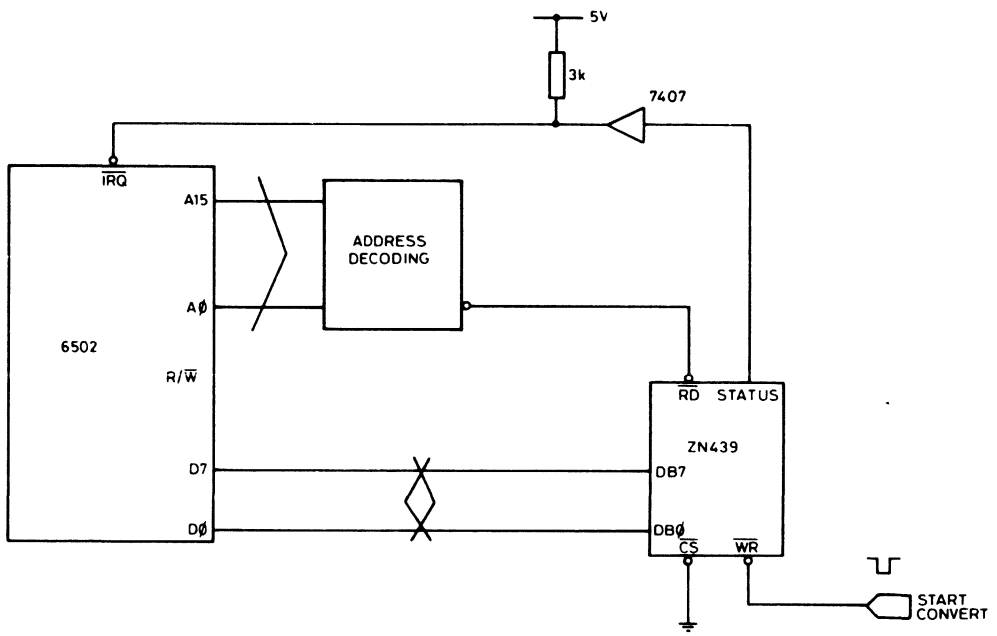


Fig. 4 Interrupt driven direct bus interfacing

Another interrupt driven application would be operating the device in its continuous conversion mode with a slow clock (e.g. 1KHz). This method could be employed when monitoring a slowly varying analogue voltage. Providing the input voltage did not change by more than 1LSB during a conversion cycle the digital result will be 8 bit accurate. The microprocessor interrupt would be generated using the status buffering already described. In this mode the status and hence the $\overline{IRQ}$ line would remain low for 1 clock cycle. Care must therefore be taken to ensure that the microprocessor can respond to the interrupt within this time. If the microprocessor doesn't respond within 1 ZN439 clock cycle then the interrupt will be missed. This will only usually be a problem in multi-interrupt systems. In such a system the ZN439 interrupt may be ignored by the microprocessor until it has finished servicing another interrupting device. Therefore the other interrupt service routine must not be longer than 1 ZN439 clock cycle.

Multi-interrupt systems

In some systems more than one device may be capable of generating an interrupt. In these multi-interrupt systems some form of polling will be required to determine the origin of the interrupt. This means that each interrupting device must provide some form of flag to indicate to the microporcessor that it has requested the interrupt. The easiest way of providing this with the ZN439 is by using the status output as an interrupt flag. This can be implemented by connecting the status output via a three-state buffer onto bit 0 of the data bus. The enable line of the three-state buffer is derived from the address decoding in the same manner as the $\overline{RD}$ input of the ZN439. Therefore by reading the data from this address and testing bit 0 the microprocessor can determine whether the ZN439 is responsible for the interrupt.

An example of this is given below where two ZN439's occupy successive addresses in the memory map. Each have separate asynchronous start convert ($\overline{WR}$) inputs. The status output of the first is connected to bit 0 and the second to bit 1 of the data bus in the manner described above. By reading the data from the flag address and examining bits 0 and 1, the microprocessor is able to determine which converter has generated the interrupt. A circuit diagram is shown in Fig. 5. A typical interrupt flow diagram and program are given in Fig. 6 and Fig. 7 respectively.

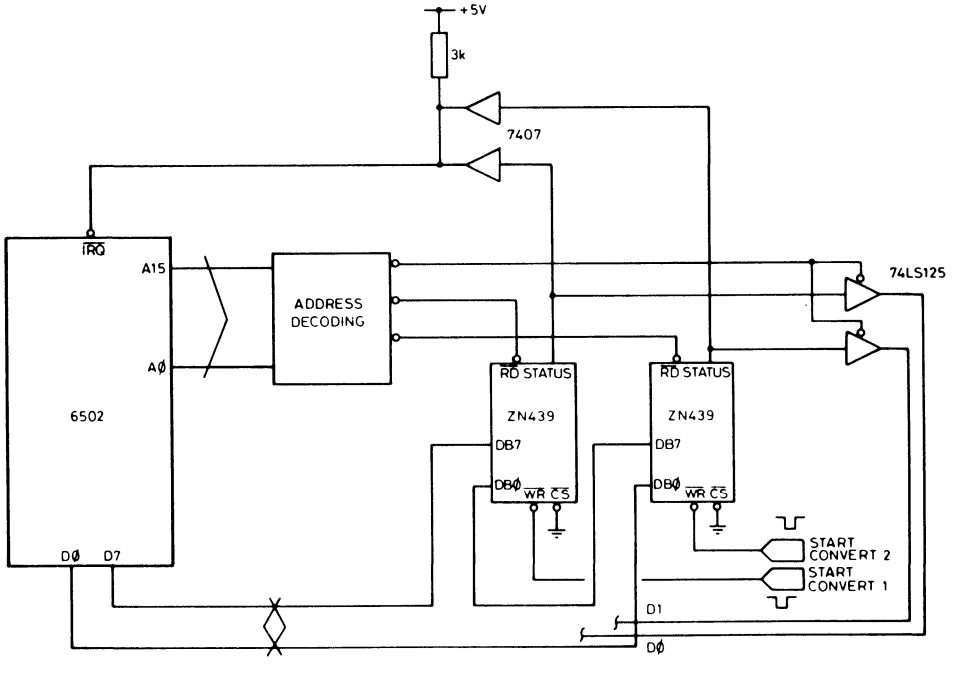


Fig. 5 Multi-interrupt direct bus interfacing

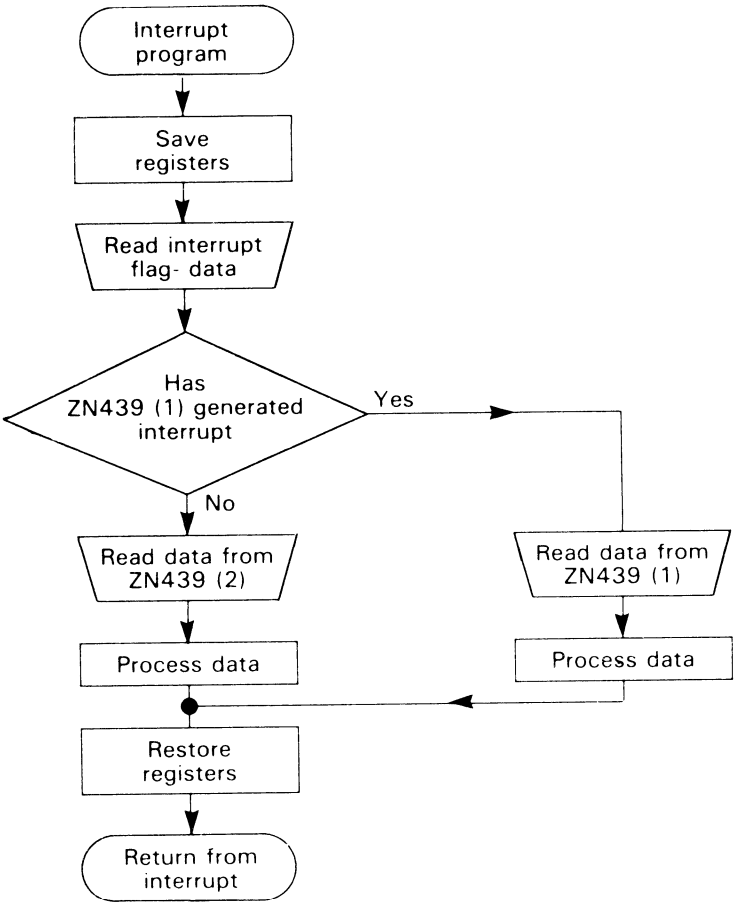

Interrupt program
Save registers
Read interrupt flag- data
Has ZN439 (1) generated interrupt
Yes
No
Read data from ZN439 (2)
Read data from ZN439 (1)
Process data
Process data
Restore registers
Return from interrupt

Fig. 6

Address	Object code	Label	Mnemonic	Operand	Comments
2000	48		PHA		
2001	8A		TXA		
2002	48		PHA		Save registers
2003	98		TYA		
2004	48		PHA		
2005	AD 00 12		LDA	1002	Read flag data
2008	4A		LSR	A	Has ZN439(1) generated the interrupt
2009	B0 08		BCS	AD2	
200B	AD 00 10		LDA	1000	Read ZN439(1) data
200E	85 80		STA	80	Process data
2010	4C 18 20		JMP	END	
2013	AD 00 11	AD2	LDA	1001	Read ZN439(2) data
2016	85 81		STA	81	Process data
2018	68	END	PLA		
2019	A8		TAY		
201A	68		PLA		Restore registers
201B	AA		TAX		
201C	68		PLA		
201D	40		RTI		Return

ADDRESS ALLOCATION

80 Memory location for storing ZN439(1) data.
81 Memory location for storing ZN439(2) data.
1000 ZN439(1).
1001 ZN439(2).
1002 Interrupt flags.
2000 Start address of program.

Note: All numbers are in Hex.

Fig. 7

Interfacing to the 4MHz CMOS 65C00 series

The high speed 4MHz 65C00 series have a maximum access time of 160nS. This access time must include both delay time through the address decoding and the enable time of the ZN439 data outputs. As the maximum enable time of the ZN439 is 160nS the device is too slow to interface directly to this microprocessor.

To overcome this problem the read cycle must be extended by use of the microprocessor RDY input. Fig. 8 shows a simple circuit using a JK flip-flop to stop the microprocesor for 1 clock period during a ZN439 read cycle. This is a standard procedure with high speed microprocessors. A timing diagram is shown in Fig. 9.

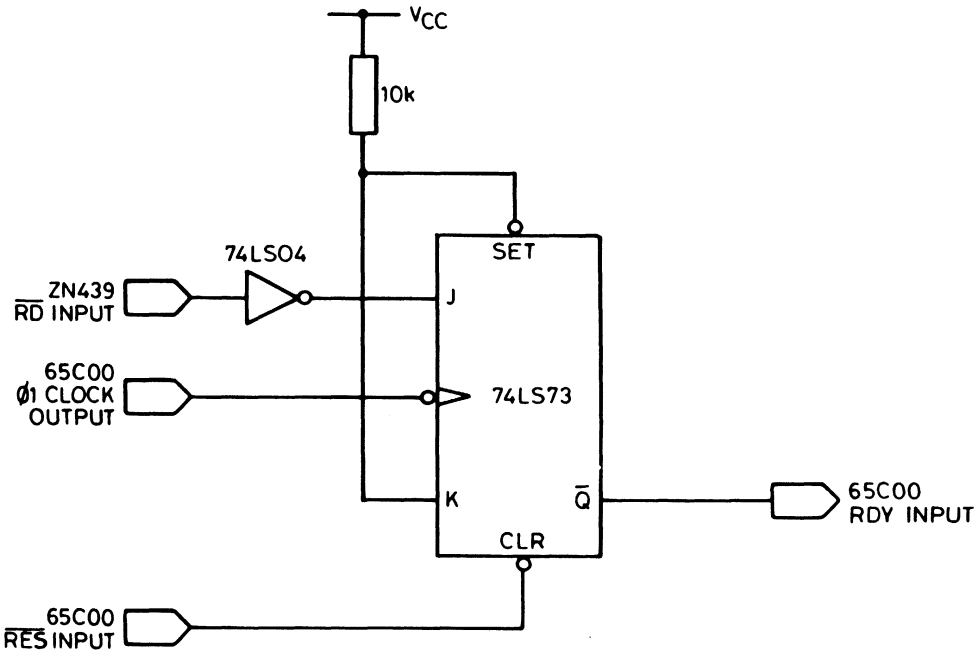


Fig. 8 Read cycle extender circuit

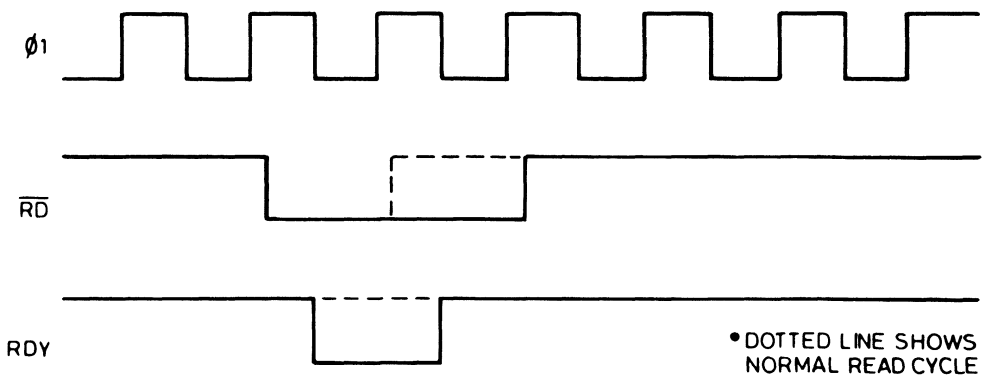


Fig. 9 Timing diagram

PORT INTERFACING

In some cases it may be necessary to interface the converter to an existing microcomputer system. In these cases the address space may already have been fully allocated and so the only interfacing possible will be via the system ports. The following section gives hardware and software details of the different techniques available for interfacing the ZN439 to the popular peripheral interface chip the 6522 VIA.

All the program examples assume the 6522 is in its reset state.

The 6522 versatile interface adaptor

The 6522 VIA is an NMOS I/O control device available in two speed options 1 and 2MHz. It contains two 8-bit bi-directional ports, each line of which can be programmed as either an input or an output. Associated with each port are two control lines. These lines can be programmed as either interrupt inputs or handshake outputs. In addition the device contains two 16-bit counter timers and a serial shift register. To facilitate control of the many features the VIA contains interrupt flag, interrupt enable, function control and auxiliary control registers.

To complement the CMOS microprocessors in the 6500 family the VIA is also available as a CMOS device the 65C22. This is available in four speed options 1, 2, 3 and 4MHz and is fully compatible with the NMOS device.

For further information please refer to the 6522 and 65C22 data sheets.

Direct port interfacing

(1) Single converter

The simplest method of interfacing a single converter to the 6522 is shown in Fig. 10. The data outputs of the ZN439 are connected to the port A data lines which are configured as inputs. As the $\overline{RD}$ input cannot be tied low it must be taken low before reading the converter data and returned high afterwards. This is achieved using the port A control line, CA2 programmed as an output. To read the data CA2 is taken low. The data is then read from the port A input register. Finally CA2 is taken high, allowing the ZN439 double buffered register to be updated after the next conversion. As only one port is required this circuit is equally applicable to port B using PB0-7 and CB2 instead of PA0-7 and CA2. A flow diagram and program showing the required initialisation and data read steps are shown in Figs. 11 and 12 respectively.

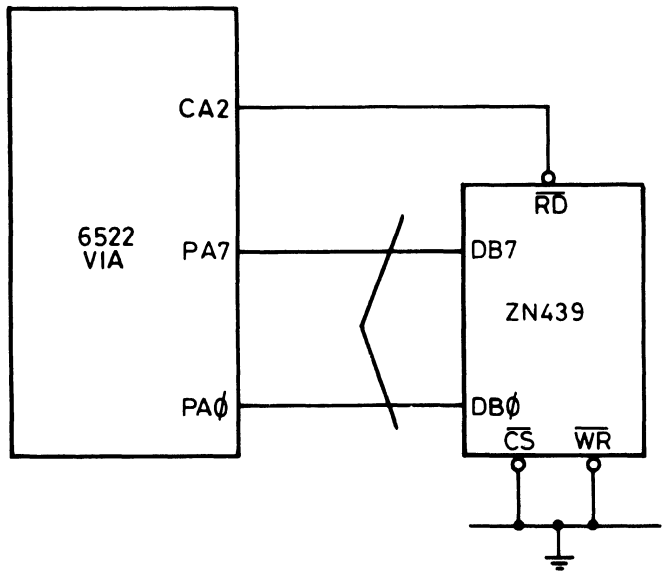


Fig. 10 Single converter - direct port interfacing

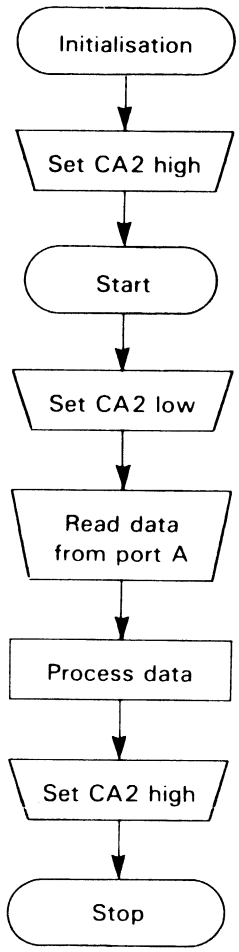

Initialisation
Set CA2 high
Start
Set CA2 low
Read data
from port A
Process data
Set CA2 high
Stop

Fig. 11

Address	Object code	Label	Mnemonic	Operand	Comments
2000	AD OC 50		LDA	500C	
2003	29 F1		AND	#F1	Sets CA2 high without affecting the other port control lines
2005	09 OE		ORA	#OE	
2007	8D OC 50		STA	500C	
3000	AD OC 50		LDA	500C	
3003	29 FD		AND	#FD	Sets CA2 low
3005	8D OC 50		STA	500C	
3008	AD O1 50		LDA	5001	Read ZN439 data
300B	85 80		STA	80	Process data
300D	AD OC 50		LDA	500C	
3010	09 02		ORA	#02	Sets CA2 high
3012	8D OC 50		STA	500C	

ADDRESS ALLOCATION

80 Memory address for storing ZN439 data.
2000 Start address of initialisation.
3000 Start address of ZN439 read program.
5001 VIA data register for port A.
500C VIA peripheral control register.

Fig. 12

(2) Multiple converters

For connecting more than one converter to a 6522 an extension of the single converter circuit is used. A circuit diagram is shown in Fig. 13. As before the port A inputs are connected to the data bit outputs of each converter. Port B is now used to provide the individual $\overline{RD}$ outputs to each converter. To read data from a ZN439 the appropriate bit output of port B is taken low. Data can then be read from the port A input register as before. Note, only one bit of port B should be taken low at a time. A flow diagram and program are shown in Figs. 14 and 15.

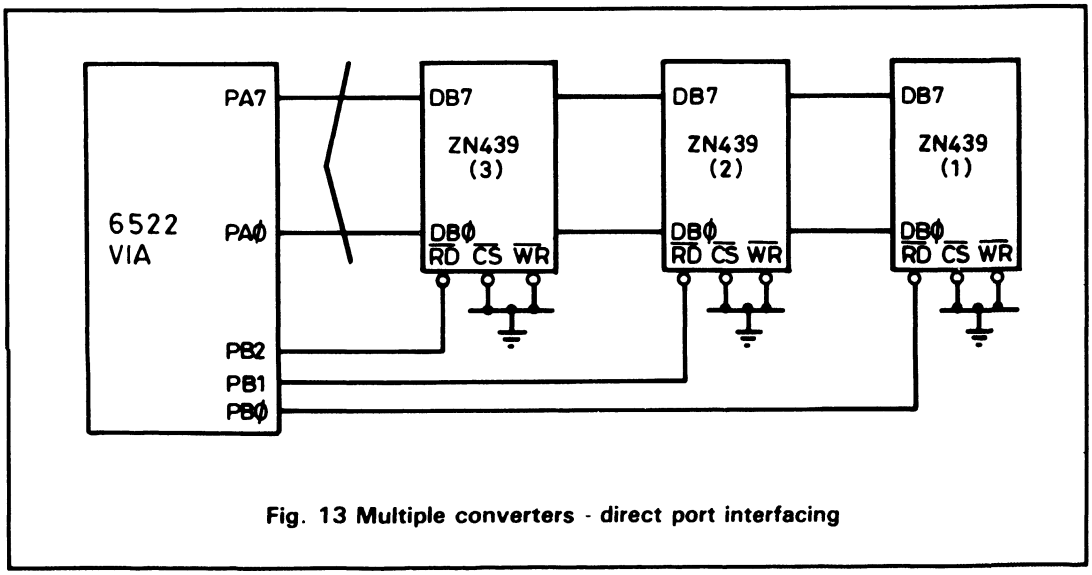


Fig. 13 Multiple converters - direct port interfacing

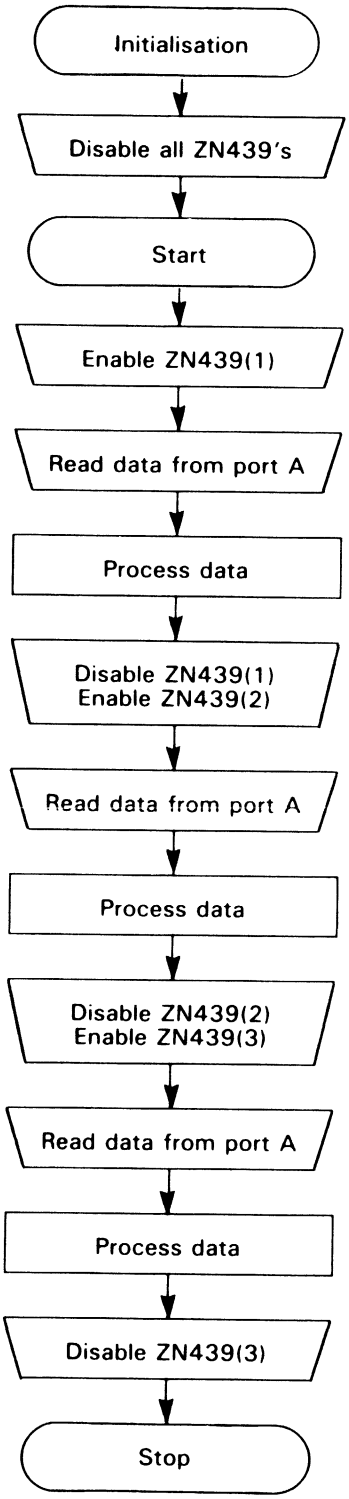

Initialisation
Disable all ZN439's
Start
Enable ZN439(1)
Read data from port A
Process data
Disable ZN439(1)
Enable ZN439(2)
Read data from port A
Process data
Disable ZN439(2)
Enable ZN439(3)
Read data from port A
Process data
Disable ZN439(3)
Stop

Fig. 14

Address	Object code	Label	Mnemonic	Operand	Comments
2000	A9 07		LDA	# 07	
2002	8D 00 50		STA	5000	Disable all ZN439's
2005	8D 02 50		STA	5002	
3000	A9 06		LDA	# 06	
3002	8D 00 50		STA	5000	Enable ZN439(1)
3005	AD 01 50		LDA	5001	Read data from ZN439(1)
3008	85 80		STA	80	Process data
300A	A9 05		LDA	# 05	Disable ZN439(1)
300C	8D 00 50		STA	5000	Enable ZN439(2)
300F	AD 01 50		LDA	5001	Read data from ZN439(2)
3012	85 81		STA	81	Process data
3014	A9 03		LDA	# 03	Disable ZN439(2)
3016	8D 00 50		STA	5000	Enable ZN439(3)
3019	AD 01 50		LDA	5001	Read data from ZN439(3)
301C	85 82		STA	82	Process data
301E	A9 07		LDA	# 07	Disable ZN439(3)
3020	8D 00 50		STA	5000	

ADDRESS ALLOCATION

80 Memory address for storing ZN439(1) data.
81 Memory address for storing ZN439(2) data.
82 Memory address for storing ZN439(3) data.
2000 Start address of initialisation.
3000 Start address of ZN439 read program.
5000 VIA data register for port B.
5001 VIA data register for port A.
5002 VIA data direction register for port B.

Fig. 15

Interrupt port interfacing

(1) Single converter

In some cases it may be advantageous to have the ZN439 interrupt driven. The ZN439 would signal to the VIA that new data was available. The VIA would then interrupt the microprocessor which would read and process the converted data. This is easily implemented using an extension of the direct port interfacing circuit of Fig. 10. By connecting the status output to the CA1 input, interrupt driven operation is made possible. A circuit diagram is illustrated in Fig. 16.

A start convert pulse is first applied to the $\overline{WR}$ input. At the end of conversion the status output goes low. This produces a negative transition on the CA1 interrupt input which sets the CA1 interrupt flag within the VIA. With the CA1 interrupt enable bit set the VIA will take the $\overline{IRQ}$ output low to generate a system interrupt. The microprocessor then responds by executing an interrupt service routine. This routine will involve reading the converter data from port A as described previously.

At this point it should be noted that a problem could arise during power up. After V_{CC} has reached 4.75V the status output will go low between 1 and 8 clock cycles later. If the RES input of the VIA is not held low for at least this time the negative transition on the status output will set the CA1 interrupt flag. Therefore once the CA1 interrupt enable bit is set an interrupt will be generated and the microprocessor will read erroneous data. To overcome this problem the CA1 interrupt flag sould be reset during initialisation before the interrupt enable bit is set.

A typical flow diagram and program are shown in Figs. 17 and 18.

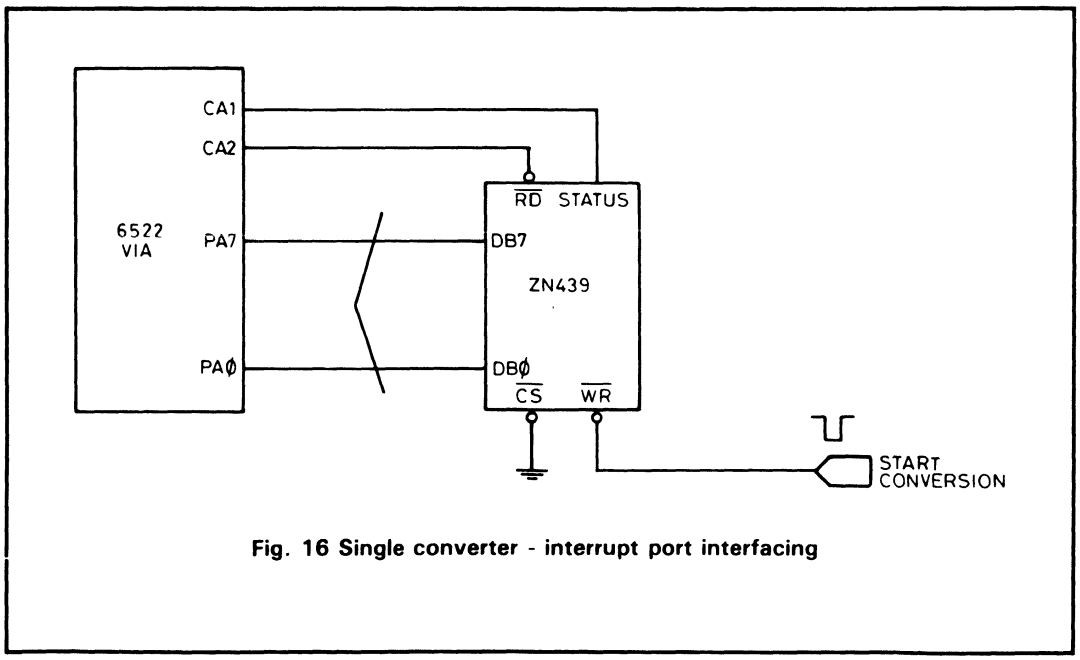


Fig. 16 Single converter - interrupt port interfacing

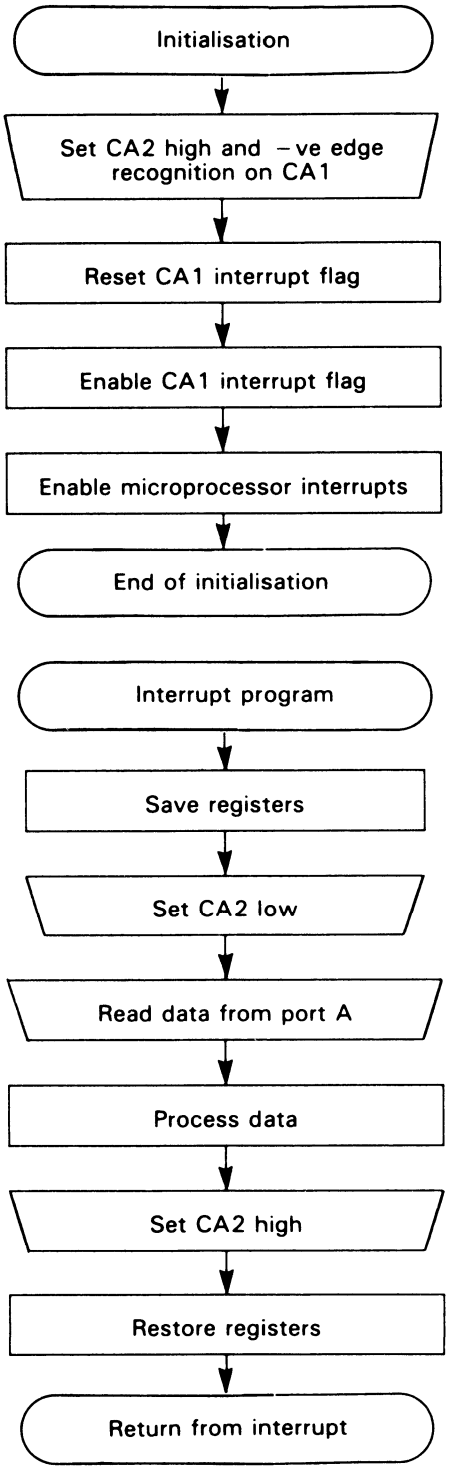

Initialisation
Set CA2 high and −ve edge recognition on CA1
Reset CA1 interrupt flag
Enable CA1 interrupt flag
Enable microprocessor interrupts
End of initialisation
Interrupt program
Save registers
Set CA2 low
Read data from port A
Process data
Set CA2 high
Restore registers
Return from interrupt

Fig. 17

Address	Object code	Label	Mnemonic	Operand	Comments
2000	AD OC 50		LDA	500C	Set CA2 high and negative edge recognition on CA1 without affecting the other port control lines
2003	29 FO		AND	#FO	
2005	09 OE		ORA	#OE	
2007	8D OC 50		STA	500C	
200A	A9 82		LDA	#82	Reset CA1 interrupt flag
200C	8D OD 50		STA	500D	
200F	8D OE 50		STA	500E	Enable CA1 interrupt flag
2012	58		CLI		Enable micro-processor interrupts
3000	48		PHA		Save registers
3001	8A		TXA		
3002	48		PHA		
3003	98		TYA		
3004	48		PHA		
3005	AD OC 50		LDA	500C	Set CA2 low
3008	29 FD		AND	#FD	
300A	8D OC 50		STA	500C	
300D	AD 01 50		LDA	5001	Read data from ZN439
3010	85 80		STA	80	Process data
3012	AD OC 50		LDA	500C	Set CA2 high
3015	09 02		ORA	#02	
3017	8D OC 50		STA	500C	
301A	68		PLA		Restore registers
301B	A8		TAY		
301C	68		PLA		
301D	AA		TAX		
301E	68		PLA		
301F	40		RTI		Return

ADDRESS ALLOCATION

80 Memory address for storing ZN439 data.
2000 Start address of initialisation.
3000 Start address of interrupt program.
5001 VIA data register for port A.
500C VIA peripheral control register
500D VIA interrupt flag register.
500E VIA interrupt enable register.

Fig. 18

(2) Multiple converters

To interface more than two converters to the VIA two problems have to be overcome.

Firstly there is the problem of generating the interrupt. The standard procedure would be to wire-OR the status outputs together and use this common output to generate the interrupt. This is achieved by connecting the common wire-OR output to the VIA interrupt input CA1.

The second problem is determining which device has generated the interrupt. This is overcome by using the status output of each device as an interrupt flag and connecting each bit to an input bit of port B. By examining the state of these flags the microprocessor can ascertain which device has requested an interrupt.

A circuit diagram detailing the connections required to interface three devices to the VIA is shown in Fig. 19. Port B is configured such that bits 0, 1 and 2 are outputs and bits 5, 6 and 7 are inputs. As in the single converter case an external start convert pulse is applied to the $\overline{WR}$ input of one of the devices. At the end of the conversion the status output goes low which sets the CA1 interrupt flag within the VIA. With the CA1 interrupt enable bit set the VIA will then interrupt the microprocessor. By reading the data on port B and examining bits 5, 6 and 7 the microprocessor can determine which device is responsible for the interrupt. The interrupting converter can then be enabled by taking bit 0, 1 or 2 low. The converter data can then be read from port A. The action of reading the data also clears the interrupt flag within the VIA which removes the interrupt. Finally the appropriate bit of port B is taken high to disable the output buffer of the ZN439 and allow update at the end of the next conversion.

It should be noted that as CA1 is an edge triggered input a second interrupt occuring soon after a first will not be recognised by the VIA. Therefore after servicing one interrupt and before returning from the service routine the interrupt flag data on port B must be examined again. This will ensure that no interrupts are missed. A flow diagram and program are shown in Figs. 20 and 21.

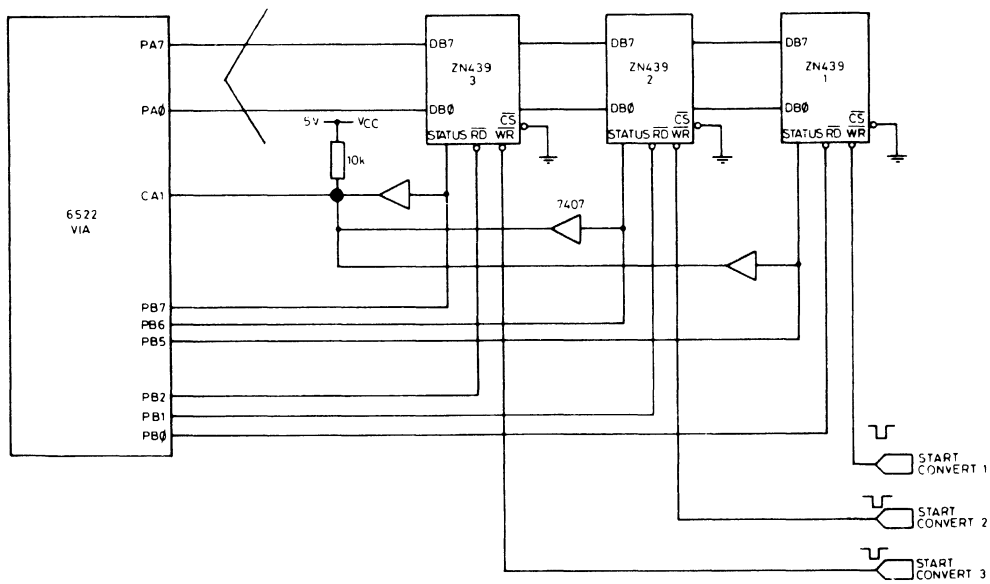
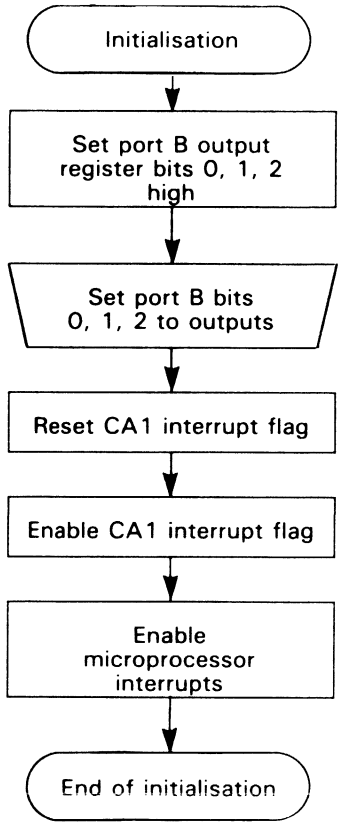
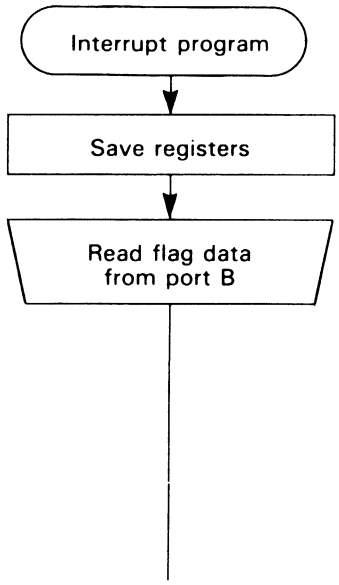


Fig. 19 Multiple converters - interrupt port interfacing


Initialisation
Set port B output register bits 0, 1, 2 high
Set port B bits 0, 1, 2 to outputs
Reset CA1 interrupt flag
Enable CA1 interrupt flag
Enable microprocessor interrupts
End of initialisation


Interrupt program
Save registers
Read flag data from port B

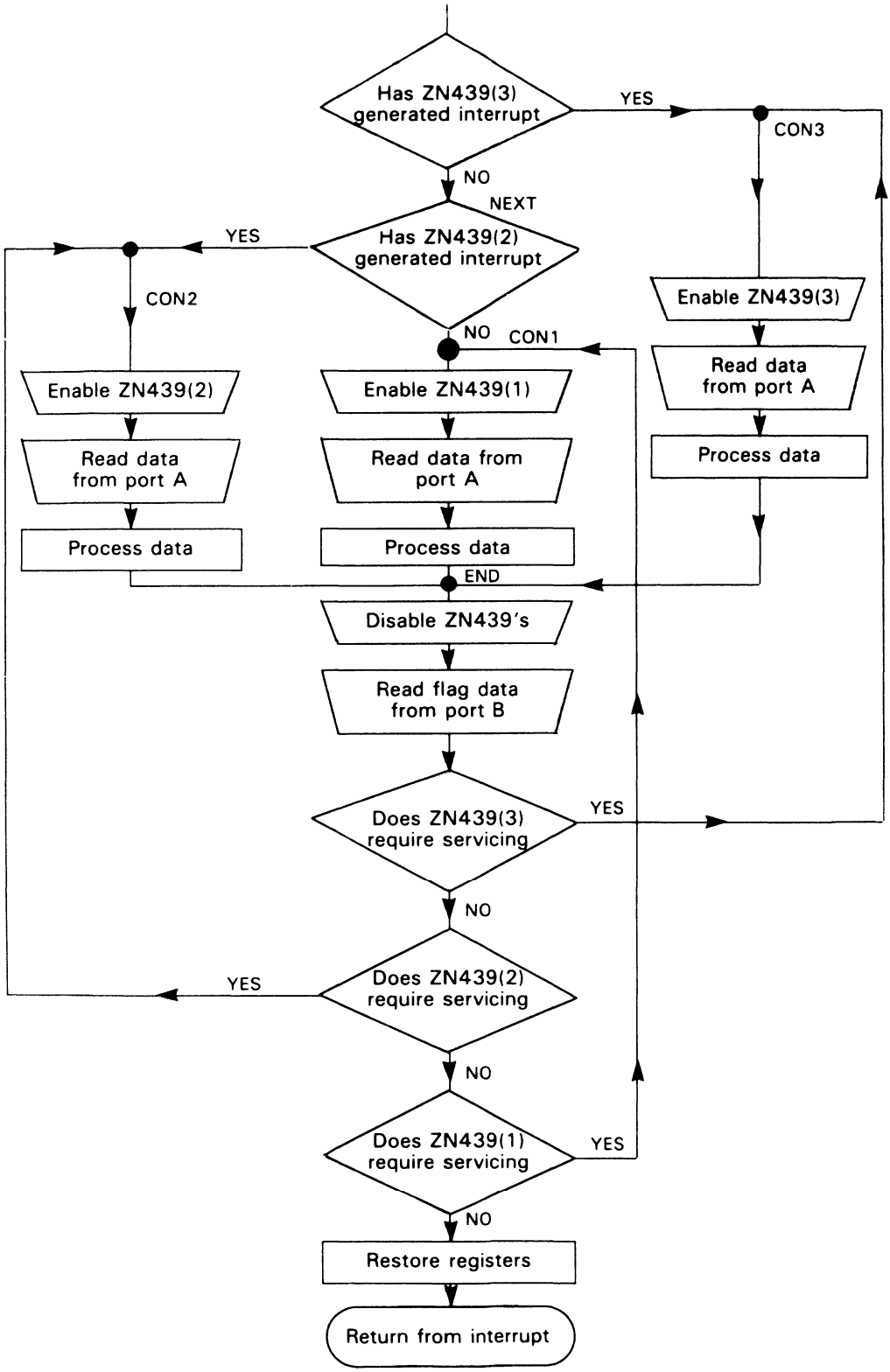

Has ZN439(3) generated interrupt
YES
CON3
NO
NEXT
Has ZN439(2) generated interrupt
YES
CON2
NO
CON1
Enable ZN439(3)
Read data from port A
Process data
Enable ZN439(2)
Read data from port A
Process data
Enable ZN439(1)
Read data from port A
Process data
END
Disable ZN439's
Read flag data from port B
Does ZN439(3) require servicing
YES
NO
Does ZN439(2) require servicing
YES
NO
Does ZN439(1) require servicing
YES
NO
Restore registers
Return from interrupt

Fig. 20

Address	Object code	Label	Mnemonic	Operand	Comments
2000	A9 07		LDA	#07	Set port B output register bits 0, 1 and 2 high
2002	8D 00 50		STA	5000	
2005	8D 02 50		STA	5002	Set port B bits 0, 1 and 2 to outputs
2008	A9 82		LDA	#82	Reset CA1 interrupt flag
200A	8D OD 50		STA	500D	
200D	8D OE 50		STA	500E	Enable CA1 interrupt flag
2010	58		CLI		Enable micro-processor interrupts
3000	48		PHA		Save registers
3001	8A		TXA		
3002	48		PHA		
3003	98		TYA		
3004	48		PHA		
3005	AD OO 50		LDA	5000	Load flag data
3008	OA		ASL	A	Has ZN439(3) generated the interrupt
3009	BO OD		BCS	NEXT	
300B	A9 03	CON3	LDA	#03	Enable ZN439(3)
300D	8D 00 50		STA	5000	
3010	AD 01 50		LDA	5001	Read data from ZN439(3)
3013	85 82		STA	82	Process data
3015	4C 37 30		JMP	END	
3018	OA	NEXT	ASL	A	Has ZN439(2) generated the interrupt
3019	BO OD		BCS	CON1	
301B	A9 05	CON2	LDA	#05	Enable ZN439(2)
301D	8D 00 50		STA	5000	
3020	AD 01 50		LDA	5001	Read data from ZN439(2)
3023	85 82		STA	81	Process data
3025	4C 37 30		JMP	END	
3028	A9 06	CON1	LDA	#06	Enable ZN439(1)
302A	8D 00 50		STA	5000	
302D	AD 01 50		LDA	5001	Read data from ZN439(1)
3030	85 80		STA	80	Process data
3032	A9 07		LDA	#07	Disable all ZN439's
3034	8D 00 50		STA	5000	

Fig. 21

Address	Object code	Label	Mnemonic	Operand	Comments
3037	AD 00 50	END	LDA	5000	Load flag data
303A	OA		ASL	A	Does ZN439(3) need servicing
303B	90 CE		BCC	CON3	
303D	OA		ASL	A	Does ZN439(2) need servicing
303E	90 DC		BCC	CON2	
3040	OA		ASL	A	Does ZN439(1) need servicing
3041	90 E5		BCC	CON1	
3043	68		PLA		Restore registers
3044	A8		TAY		
3045	68		PLA		
3046	AA		TAX		
3047	68		PLA		
3048	40		RTI		Return

ADDRESS ALLOCATION

80 Memory address for storing ZN439(1) data.
81 Memory address for storing ZN439(2) data.
82 Memory address for storing ZN439(3) data.
2000 Start address of initialisation.
3000 Start address of interrupt program.
5000 VIA data register for port B.
5001 VIA data register for port A.
5002 VIA data direction register for port B.
500D VIA interrupt flag register.
500E VIA interrupt enable register.

Fig. 21 (cont.)

CONCLUSIONS

The examples given in this report should demonstrate the minimal hardware and simple software required to interface the ZN439 to the 6500 series of microprocessors. A wide variety of configurations have been given to allow the designer maximum flexibility in choosing an option best suited to his application.

All the programs given show the start address at location 2000 with the VIA starting at location 5000. These are purely arbitrary and will undoubtedly reside at different locations within the designers system. All the programs are directly relocatable except the last program of Fig. 21 which includes two absolute jumps whose operands will require changing.

In the flow diagrams there is a box labelled 'process data'. This translates in the program to storing the ZN439 data in a memory location. In reality this will be replaced by more complex data processing. For completeness the X and Y registers are saved and restored during the interrupt service routine, despite not being used in the program. This is because the more complex processing required by the designer will probably include the use of the X and Y registers.

It has been assumed throughout that the ZN439's will be the only interrupting devices in the system. If this is not the case then some form of polling will be required to determine what has generated the interrupt. With port interfacing this is easily achieved by examining the VIA interrupt flag register. In the case of direct bus interfacing the interrupt flag provided by the buffered status output (Fig. 5) can be examined.

Despite this report being written for the 6500 family the principles involved are valid for other microprocessors. It is therefore hoped that the techniques presented here will prove valuable to designers interfacing the ZN439 to other popular microprocessors.

Interfacing the ZN447/8/9 A-D Converters to the Z80μP via a Z80 PIO

This report illustrates how to interface one or more Plessey ZN447/8/9 A-D converters to a Z80 based microprocessor system using a Z80 PIO. Circuit diagrams and program examples are given to enable the user to get his interface system working. The following is also applicable to the faster versions of the Z80μP and the Z80 PIO and also to the CMOS versions. Most of the principles described can also be applied when interfacing the ZN447/8/9 to other popular μPs.

In order to keep this report concise it is assumed that the reader is familiar with the Z80 system.

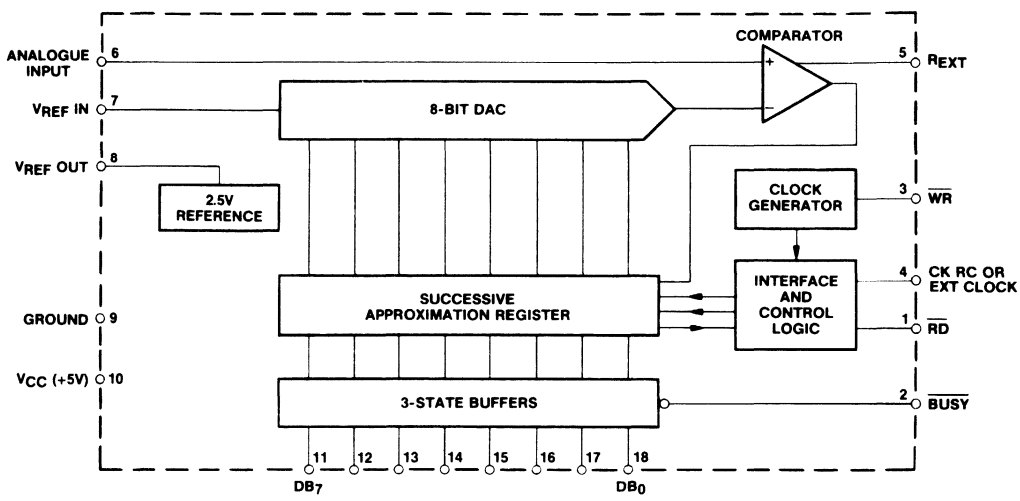


Fig. 1 ZN447/8/9 system diagram

TNE ZN447/8/9 A-D CONVERTER

The ZN447/8/9 are 8-bit successive approximation A-D converters with linearity errors of ± ¼, ±½ and 1 LSB respectively.

Hereafter any description relating to one of these devices is equally applicable to the other two types.

All active circuitry is contained on-chip including three-state output buffers, 2.5V bandgap reference and a clock generator.

They are each capable of converting unipolar or bipolar input voltages with the only external components required for operation being a reference resistor and capacitor, clock capacitor, resistor to the negative supply and the analogue input scaling resistor(s) (to accommodate the different input voltages).

A conversion is initiated by taking the $\overline{WR}$ input low and then high. The conversion then takes between 7½ and 8½ clock cycles after the $\overline{WR}$ positive edge. The $\overline{WR}$ input signal may be completely asynchronous to the chip clock. The falling edge of the $\overline{WR}$ signal sets the MSB high and the remaining bits low. This edge also sets the $\overline{BUSY}$ output low. Once started the converter cycles through a successive approximation routine to arrive at a result (see data sheet for explanation). When the conversion is finished, the $\overline{BUSY}$ output goes high indicating that valid data may now be read. A low at the $\overline{RD}$ input enables the data outputs and a high puts them into the high impedance state.

The devices will operate correctly with clock frequencies up to at least 900kHz. At 900kHz the conversion time is less than 9.5μs. (in fact the devices will typically operate above 900kHz but some loss in accuracy may result).

The negative supply requirement is minimal (e.g. 75μA) and can easily be supplied from a simple diode pump circuit.

Further information including the input resistors required for various unipolar and bipolar input voltages and examples of diode pump circuits, can be obtained from the data sheet.

Z80 PIO

The Z80 PIO is a programmable two port device which provides a TTL compatible interface between peripheral devices and the Z80 CPU. It is capable of interfacing directly to the CPU without any external logic. The two 8-bit, bidirectional ports, each have two handshake lines (RDY and $\overline{STB}$) for use when transferring data to or from peripherals. Either port or indeed any port bit, can be programmed to act as an input or output.

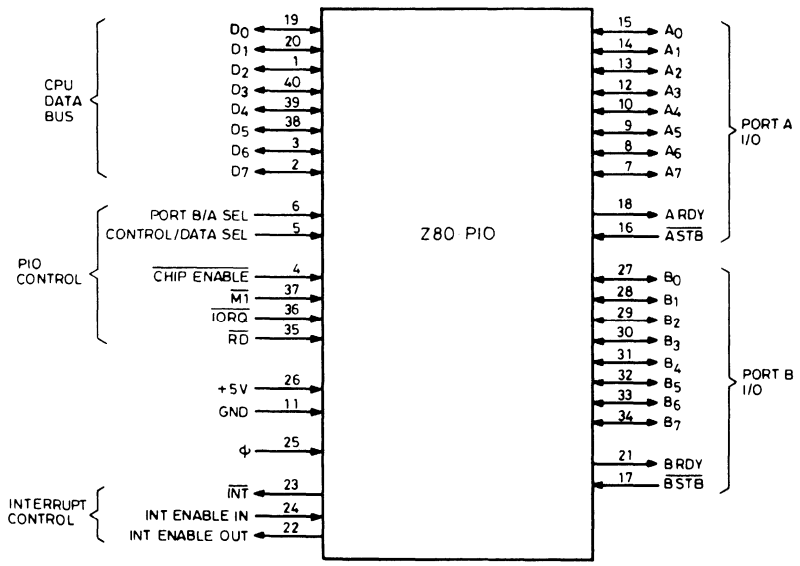


Fig. 2 Z80 PIO

The PIO has 4 operating modes:

Mode 0 (Output mode) - All port bits are set to outputs.

Mode 1 (Input mode) - All port bits are set to inputs.

Mode 2 (Bidirectional mode) - Used for bidirectional data transfer - not considered in this report.

Mode 3 (Control mode) - Each bit can be programmed individually to act as an input or output. Useful for status and control applications.

We will utilise mode 1 for reading the result of the A-D conversion. With mode 3 we can configure some of the port bits as outputs, taking them low and high as desired (can be used for controlling the $\overline{RD}$ and $\overline{WR}$ input on the converters) and we can configure some of the port bits as inputs (for monitoring the $\overline{BUSY}$ outputs). If the $\overline{BUSY}$ outputs are not being monitored and the port bits are being used as outputs, mode 0 could instead be used for controlling the $\overline{RD}$ and $\overline{WR}$ inputs.

In the input mode, the $\overline{STB}$ input needs to be low to allow data into the port. A positive edge on the $\overline{STB}$ latches data into the port, causes RDY to go low and generates an interrupt if enabled. During a port read the RDY line will be forced low, if not already low, and then high.

This is a brief introduction to a complex device. Further information can be obtained from the manufacturers data sheets.

INTERFACING A SINGLE ZN447/8/9 TO THE Z80 USING A SINGLE PORT

If it is required to interface only one ZN448 to the Z80 system, this can be achieved using only a single port (½PIO). Here the $\overline{RD}$ input on the ZN448 is tied low and hence the data outputs are permanently enabled.

A conversion can be started with a $\overline{WR}$ pulse derived from the RDY signal or from some other logic. Valid data can then be read when the conversion is finished. In order to ensure this, either a program delay can be used (i) below) or the $\overline{BUSY}$ output can be used to generate an interrupt via the port $\overline{STB}$ input ((ii) below).

(i) Data acquisition using a program delay

Here a dummy read is issued to the port to generate a positive transition on the RDY output. This edge then triggers a monostable which in turn supplies a $\overline{WR}$ pulse to the ZN448. This initiates a conversion. The program then cycles through a delay routine to give the conversion time to finish. After this a genuine read is issued to the port and the data then processed as required.

The circuit diagram is as follows:

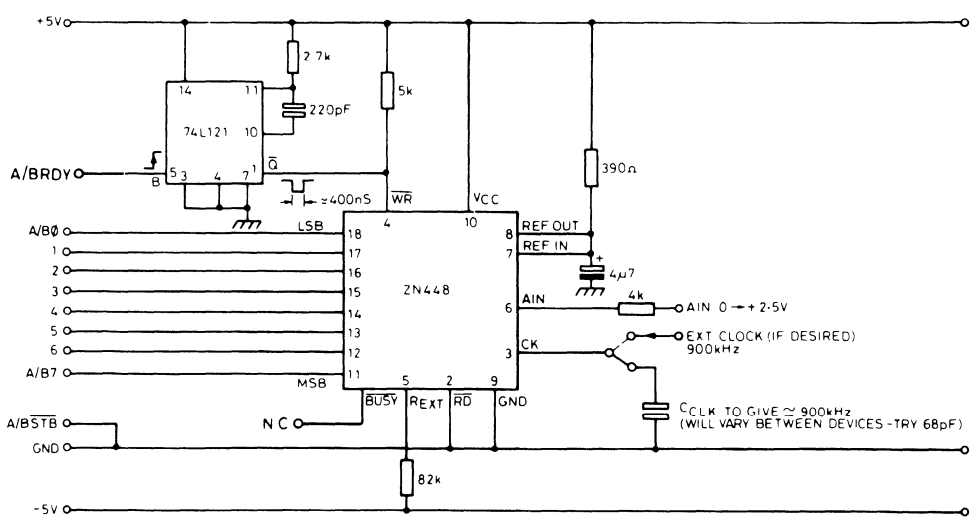


Fig. 3 Interfacing a single ZN448 to a single port - program controlled

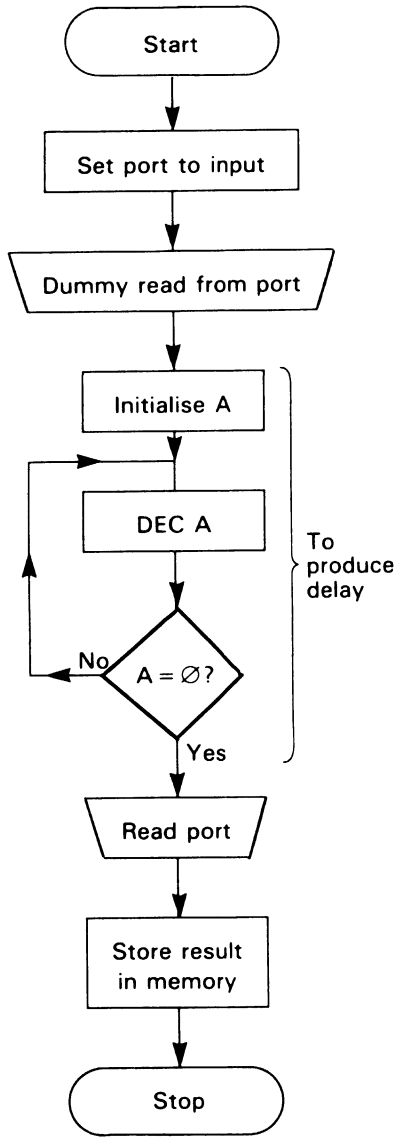
PROGRAM EXAMPLE

This is a program to start a conversion, cycle through a delay routine (until conversion has finished) and then read the result. This data is then stored in memory.

PROGRAM STATEMENT

: Nominate memory location for storing the conversion results:
: Decide on delay required (see comments for suggestions).
: It is assumed that the port needs initialising.

FLOWCHART 1



PROGRAM LISTING

PROGRAM 1

Address	Object code	Label	Source code	Comments
NN00	3E 4F		LD A,4FH	Sets port to input (Mode 1)
NN02	D3 PORTCO		OUT PORTCO,A	
NN04	DB PORTDA		IN A,PORTDA	Dummy read from port
NN06	3E DELAY		LD A,DELAY	Initialises A for delay
NN08	3D	(1)	DEC A	Delay routine
NN09	20 FD		JR NZ, (1)	
NN0B	DB PORTDA		IN A,PORTDA	Reads result of conversion
NN0D	32 MEM		LD (MEM),A	Stores result
NN10	?		?	Returns to monitor program (Command(s) system dependant)

KEY:

NN00 = Any Suitable starting address.
PORTCO = Port control address.
PORTDA = Port data address.
DELAY = Initialisation byte for delay (see comments).
MEM = 16-bit memory location nominated for storing data. (Needs assembling in the order Lo-byte, Hi-byte in the object code).

COMMENTS

The delay required depends on processor speed and the ZN448 clock frequency. With the ZN448 clock frequency at 900kHz, try working down from DELAY = 06H. For slower clocks the delay may need increasing accordingly.

When the processor reads the result of the conversion from the port, a further conversion is automatically initiated. This is of no consequence during normal operation. However if the data is being inspected manually for evaluation purposes, the data can appear incorrect at the first glance. This is because the valid data on the ZN448 outputs is one conversion behind the data read into the processor. Hence if the analogue input voltage is on the edge of a code transition, any noise present could possibly cause the result in memory and the data on the ZN448 outputs to differ slightly. If desired this can be overcome by examining the ZN448 outputs just before the conversion result is read (e.g. insert a break in the program), and then acquire the data for subsequent comparison.

The above arrangement is useful when there is only one spare port and it can be dedicated to this purpose.

(ii) Data acquisition under interrupt control

Interrupts are useful when interfacing to slow peripherals. However the ZN448 is not itself a slow peripheral as it can be operated to give a conversion time of less than 10μs. Hence it does not need to be interrupt driven.

However it may be required to call on the ZN448 relatively infrequently - as governed by some timing logic (e.g. a counter timer chip):

(a) this timing logic could vector to a subroutine which then starts a conversion and reads the result. In this case the subroutine might as well incorporate a delay - this has been covered in the previous section.

(b) alternatively this timing logic could initiate a conversion directly or, for example, via a monostable. This effectively makes the ZN448 appear slower and now makes interrupts more useful.

The second situation (b) above is now considered in this section. It is left to the user to configure this "timing logic" to best suit his particular requirements.

Remember that $\overline{\text{BUSY}}$ goes high to signal the end of conversion and also that the port $\overline{\text{STB}}$ input responds to positive transitions. Thus when $\overline{\text{BUSY}}$ is connected to $\overline{\text{STB}}$ and interrupts are enabled, an interrupt will be generated when $\overline{\text{BUSY}}$/$\overline{\text{STB}}$ goes high. This would then summon a service routine to read the result of the conversion.

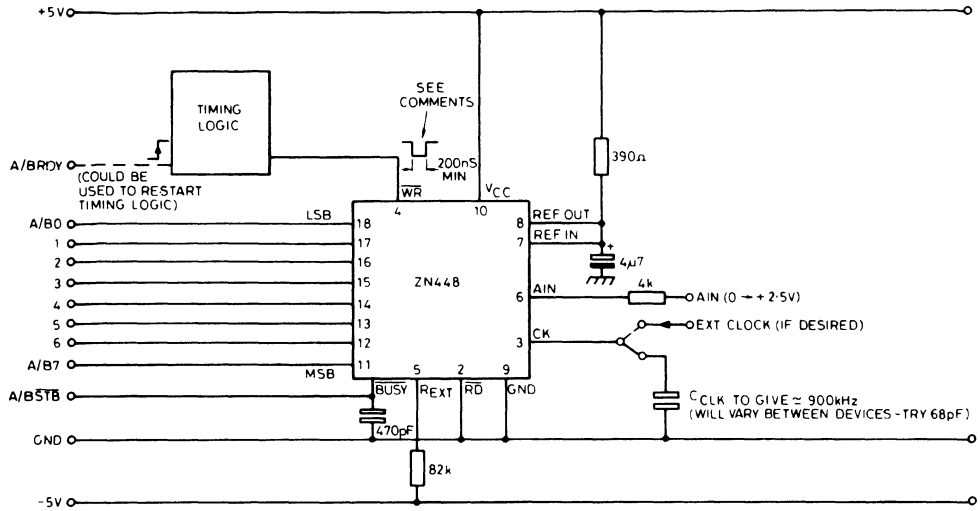


Fig. 4 Interfacing a single ZN448 to a single port - interrupt driven

The capacitor on the $\overline{\text{BUSY}}$ O/P is to meet the port data to $\overline{\text{STB}}$ rising edge set up time.

PROGRAM EXAMPLE

Here, when an interrupt is generated via $\overline{\text{BUSY}}$, the μP is vectored to the service routine which then reads and stores the result of the conversion, the conversion having been previously initiated by the timing logic.

The μP is set to interrupt mode 2, as the ports are designed to be used in this mode. The contents of the I register and the port interrupt vector are combined by the μP to form a 16-bit vector. This is then used to look up the starting address of the interrupt service routine. The μP then loads the program counter with this address and continues program execution from this location.

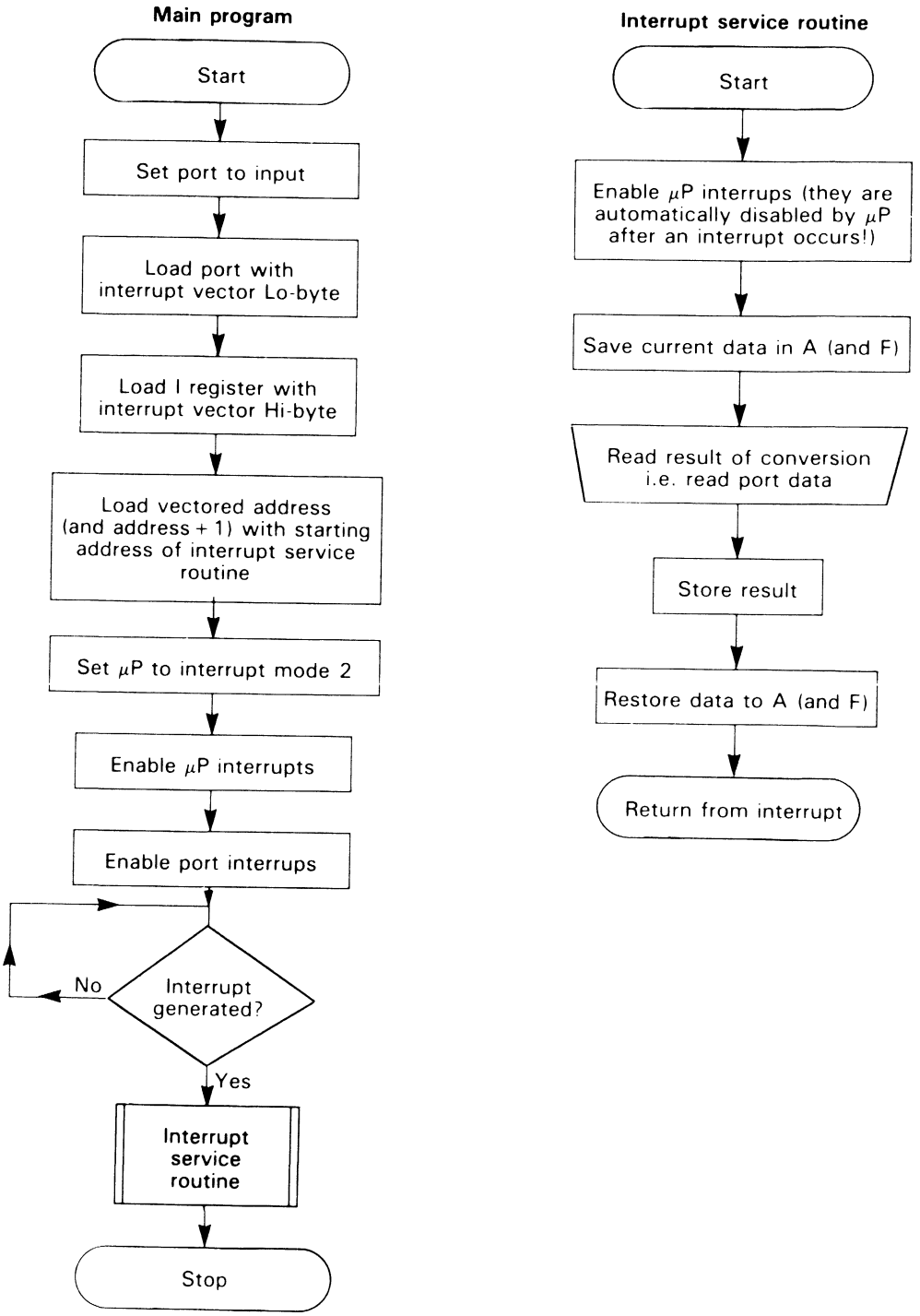
PROGRAM STATEMENTS

: Nominate memory locations for the vectored address, the interrupt service routine and for storing the conversion result.

: It is assumed that the user initiates conversion correctly when required.

: It is assumed that the port needs initialising:

FLOWCHART 2


Main program
Start
Set port to input
Load port with interrupt vector Lo-byte
Load I register with interrupt vector Hi-byte
Load vectored address (and address + 1) with starting address of interrupt service routine
Set μP to interrupt mode 2
Enable μP interrupts
Enable port interrupts
No
Interrupt generated?
Yes
Interrupt service routine
Stop
Interrupt service routine
Start
Enable μP interrupts (they are automatically disabled by μP after an interrupt occurs!)
Save current data in A (and F)
Read result of conversion i.e. read port data
Store result
Restore data to A (and F)
Return from interrupt

PROGRAM LISTING

PROGRAM 2

Address	Object code	Label	Source code	Comments
NN00	3E 4F		LD A,4FH	Sets port to input (Mode 1)
NN02	D3 PORTCO		OUT PORTCO,A	
NN04	3E IVECL		LD A,IVECL	Loads port with interrupt vector Lo-byte
NN06	D3 PORTCO		OUT PORTCO,A	
NN08	3E IVECH		LD A,IVECH	Loads I register with interrupt vector Hi-byte
NN0A	ED 47		LD I,A	
NN0C	3E SERVL		LD A,SERVL	Loads vectored address (and consecutive address) with starting address of interrupt service routine
NN0E	32 IVEC		LD (IVEC),A	
NN11	3E SERVH		LD A,SERVH	
NN13	32 IVEC + 1		LD (IVEC + 1),A	
NN16	ED 5E		IM 2	Sets μP to Interrupt mode 2
NN18	FB		EI	Enables μP interrupts
NN19	3E 83		LD A,83H	Enables port interrupts
NN1B	D3 PORTCO		OUT PORTCO,A	
NN1D	76		HALT	Waits for interrupt (or reset!)
NN1E	?		?	Returns to monitor (command(s) system dependant)

INTERRUPT SERVICE ROUTINE

Address	Object code	Label	Source code	Comments
MM00	FB		EI	Re-enables μP interrupts
MM01	F5		PUSH AF	Stores current values of AF
MM02	DB PORTDA		IN A,PORTDA	Reads result of conversion
MM04	32 MEM		LD(MEM),A	Stores result in memory
MM07	F1		POP AF	Restores AF values
MM08	ED 4D		RETI	Returns from interrupt

KEY:

NN00 = Any Suitable starting address.
PORTCO = Port control address.
PORTDA = Port data address.
IVECL = Low-byte of 16-bit interrupt vector (in port).
IVECH = High-byte of 16-bit interrupt vector (in I register).
IVEC = 16-bit interrupt vector formed by IVECH and IVECL.
IVEC + 1 = 16-bit address one location higher up in memory than IVEC.
SERVL = Interrupt service routine starting address-low byte.
SERVH = Interrupt service routine starting address-high byte.
MM00 = 16-bit starting address for interrupt service routine formed by SERVH and SERVL.
MEM = 16-bit address nominated for storing conversion results.
(Remember that the above 16-bit addresses need to be assembled in the order Lo-byte, Hi-byte in the object code).

COMMENTS

Remember that the $\overline{WR}$ falling edge sets the MSB high and all the other bits low. Hence the μP must latch the conversion result before any further $\overline{WR}$ falling edges are generated - otherwise incorrect data could be latched! This arrangement is useful when acquiring data relatively infrequently, under the control of some external logic, and/or when the ZN448 is operated with a slow clock.

For evaluation purposes, a single-shot debounced $\overline{WR}$ pulse may be supplied. Data can then be examined for integrity.

INTERFACING ONE OR MORE ZN447/8/9's TO THE Z80.

When it is required to connect more than a single ZN448 to a port, some control must be exerted over the three-state outputs. This is easily achieved by connecting the $\overline{RD}$ inputs to the bit outputs from another port. The relevant port bits and thus the $\overline{RD}$ inputs, can then be taken low individually, to enable only the desired device.

Further, this controlling port can do other useful things for us, such as generating $\overline{WR}$ pulses (by taking the relevant port bit(s) low and back high) and checking for the end of a conversion by monitoring the $\overline{BUSY}$ output(s).

Setting some of the port bits as inputs and some as outputs takes advantage of the control mode (mode 3) of the port.

The enable/disable times of the converter outputs need not be considered, since they are much less than the Z80 instruction execution times.

DATA ACQUISITION UNDER PROGRAM CONTROL

Here one port is assigned to reading the data from the ZN448's and another port used to control the $\overline{RD}$ and $\overline{WR}$ inputs and to monitor the $\overline{BUSY}$ outputs.

As an example consider interfacing 2 × ZN448's as follows:

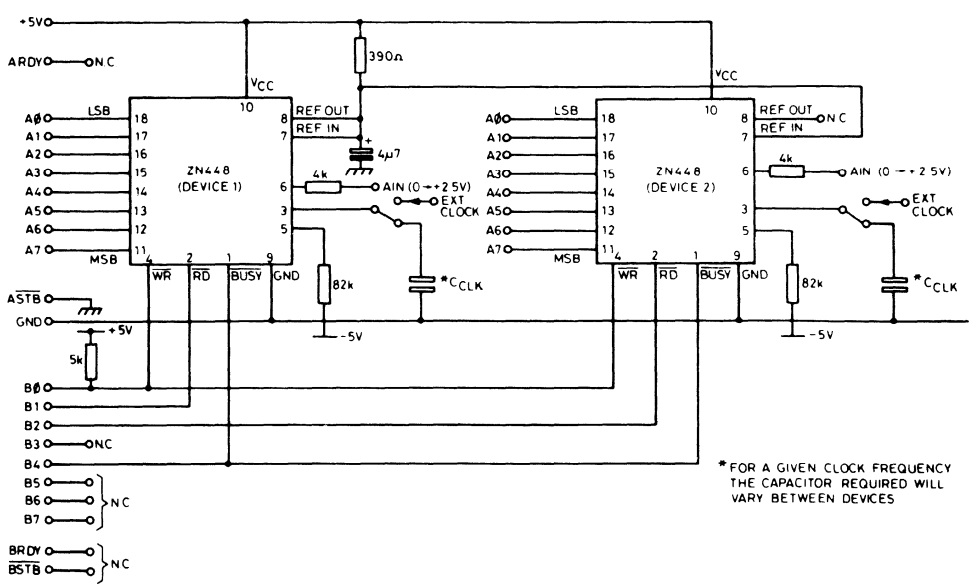


Fig. 5 Interfacing 2 × ZN448's to the Z80 using both ports of a Z80 PIO - $\overline{BUSY}$'s polled

Note that in the circuit of Fig. 5, the reference input ($V_{REF\ IN}$) of the second ZN448 is driven from the reference output ($V_{REF\ OUT}$) of the first ZN448. This provides excellent gain tracking between converters. Up to five ZN448's may be driven from a single internal reference without changing the reference resistor.

PROGRAM EXAMPLE

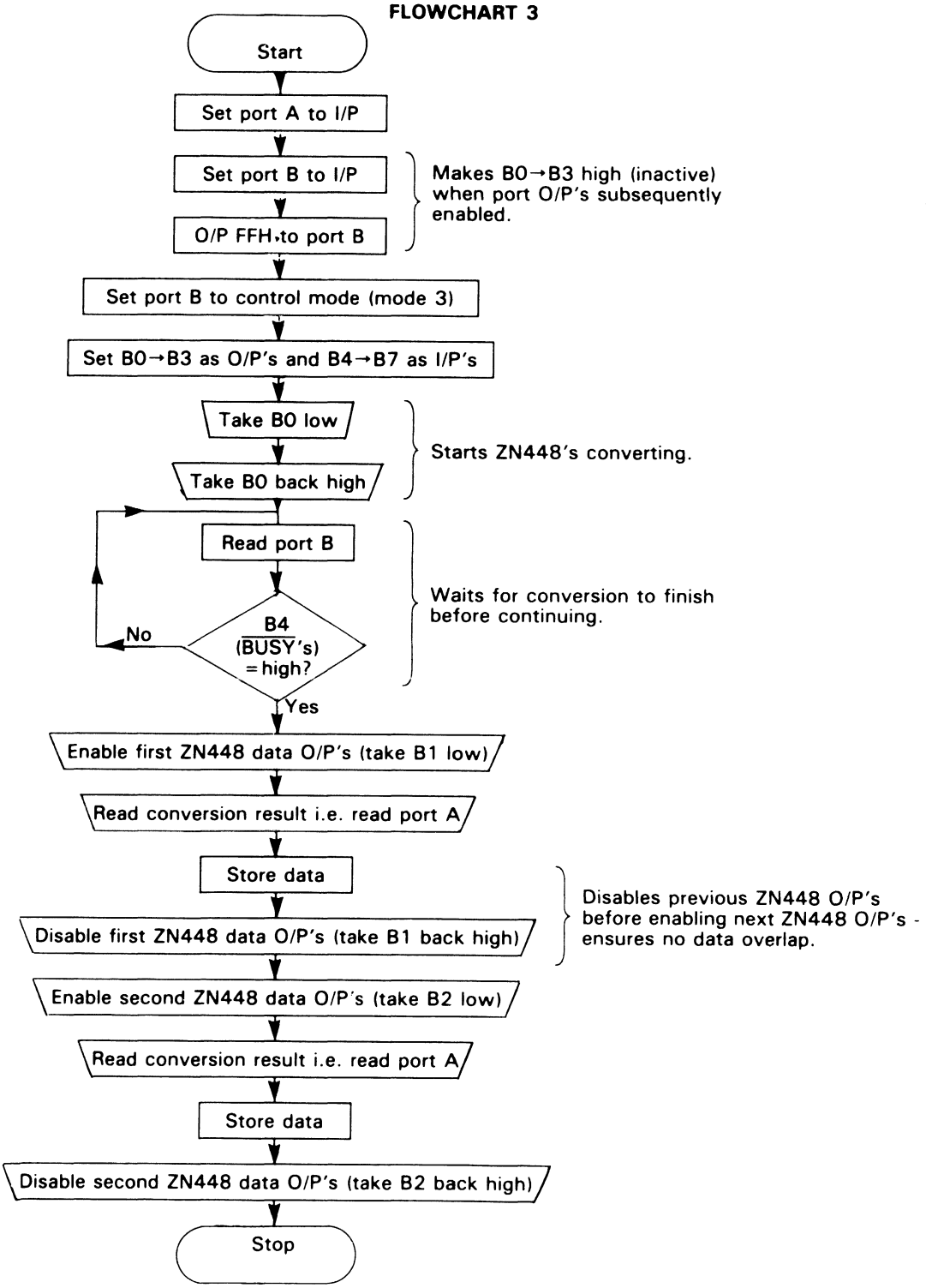
Here is a program to start the two ZN448's converting, then read and store the data when they have finished the conversion.

Conversion is initiated by taking B0 (= both $\overline{WR}$ inputs) low and then high. B4 (= both $\overline{BUSY}$'s) is then polled until it is found to be high, thus indicating that both ZN448's have finished converting. Each device is then brought out of the three-state condition in turn - by taking B1 and B2 (= both $\overline{RD}$ inputs) low individually - to allow the data to be read.

PROGRAM STATEMENTS

```
: Nominate memory locations for storing the
  conversion results.
: It is assumed that both ports need initialising.
: FEH = Take WR low word.
: FDH = Select first ZN448 word.
: FBH = Select second ZN448 word.
```

FLOWCHART 3


Start
Set port A to I/P
Set port B to I/P
O/P FFH to port B
Makes B0→B3 high (inactive) when port O/P's subsequently enabled.
Set port B to control mode (mode 3)
Set B0→B3 as O/P's and B4→B7 as I/P's
Take B0 low
Take B0 back high
Starts ZN448's converting.
Read port B
B4 (BUSY's) = high?
No
Yes
Waits for conversion to finish before continuing.
Enable first ZN448 data O/P's (take B1 low)
Read conversion result i.e. read port A
Store data
Disable first ZN448 data O/P's (take B1 back high)
Disables previous ZN448 O/P's before enabling next ZN448 O/P's - ensures no data overlap.
Enable second ZN448 data O/P's (take B2 low)
Read conversion result i.e. read port A
Store data
Disable second ZN448 data O/P's (take B2 back high)
Stop

PROGRAM LISTING

PROGRAM 3

Address	Object code	Label	Source code	Comments
NN00	3E 4F		LD A,4FH	Sets port A to input (Mode 1)
NN02	D3 PORTCO1		OUT PORTCO1,A	
NN04	DB PORTCO2		OUT PORTCO,A	Sets port B to input (mode 1)
NN06	3E FF		LD A,FFH	O/P's FFH to port B (to make O/P's inactive when first enabled)
NN08	D3 PORTDA2		OUT PORTDA2,A	
NN0A	3E CF		LD A,CFH	Sets port B to control mode (mode 3)
NN0C	D3 PORTCO2		OUT PORTCO2,A	
NN0E	3E F0		LD A,F0H	Sets B0→B3 as O/P's and B4→B7 as I/P's
NN10	D3 PORTCO2		OUT PORTCO2,A	
NN12	3E FE		LO A,FEH	Takes B0 low and then back high to start devices converting
NN14	D3 PORTDA2		OUT PORTDA2,A	
NN16	3E FF		LD A,FFH	
NN18	D3 PORTDA2		OUT PORTDA2,A	
NN1A	DB PORTDA2	POLL	IN A,PORTDA2	Waits for $\overline{BUSY}$'s to go high before continuing
NN1C	CB 67		BIT 4,A	
NN1E	28 FA		JR Z,POLL	
NN20	3E FD		LD A,FDH	Takes $\overline{RD}$ low on first ZN448
NN22	D3 PORTDA2		OUT PORTDA2,A	
NN24	DB PORTDA1		IN A,PORTDA1	Reads and stores first ZN448 conversion result
NN26	32 MEM1		LD (MEM1),A	
NN29	3E FF		LD A,FFH	Takes $\overline{RD}$ back high
NN2B	D3 PORTDA2		OUT PORTDA2,A	
NN2D	3E FB		LD A,FBH	Takes $\overline{RD}$ low on second ZN448
NN2F	D3 PORTDA2		OUT PORTDA2,A	
NN31	DB PORTDA1		IN A,PORTDA1	Reads and stores second ZN448 conversion result
NN33	32 MEM2		LD (MEM2),A	
NN36	3E FF		LD A,FFH	Takes RD back high
NN38	D3 PORTDA2		OUT PORTDA2,A	
NN3A	?		?	Return to monitor (command(s) system dependant)

KEY:

NN00 = Any Suitable starting address.
PORTCO1 = Port A control address.
PORTCO2 = Port B control address.
PORTDA1 = Port A data address.
PORTDA2 = Port B data address.
MEM1 = 16-bit address nominated for storing first ZN448 data. MEM2 = 16-bit address nominated for storing second ZN448 data.
(Remember that MEM1 and MEM2 need to be assembled in the order Lo-byte, Hi-byte in the object code).

COMMENTS

The principles illustrated in program 3 can be extended to allow the interfacing of more ZN448's. In fact it can immediately be seen that there are four port B lines spare that can be used for this purpose.

Further, up to three $\overline{\text{BUSY}}$ outputs can be connected to a single port bit and likewise up to three $\overline{\text{WR}}$ inputs can be driven from a single port bit - but here the pull-up resistor may need reducing to 2.4K. (If a CMOS PIO is used, the pull-up resistor can be dispensed with).

We can readily interface four ZN448's by using two port lines to drive the $\overline{\text{WR}}$ inputs and two port lines to monitor the $\overline{\text{BUSY}}$ outputs. The remaining four port lines connecting to the $\overline{\text{RD}}$ inputs and being used to select the required ZN448.

If the $\overline{\text{BUSY}}$ outputs are not polled and a software delay is used instead (covered in the section on interfacing a single ZN447/8/9), we can interface up to 6 devices. Two of the port lines will be needed to drive the 6 $\overline{\text{WR}}$ inputs and the remaining 6 lines will again be used to enable the required ZN448.

The leakage current of the ZN448 three-state outputs need not concern us ($\pm 2\mu$A max. at 2V).

If the software needs changing to suit a particular hardware setup, the above principles are still applicable i.e.:

- Initiate conversions by taking the relevant port bit(s) assigned to the $\overline{\text{WR}}$ inputs low and back high.
- Ensure that conversion is over before reading the result - by polling the $\overline{\text{BUSY}}$ outputs (or using a softare delay).
- Enable the ZN448's individually (to prevent contention) - by taking the appropriate port bit(s) and hence $\overline{\text{RD}}$ inputs low individually - and read the conversion result.

In practice it may be that we are interested in only one of the ZN448's at a particular time. Here, though we may start several devices converting at the same time, we can just ignore the others and read only the desired device.

DATA ACQUISITION UNDER INTERRUPT CONTROL

As discussed in the previous section on interrupts, the ZN448 is not a slow peripheral and hence does not need to be interrupt driven. However if it is wished to utilise the ZN448 relatively infrequently - under the control of some timing logic - then interrupts become more useful. This is considered in this section.

Here one port is assigned to reading the data from the ZN448's and another port is used to control the $\overline{\text{RD}}$ inputs and to monitor the $\overline{\text{BUSY}}$ outputs. In fact we can set the port to generate an interrupt when only one of a number of port bits go high. Thus we can generate an interrupt when a $\overline{\text{BUSY}}$ goes high. In order to get these facilities the port needs setting to its control mode (mode 3).

Care must be taken when using a port to generate interrupts in this manner. This is because the bits set to give the interrupt, must first all be low, before an interrupt can be generated on any of them going high. Also if any of these bits remain high, further interrupts will be prevented. Therefore, the relevant port bits must be set low initially and must also be set back low after the interrupting device has been serviced. This means that for our purposes, we must ensure that the $\overline{\text{WR}}$ inputs and hence the $\overline{\text{BUSY}}$ outputs, are low initially and are set back low again after servicing. This can be achieved using positive edge triggered D-type flip-flops with preset and clear inputs - see below. (Remember that $\overline{\text{BUSY}}$ is held low by a low on the $\overline{\text{WR}}$ input and goes high at the end of a conversion).

An example, consider interfacing two ZN448's as follows:

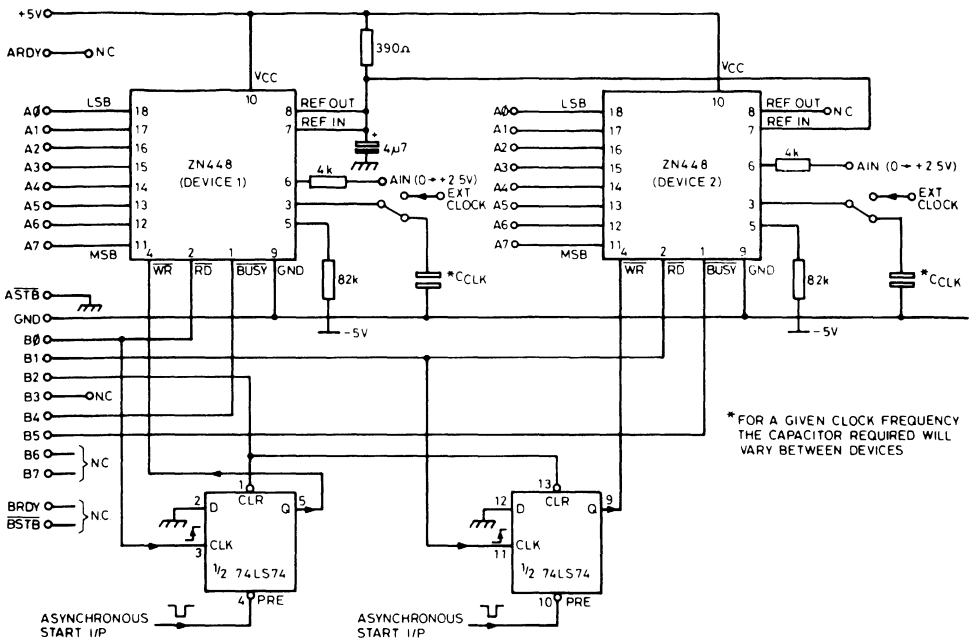


Fig. 6 Interfacing 2 × ZN448's to the Z80 using both ports of a Z80 PIO - interrupt driven

(Note that again one reference is used to drive both devices, as in the previous section).

In the circuit of Fig. 6, B2 is used to clear the $\overline{\text{BUSY}}$'s initially and the rising edge of the relevant $\overline{\text{RD}}$ signal is used to clear the $\overline{\text{BUSY}}$'s after servicing (as described below). Thus complying with the above requirements.

The falling edge of the asynchronous start input signal from the timing logic, forces the Q output high on the associated D-type flip-flop. Hence the $\overline{\text{WR}}$ input, which was previously low, is now taken high and this starts a conversion. At the end of the conversion the $\overline{\text{BUSY}}$ output goes high and this is used to generate our interrupt.

During the service routine, the $\overline{\text{RD}}$ input on a given device is taken low to enable the outputs, and then back high after the data has been latched into port A. Thus a $\overline{\text{RD}}$ positive edge is generated every time a device is read. This edge clocks a low through to the Q output on the appropriate D-type, and hence takes the relevant $\overline{\text{WR}}$ input and $\overline{\text{BUSY}}$ output low.

For correct clearing of the $\overline{\text{BUSY}}$'s and hence correct operation, the asynchronous start input signals must:

(i) be inactive (high) when the CLR inputs on the D-types (B2) are low initially.

(ii) have returned back high after initiating a conversion, before the associated $\overline{\text{RD}}$ positive edge occurs.

PROGRAM EXAMPLE

This program vectors to an interrupt service routine on the occurrence of an interrupt. The service routine then reads and stores the data from the interrupting ZN448('s).

Conversion is initiated by the users timing logic and an interrupt is generated when one or more of the $\overline{\text{BUSY}}$ outputs goes high.

The μP is set to interrupt mode 2 as the ports are designed to be used with this mode. The contents of the I register and the port interrupt vector are combined by the μP to form a 16-bit vector. This vector is then used to look up the starting address of the interrupt service routine. The μP then loads the program counter with this address and continues program execution from this location.

PROGRAM STATEMENTS

: It is assumed that the user initiates conversion correctly when required.

: It is assumed that both ports need initialising.

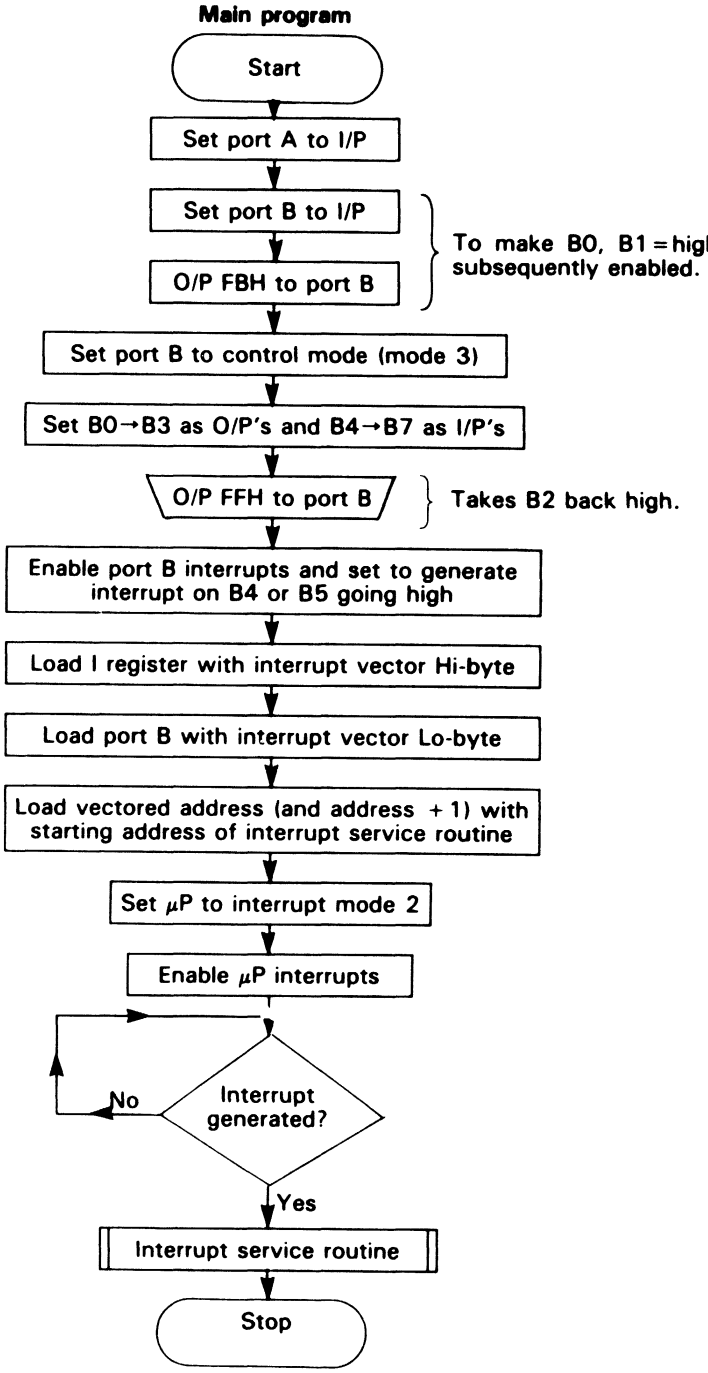
: Nominate memory locations for the vectored address, the interrupt service routine and for storing the conversion results.

: FEH = Select first ZN448 word.

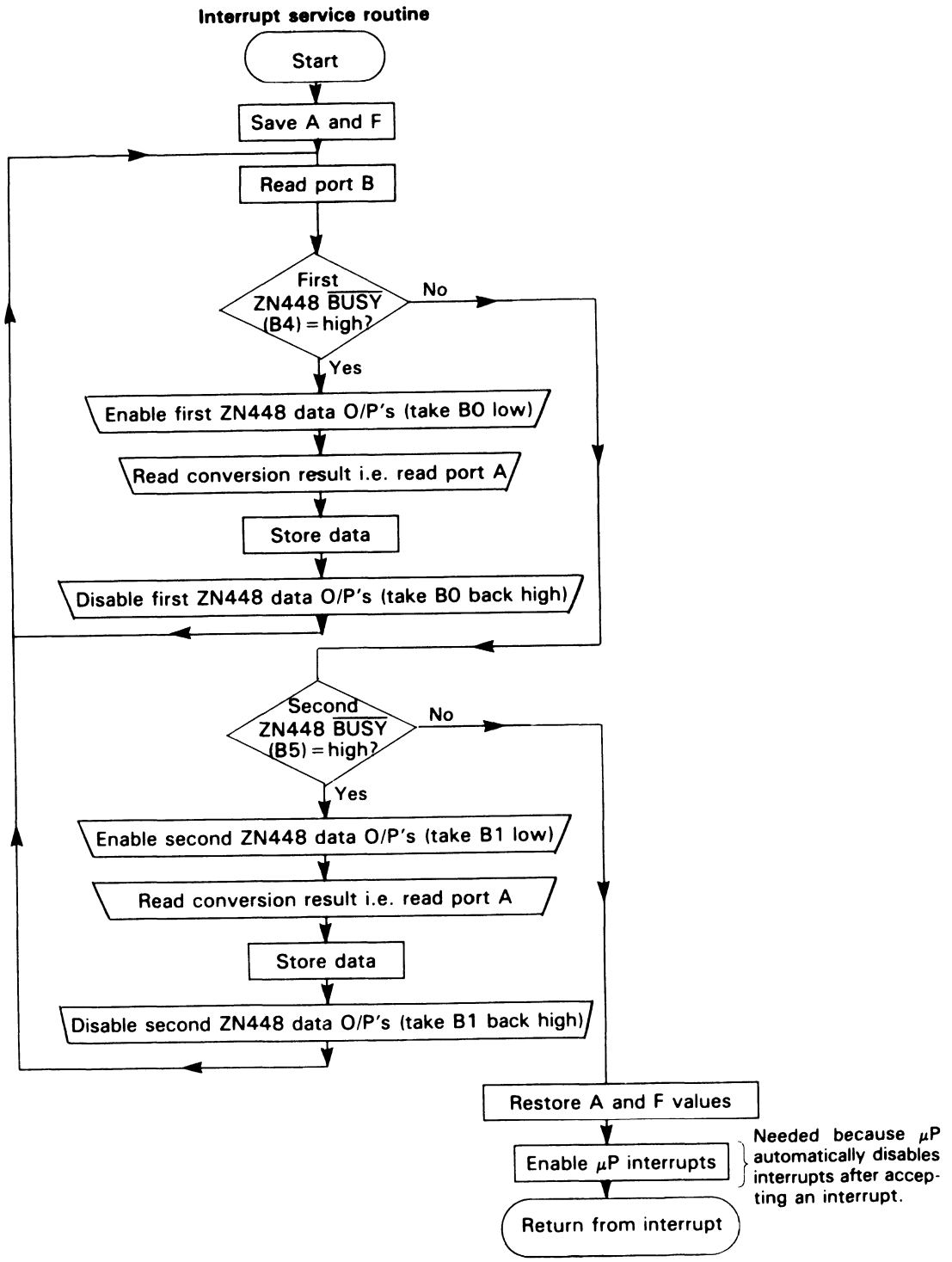
: FDH = Select second ZN448 word.

: FBH = Clear $\overline{\text{BUSY}}$ outputs word.

FLOWCHART 4


Main program
Start
Set port A to I/P
Set port B to I/P
O/P FBH to port B
To make B0, B1 = high and B2 = low when O/P's subsequently enabled.
Set port B to control mode (mode 3)
Set B0→B3 as O/P's and B4→B7 as I/P's
O/P FFH to port B
Takes B2 back high.
Enable port B interrupts and set to generate interrupt on B4 or B5 going high
Load I register with interrupt vector Hi-byte
Load port B with interrupt vector Lo-byte
Load vectored address (and address + 1) with starting address of interrupt service routine
Set μP to interrupt mode 2
Enable μP interrupts
Interrupt generated?
No
Yes
Interrupt service routine
Stop

FLOWCHART 4 (cont.)



PROGRAM LISTING

PROGRAM 4

Address	Object code	Label	Source code	Comments
NN00	3E 4F		LD A,4FH	
NN02	D3 PORTCO1		OUT PORTCO1,A	Sets port A to I/P (Mode 1)
NN04	D3 PORTCO2		OUT PORTCO2,A	
NN06	3E FB		LD A,FBH	Sets port B to I/P (mode 1) and sets CLR on D-types to go low when port O/P's enabled
NN08	D3 PORTDA2		OUT PORTDA2,A	
NN0A	3E CF		LD A,CFH	
NN0C	D3 PORTCO2		OUT PORTCO2,A	Sets port B to control mode (mode 3)
NN0E	3E F0		LD A,F0H	
NN10	D3 PORTCO2		OUT PORTCO2,A	Sets B0→B3 as O/P's and B4→B7 as I/P's
NN12	3E FF		LO A,FFH	
NN14	D3 PORTDA2		OUT PORTDA2,A	Takes CLR on D-types back high
NN16	3E B7		LD A,B7H	
NN18	D3 PORTCO2		OUT PORTCO2,A	Sets port B to generate Int. on B4 or B5 going high, also enables port interrupts
NN1A	3E CF		LD A,CFH	
NN1C	D3 PORTCO2		OUT PORTCO2,A	
NN1E	3E IVECH		LD A,IVECH	
NN20	ED 47		LD I,A	Loads I reg. with interrupt vector Hi-byte
NN22	3E IVECL		LD A,IVECL	
NN24	D3 PORTCO2		OUT PORTCO2,A	Loads port B with interrupt vector Lo-byte
NN26	3E SERVL		LD A,SERVL	
NN28	32 IVEC		LD (IVEC),A	
NN2B	3E SERVH		LD A,SERVH	Loads vectored address (and next consecutive address) with starting address of interrupt service routine
NN2D	32 IVEC + 1		LD (IVEC + 1),A	
NN30	ED 5E		IM 2	Sets μP to interrupt mode 2
NN32	FB		EI	Enables μP's interrupts
NN33	76		HALT	Waits for Interrupt (or reset!)
NN34	?		?	Returns to monitor (command(s) system dependant)

PROGRAM 4 (cont.)

Interrupt service routine

Address	Object code	Label	Source code	Comments
MM00	F5		PUSH AF	Saves current values of A and F
MM01	DB PORTDA2	POLL1	IN A,PORTDA2	Reads port B
MM03	CB 67		BIT 4,A	Tests B4 and jumps if B4 = 0
MM05	28 0F		JR Z,POLL2	
MM07	3E FE		LD A,FEH	Selects first ZN448
MM09	D3 PORTDA2		OUT PORTDA2,A	
MM0B	DB PORTDA1		IN A,PORTDA1	Reads and stores first ZN448 data
MM0D	32 MEM1		LD (MEM1),A	
MM10	3E FF		LD A,FFH	Puts first ZN448 O/P's back into high impedance state
MM12	D3 PORTDA2		OUT PORTDA2,A	
MM14	18 EB		JR, POLL1	Jumps back to read port B
MM16	CB 6F	POLL2	BIT 5,A	Tests B5 and jumps if B5 = 0
MM18	28 0F		JR Z,RETURN	
MM1A	3E FD		LD A,FDH	Selects second ZN448
MM1C	D3 PORTDA2		OUT PORTDA2,A	
MM1E	DB PORTDA1		IN A,PORTDA1	Reads and stores second ZN448 data
MM20	32 MEM2		LD (MEM2),A	
MM23	3E FF		LD A,FFH	Puts second ZN448 O/P's back into high impedance state
MM25	D3 PORTDA2		OUT PORTDA2,A	
MM27	18 D8		JR, POLL1	Jumps back to read port B
MM29	F1	RETURN	POP AF	Restores A and F values
MM2A	FB		EI	Re-enables μP Int's.
MM2B	ED 4D		RETI	Return from Int.

KEY:

NN00 = Any Suitable starting address.
PORTCO1 = Port A control address.
PORTCO2 = Port B control address.
PORTDA1 = Port A data address.
PORTDA2 = Port B data address.
IVECL = Low byte of 16-bit interrupt vector (in port).
IVECH = High byte of 16-bit interrupt vector (in I Reg.).
IVEC = 16-bit interrupt vector formed by IVECH and IVECL.
IVEC + 1 = 16-bit address one location higher up in memory than IVEC.
SERVL = Interrupt service routine starting address-low byte.
SERVH = Interrupt service routine starting address-high byte.
MM00 = 16-bit starting address for interrupt service routine formed by SERVH and SERVL.
MEM1 = 16-bit address nominated for storing first ZN448 data.
MEM2 = 16-bit address nominated for storing second ZN448 data.
(Remember that the above 16-bit addresses need assembling in the order Lo-byte, Hi-byte in the object code).

COMMENTS

The principles illustrated above can be extended to allow more ZN448's to be interrupt driven in this manner. Readily we can interface three ZN448's with each $\overline{RD}$ and $\overline{BUSY}$ allocated to their own port bit. Further if we clear the $\overline{BUSY}$ outputs by some method which does not use one of the port bits, we can interface four ZN448's. (For example we could pulse the CLR inputs low on the D-types, by writing to an address dedicated to this purpose).

It is important to realise that in the above example, the μP was not allowed to return from the service routing until both $\overline{BUSY}$'s were low simultaneously. This is to ensure that none of them remain high and inhibit further interrupts! Regardless of how many ZN448's are being interfaced, the same applies i.e. ensure that all $\overline{BUSY}$'s are low before returning from the service routine.

The software may need modifying to suit a particular hardware setup. If so, then in addition to the above, it should be ensured that the $\overline{BUSY}$ outputs are cleared initially and after device servicing.

The leakage current of the ZN448 three-state outputs need not concern us ($\pm 2\mu$A max. at 2V).

FURTHER CONSIDERATIONS

Some sections of the above programs can be separated out and placed in the users initialisation routines i.e. they do not need repeating once proper initialisation has been achieved. Also the above programs were ended in some "return to monitor' commands. However in a real environment, sections of the programs will probably form part of a subroutine or loop, or part of a service routine.

The data acquired in the above examples was put straight into memory. It could instead have been processed and then either stored or outputted to another port.

In the examples given, where the $\overline{RD}$ inputs are controlled by port bits, these bits could be further decoded, thus extending their addressing range. This would also have the benefit of preventing the outputs from more than one device being enabled together (sould an erroneous word be accidentally written to that port).

Again when the ZN448 three-state outputs are controlled, various other devices can be connected to the port that reads the data. This port could also be swapped between input and output modes - provided proper control is exerted.

In the foregoing description, port A has been used for reading the data and port B for controlling/monitoring the ZN448's. These ports could be interchanged or could even be from different PIO's.

SUMMARY

This report describes the versatility with which the Plessey ZN447/8/9 A-D converters can be interfaced to the Z80μP. Clearly there are many other ways of storing and processing the acquired data. The user can tailor these to suit his own particular requirements.

Most of the above principles can also be applied when interfacing the ZN447/8/9 to other popular μPs. Full Engineering and Applications support is available to assist with technical queries relating to the applications of any Plessey converter products.

An Analogue Output System for the Z80μP using the ZN558 8-Bit DAC

This report is intended to illustrate how to interface the Plessey ZN558 8-bit D-A converter to a Z80 based microprocessor system using a Z80 PIO. Circuit diagrams and program examples are given to enable the user to get his interface system working. The following is equally applicable to the faster versions of the Z80 microprocessor and the Z80 PIO and also to the CMOS versions.

In order to keep this report concise it is assumed the reader is familiar with the Z80 system.

THE ZN558 D-A CONVERTER

The ZN558 is a monolithic 8-bit μP compatible D-A converter with input latches to facilitate updating from a data bus. It operates from a single +5V supply and is TTL and 5V CMOS compatible. The latch is transparent when $\overline{\text{enable}}$ is LOW and the data is held when enable is taken HIGH. The ZN558 also contains a 2.5V reference the use of which is pin optional to retain flexibility. An external reference may therefore be substituted.

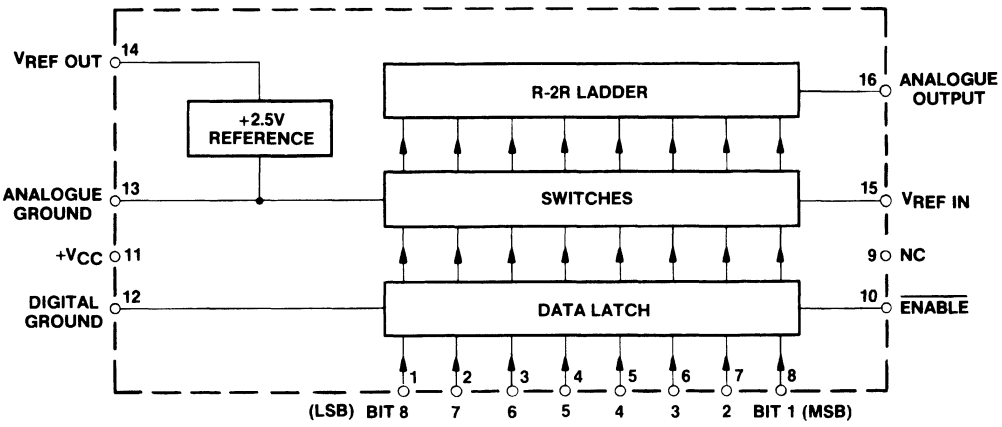


Fig. 1 ZN558 system diagram

The typical worst case settling time for the ZN558 is 1.25μs and the typical 1LSB major transition settling time is 800ns.

Further information including suitable analogue output buffering circuits can be obtained from the data sheet.

Z80 PIO

The Z80 PIO is a programmable two port device which provides a TTL compatible interface between peripheral devices and the Z80 CPU. It is capable of interfacing directly to the CPU without any external logic. The two 8-bit, bidirectional ports, each have two handshake lines (RDY and $\overline{STB}$) for use when transferring data to or from peripherals. Either port or indeed any port bit, can be programmed to act as an input or output.

This is a very brief introduction to a very complex device. Further information can be obtained from the manufacturers data.

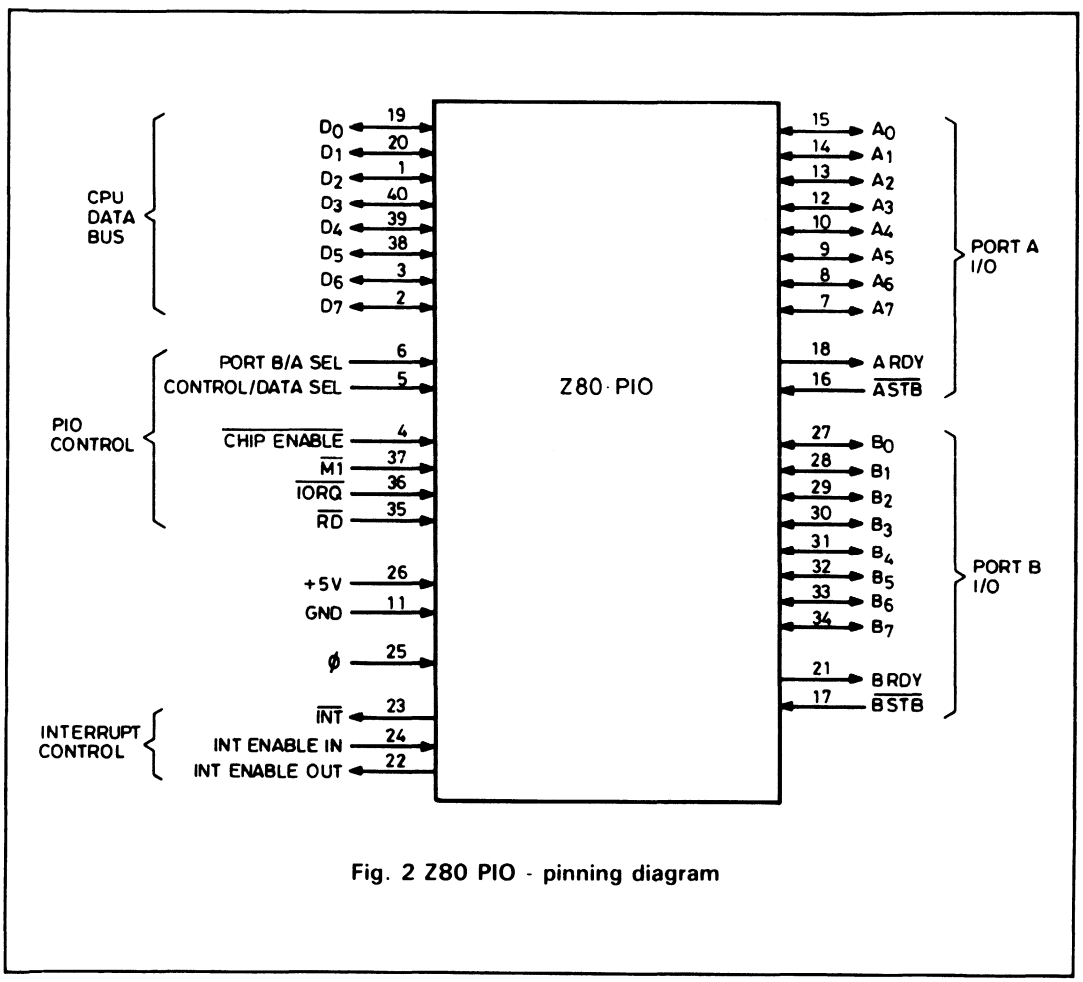


Fig. 2 Z80 PIO - pinning diagram

INTERFACING A SINGLE ZN558 D-A TO THE Z80

If the Z80 is required to interface to only one ZN558, this can be achieved with a single port (outputting data to the ZN558), if the enable input is tied LOW.

With $\overline{\text{enable}}$ tied LOW, the ZN558 will convert whatever is presented to its inputs at all times. The circuit diagram for this arrangement is as follows:

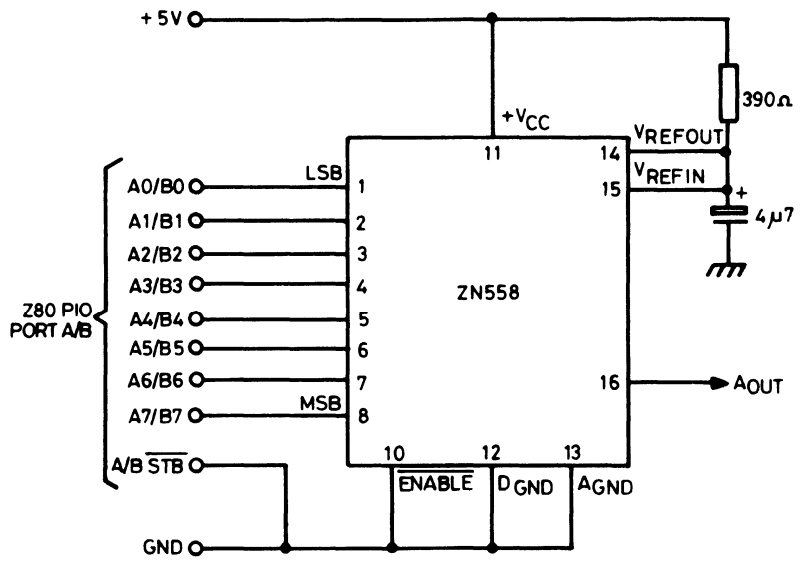


Fig. 3 Circuit diagram for interfacing a single ZN558 to the Z80

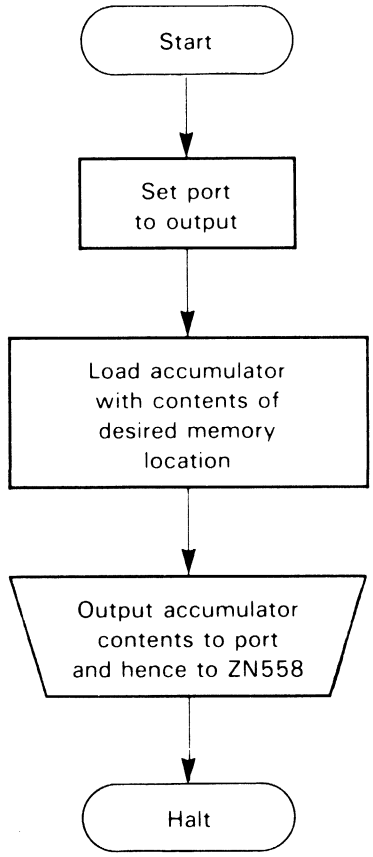
PROGRAM EXAMPLE

This is a program to read the contents of a memory location - which has been previously loaded with the desired data - and subsequently output this data to the ZN558 via one of the Z80 PIO ports.

PROGRAM - STATEMENTS

:It is assumed that the port is in the reset state:
:Load desired memory location with required data:

PROGRAM FLOWCHART



PROGRAM LISTING

Address	Object code	Source code	Comments
NN00	3E 0F	LD A, 0FH	Sets port to O/P (mode O).
NN02	D3 add1	OUT add1, A	
NN04	3A YZ WX	LD A, (WXYZ)	Loads acc. with the desired data from the specified memory location.
NN07	D3 add2	OUT add2, A	O/P's acc. contents to port and hence to ZN558
NN09	76	HALT	Halts processor.

NOTES

NN00 = Any convenient starting address
add1 = Port control address
add2 = Port data address
WXYZ = MEMORY LOCATION which has been previously loaded with data, where WX = HI-address byte and YZ = LO-address byte.

COMMENTS

This arrangement has the advantage of simplicity and is useful where a port can be dedicated to this purpose.

The data in the above example was obtained from the designated memory location. This Data could instead have been read in from some port and maybe processed before subsequently being outputted to the ZN558.

INTERFACING ONE OR MORE ZN558's TO THE Z80

The general arrangement for interfacing several ZN558's to a Z80 system is shown in the following diagram.

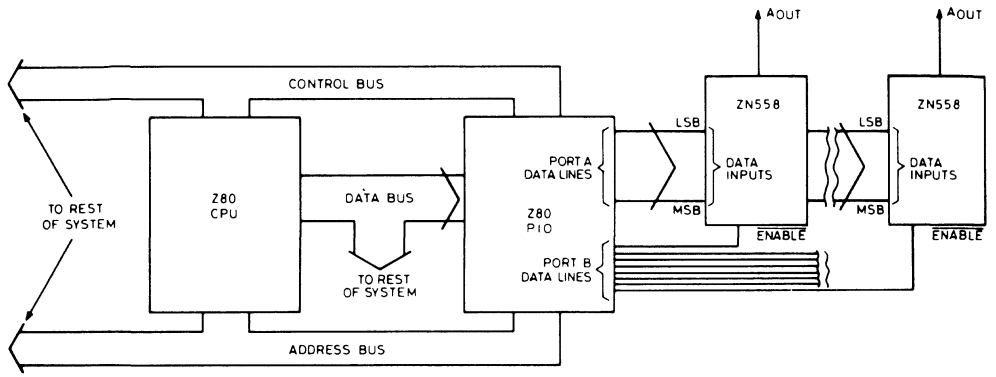


Fig. 4 Interfacing several ZN558's to the Z80 - schematic diagram

Here the ZN558 data inputs are connected to the data lines from one port and the enable inputs are controlled with the data lines from another port. These lines are taken LOW individually when it is required to make one of the ZN558's read the data presented to its inputs. The relevant line can then be taken back high to latch this data. This arrangement allows the ZN558's to be addressed or selected individually and ignore the data the rest of the time.

The data set-up and hold times and the $\overline{\text{enable}}$ pulse width need not be considered since they are much less than the Z80 instruction execution times.

A circuit diagram and program example for interfacing to two ZN558's follows. This implementation can easily be extended if more ZN558's are required:

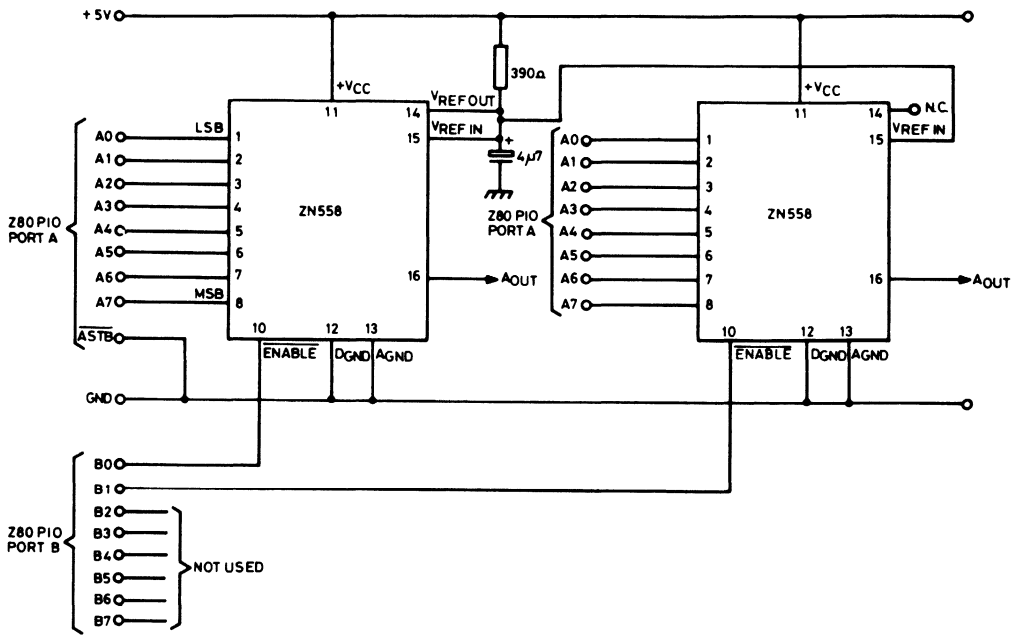


Fig. 5 Circuit diagram for interfacing two ZN558's to the Z80 - latching controlled by port B

Note that in the above diagram, the reference input ($V_{REF\ IN}$) of the second ZN558 is driven from the reference output ($V_{REF\ OUT}$) of the first ZN558. This provides excellent gain tracking between the converters. Up to five ZN558's may be driven from a single internal reference without having to change the reference resistor (R_{REF}).

PROGRAM EXAMPLE

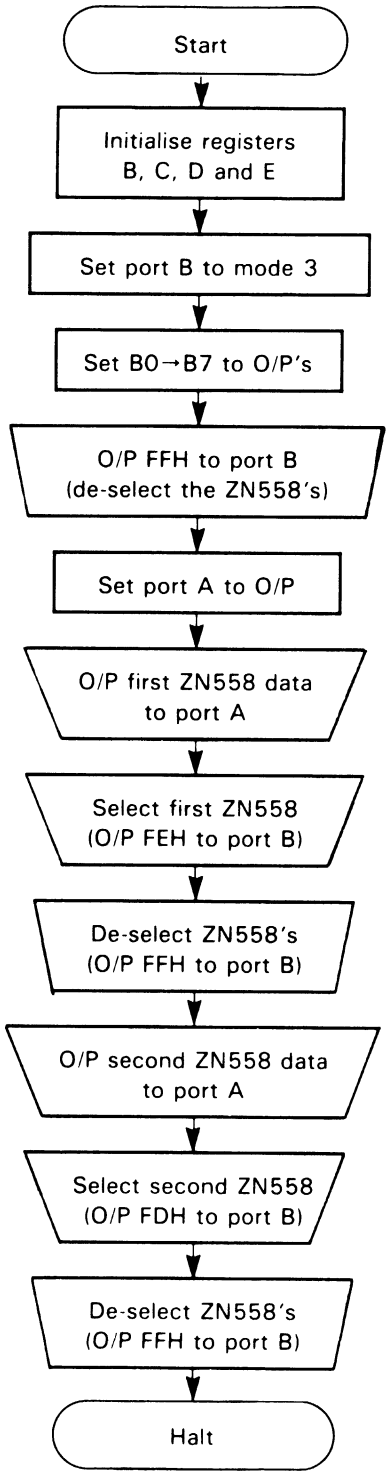
This is a program to write different data to two ZN558's. Port A is used for writing the data and port B is used to select the relevant ZN558.

Some of the Z80 registers are being used to hold the select and de-select words and to hold the port B data address.

PROGRAM - STATEMENTS

:It is assumed that the port is in the reset state:
B0 connected to enable on first ZN558
B1 connected to the enable on second ZN558
C REGISTER = Port B data address
D REGISTER = De-select ZN558's word (FFH)
E REGISTER = Select first ZN558 word (FEH)
B REGISTER = Select second ZN558 word (FDH)

PROGRAM FLOWCHART



PROGRAM LISTING

Address	Object code	Source code	Comments
NN00	06 FD	LD B, FDH	Initialises registers B,C,D & E
NN02	0E add1	LD C, add1	
NN04	16 FF	LD D, FFH	
NN06	1E FE	LD E, FEH	
NN08	3E CF	LD A, CFH	Sets port B to mode 3
NN0A	D3 add2	OUT add2, A	
NN0C	3E 00	LD A, 00H	Sets B0→B7 to O/P's
NN0E	D3 add2	OUT add2, A	
NN10	ED 51	OUT (C), D	O/P's FFH to port B i.e. de-selects ZN558's
NN12	3E 0F	LD A, 0FH	Sets port A to O/P's
NN14	D3 add3	OUT add3, A	
NN16	3E data1	LD A, data1	O/P's first ZN558 data to Port A
NN18	D3 add4	OUT add4, A	
NN1A	ED 59	OUT (C), E	Selects first ZN558
NN1C	ED 51	OUT (C), D	De-selects ZN558's
NN1E	3E data2	LD A, data 2	O/P's second ZN558 data to Port A
NN20	D3 add4	OUT add4, A	
NN22	ED 41	OUT (C), B	Selects second ZN558
NN24	ED 51	OUT (C), D	De-selects ZN558's
NN26	76	HALT	HALTS processor

NOTES

NN00 = Any convenient starting address
add1 = Port B data address
add2 = Port B control address
add3 = Port A control address
add4 = Port A data address
data1 = Data to first ZN558 (selected by B0)
data2 = Data to second ZN558 (selected by B1)

COMMENTS

As previously stated this principle can be extended to address additional ZN558's if required. The enable inputs on these other ZN558's being connected to the desired port B data bits. Each port bit can then be taken low individually as required - by writing different select words to the port - to address the relevant ZN558.

The relevant D.C. characteristics for the ZN558 and the Z80 PIO are shown in the following table:

Z80 PIO - CMOS	Z80 PIO - NMOS	ZN558
$V_{OH} = 2.4V$ min. when $I_{OH} = -1.6mA$	$V_{OH} = 2.4V$ min. when $I_{OH} = -250\mu A$	$I_{IH} = 20\mu A$ max. when $V_{IH} = 2.4V$
$V_{OL} = 0.4V$ max. when $I_{OL} = 2mA$	$V_{OL} = 0.4V$ max. when $I_{OL} = 2mA$	$I_{IL} = -5\mu A$ max. when $V_{IL} = 0.4V$

TABLE 1 ZN558 AND Z80 PIO - D.C. CHARACTERISTICS

In some applications, it may be undesirable to use the Z80 registers as above i.e. to hold the ZN558('s) and port addressing words. If this is the case, these instructions can easily be substituted with:

```
LD A, byte
OUT address, A
```

as have been used in other parts of the program.

FURTHER CONSIDERATIONS

In the above examples the port used for outputting the data byte is set to mode O. However for our purpose we do not need the handshake lines (RDY and $\overline{STB}$). Therefore the RDY line is ignored and the $\overline{STB}$ line is tied low (to prevent any spurious transitions). If preferred this port could be set to mode 3 with all the bits set as outputs (here RDY is held LOW and $\overline{STB}$ is inhibited internally).
In addition to connecting the ZN558('s) to the data port, it may be required to connect a peripheral that will utilise the handshake lines (obviously the ZN558('s) will have to be selected only when required, to ignore unwanted data). Here it is up to the user to ensure that this other peripheral ignores the handshake lines when data is written to the ZN558('s) e.g. gate RDY and possibly $\overline{STB}$ with lines from the addressing port. Further, addressing the ZN558('s) as above allows the data port to be swapped between input and output modes.

Above port A has been used for outputting the data and port B used for addressing the ZN558's. This need not be the case, the ports could be swapped round or even be from different PIO's.

Also the programs given above have been terminated with the HALT command. For evaluation purposes this could be replaced for example with some command(s) that will return control to the monitor. In practice the program used will probably form part of a subroutine or loop.

SUMMARY

The foregoing describes the ease with which the ZN558 can be interfaced to the Z80 microprocessor. Clearly, many other variations are possible on loading, processing and outputting the data and the user can tailor these to suit his own particular requirements.

Further the above principles can easily be extended to allow the ZN558 to be interfaced to other popular microprocessors.

ZN450 3½ Digit DVM Evaluation Kit

The ZN450 is the first charge-balancing DVM IC to contain all the active circuitry on a single chip and requires only a handful of external passive components and a display to function.

No engineering design effort is required and the only obstacle to building a DVM is that of obtaining the components and wiring a breadboard.

The ZN450 evaluation kit is intended to remove even this obstacle and to facilitate the evaluation of this unique IC. The kit contains all the components necessary to construct a DVM with a basic sensitivity of 199.9mV full-scale, powered from a 9V battery (not supplied).

In addition, provision is made on the printed circuit board for various options to increase the versatility of the DVM. Components required for these options are NOT provided but suitable values are indicated in the text. Additional applications data on the ZN450 is given in the data sheet.

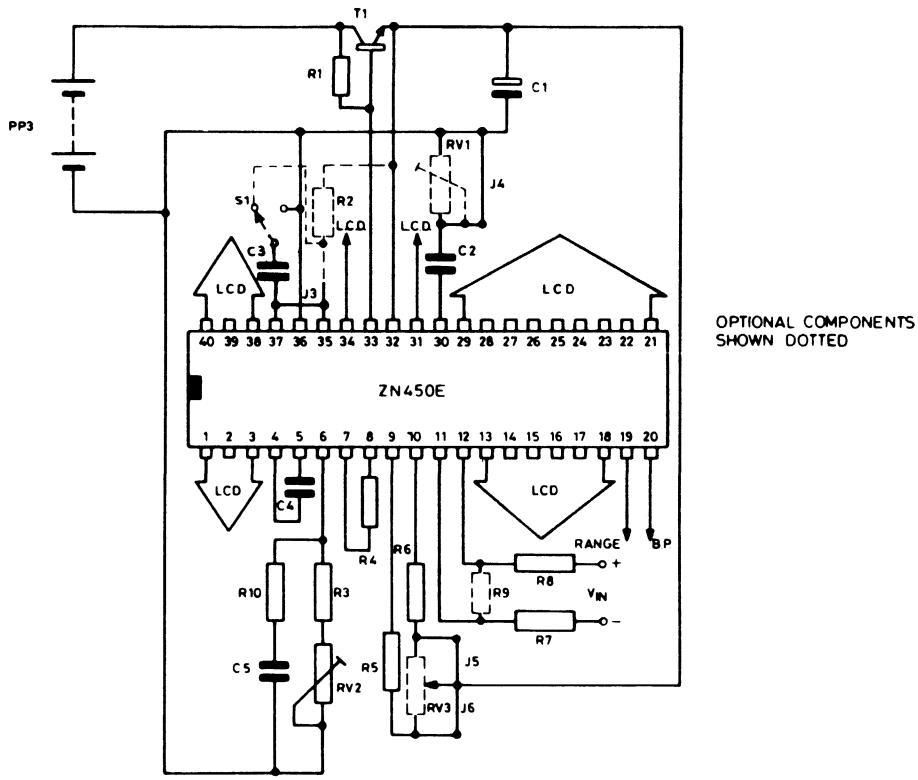


Fig. 1 Circuit diagram

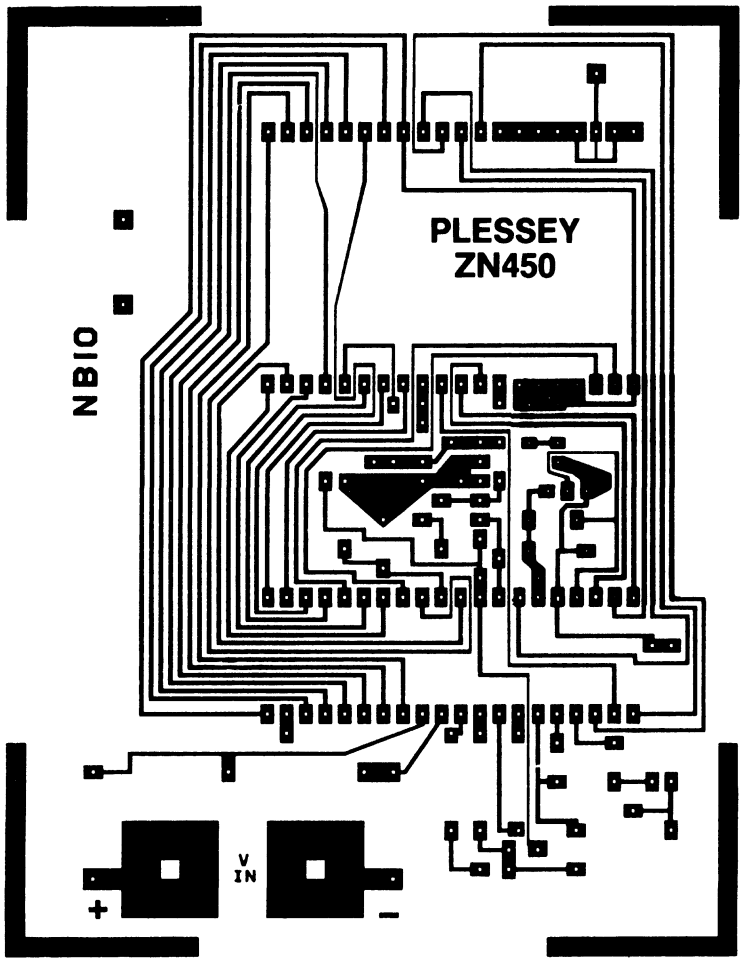


Fig. 2 Printed circuit board (actual size)

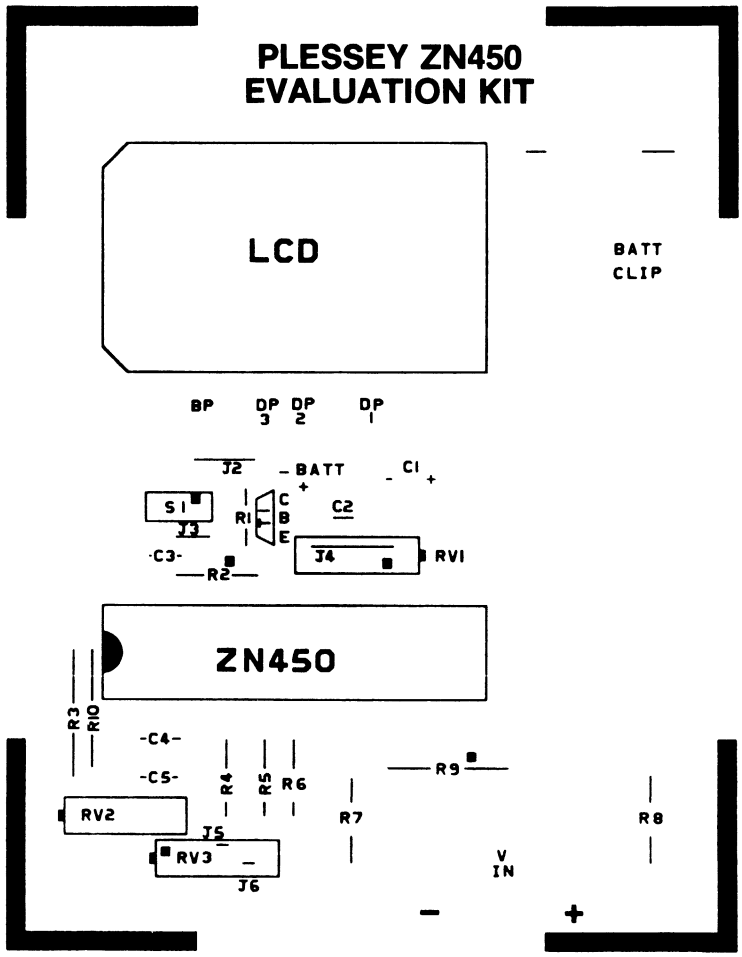


Fig. 3 Component layout (actual size)

Resistors

R1	=	15k 5%
R3	=	470k 2%
R4	=	200k 1%
R5	=	10M 5%
R6	=	10M 5%
R7	=	1k 5%
R8	=	1k 5%
R10	=	10k 5%
RV2	=	100k multi-turn trimmer

Capacitors

C1	=	47μF 16V
C2	=	330 or 470pF
C3	=	100nF
C4	=	100nF
C5	=	10nF

Semiconductors

IC1	=	ZN450E
T1	=	ZTX108

Display

LUCID type 101 F111 or HAMLIN 3901/315/050

Hardware

Printed circuit board, 40 pin I.C. socket,
red 4mm socket, black 4mm socket,
battery connector, battery clip,
2 x 8 B.A. nut, 2 x 8 B.A. bolt,

Optional Components

R2	=	22k 5%
RV1	=	10k ¾in. multi-turn trimmer
RV3	=	1M ¾in. multi-turn trimmer
R9	=	See text
S1	=	Miniature p.c.b. slide switch

Table 1 ZN450 evaluation kit component list

CONSTRUCTION

The circuit of the ZN450 evaluation kit as supplied is shown in Fig.1, whilst the printed circuit track pattern and component layout are given in Figs. 2 and 3. Before commencing construction of the DVM check all the components against the parts list in Table 1. Please notify Plessey Semiconductors in the event of any missing, damaged or incorrect components. Note that some types of liquid crystal display are supplied with snap on connectors. These are designed for minimum insertion force and should be fitted as shown in Fig.4. The display is mated to the connector at an angle of about 30° and is then pivoted to open the connector jaws before pushing fully home. Once this has been done fit and solder all the components provided, not forgetting links J1-J6. If any of the decimal points are not to be used these should be linked to the backplane as shown in Fig.5. Decimal points which are to be used should be connected to a suitable drive circuit, examples of which are given in the ZN450 data sheet.

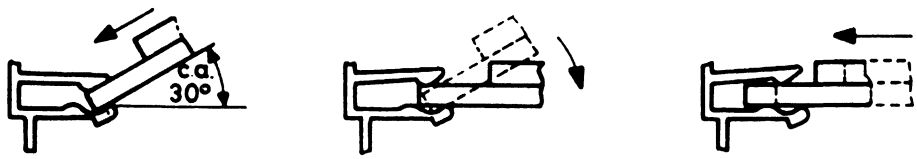


Fig. 4 Fitting the liquid crystal display connectors

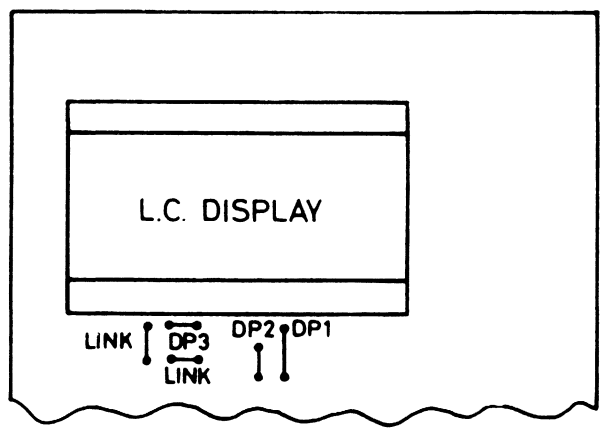


Fig. 5 Connecting unused decimal points to the backplane

Connect the battery, short input + and input − together and check for a zero reading. Apply a known voltage near full-scale and calibrate the DVM using RV2. Reverse the input leads and check that the roll-over error is less than ± 2 digits.

OPTIONS

1. **Input Attenuator**

For input ranges greater than 200mV a fixed input attenuator may be added to the board by replacing R7 and R8 with suitable components and adding R9. An unbalanced attenuator may be added if R7 is replaced with a jumper link or a balanced attenuator may be constructed by making R7 = R8.

These options are shown in Fig. 6.

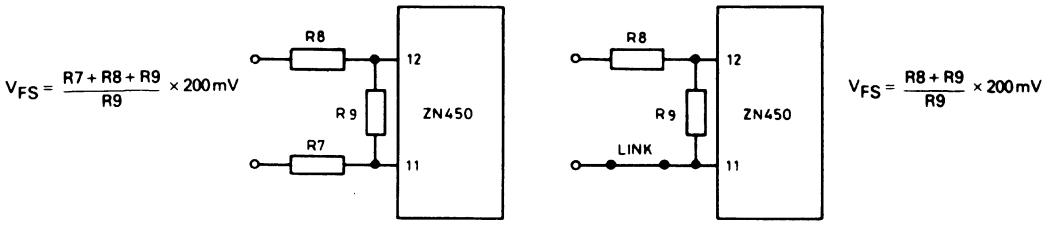


Fig. 6 Balanced and unbalanced input attenuators

2. Input offset nulling

If the ZN450 is fed from a high impedance source then the input offset current of the ZN450 may generate a zero error. The input offset current can be nulled out using RV3. If RV3 is used then omit jumper links J5 and J6.

3. Display hold

To use the display hold facility add switch S1 and resistor R2. Remove jumper link J3.

4. Adjustable oscillator frequency

The oscillator frequency, and hence the conversion rate of the ZN450, may be adjusted if J4 is replaced by potentiometer RV1.

5. Use of shunt regulator

To use the on-chip shunt regulator instead of the external series regulator transistor, omit T1, link its B and E terminals on the P.C. board with a jumper and change R1 to a suitable value as indicated in the data sheet.

6. Use of regulated 5V supply

The ZN450 may be powered from a regulated 5V supply if R1 and T1 are omitted and supply + is connected to the E terminal of T1 on the P.C. board.

Underrange/overrange output

This output is available at pin 19 of the I.C. A suitable decoding circuit is given in the data sheet.

Low battery indication

The LO BAT indicator (←on some types of display) is normally connected to the backplane. If this facility is to be used then break the thin track linking pin 38 of the display to the backplane and connect the low battery detector to pin 38. A suitable low battery detection circuit is given in the data sheet.

ZN451 3½ Digit DVM Evaluation Kit

The ZN451 is the first DVM IC that allows external signal conditioning circuits to be included inside the auto-zero loop, thus allowing their zero errors to be removed by the DVM's digital auto-zero system. In this way very low full-scale inputs can be obtained by including op-amps in the circuit.

Using low cost FET input op-amps and CMOS analogue switches full-scale input ranges of ±1.999mV can easily be achieved. However, at these sort of signal levels careful layout and grounding is mandatory. The ZN451 evaluation kit offers the user an optimised circuit board layout and all compoents for a DVM with one microvolt resolution so that the ZN451 can be evaluated without any problems.

In addition, provision is made on the printed circuit board for various optional components to increase the versatility of the DVM. These components are NOT included in the kit but suitable values are indicated in the parts list. Additional applications data on the ZN451 is also given in the data sheet.

The kit may be powered from a 9V battery (not supplied) or from any supply rail from +5V upwards.

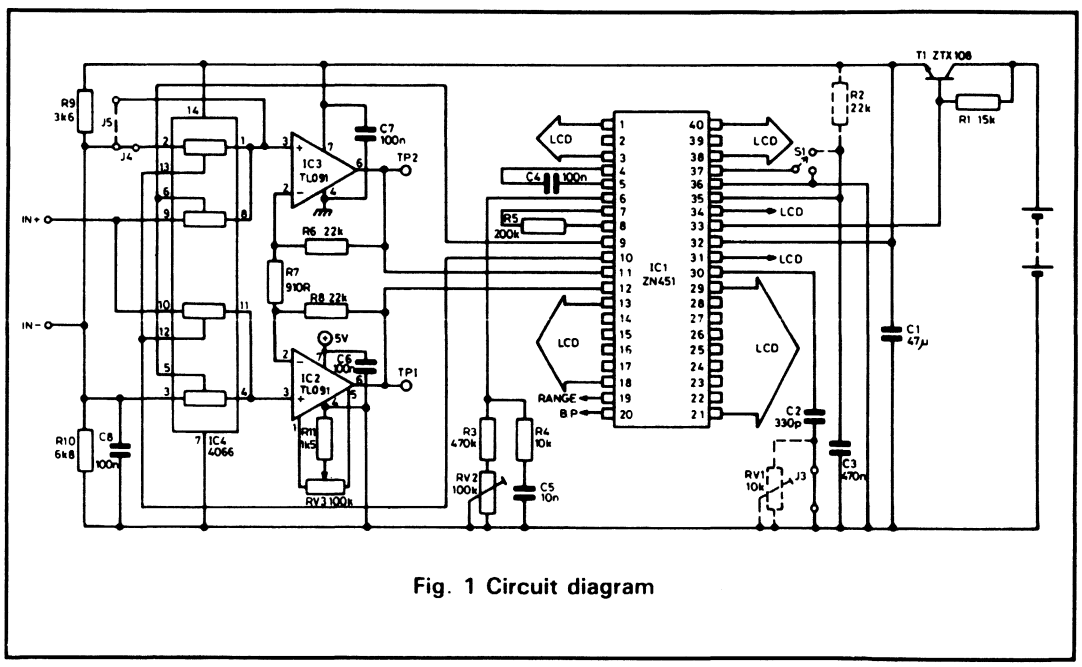


Fig. 1 Circuit diagram

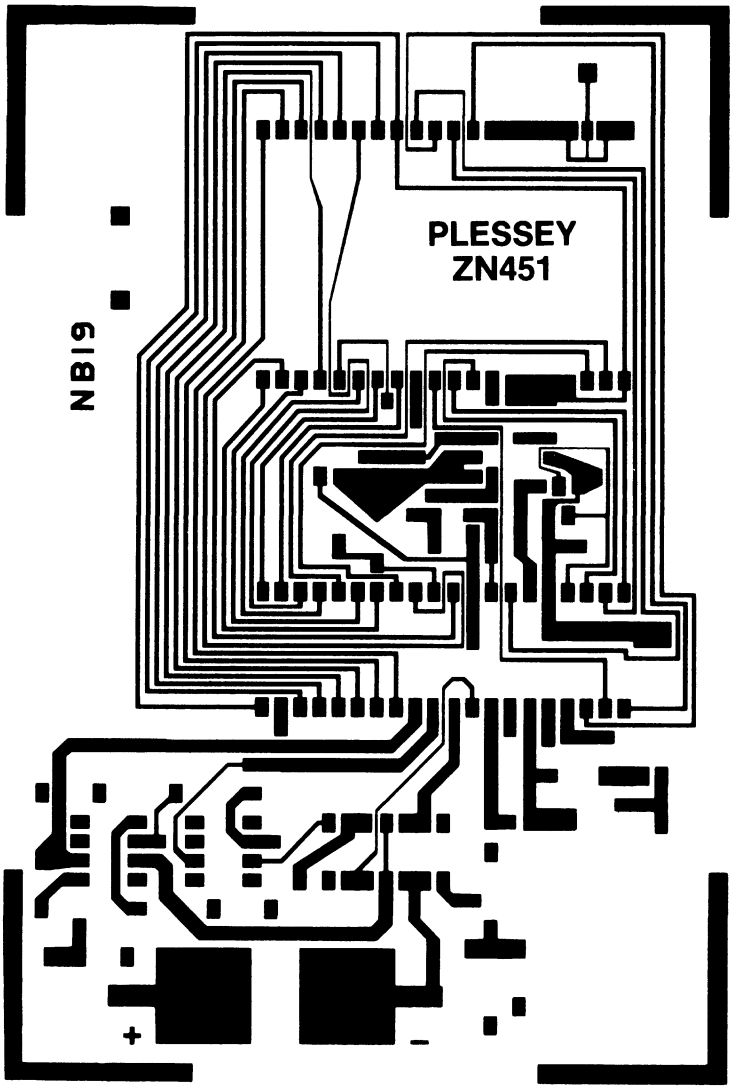


Fig. 2 Printed circuit board (actual size)

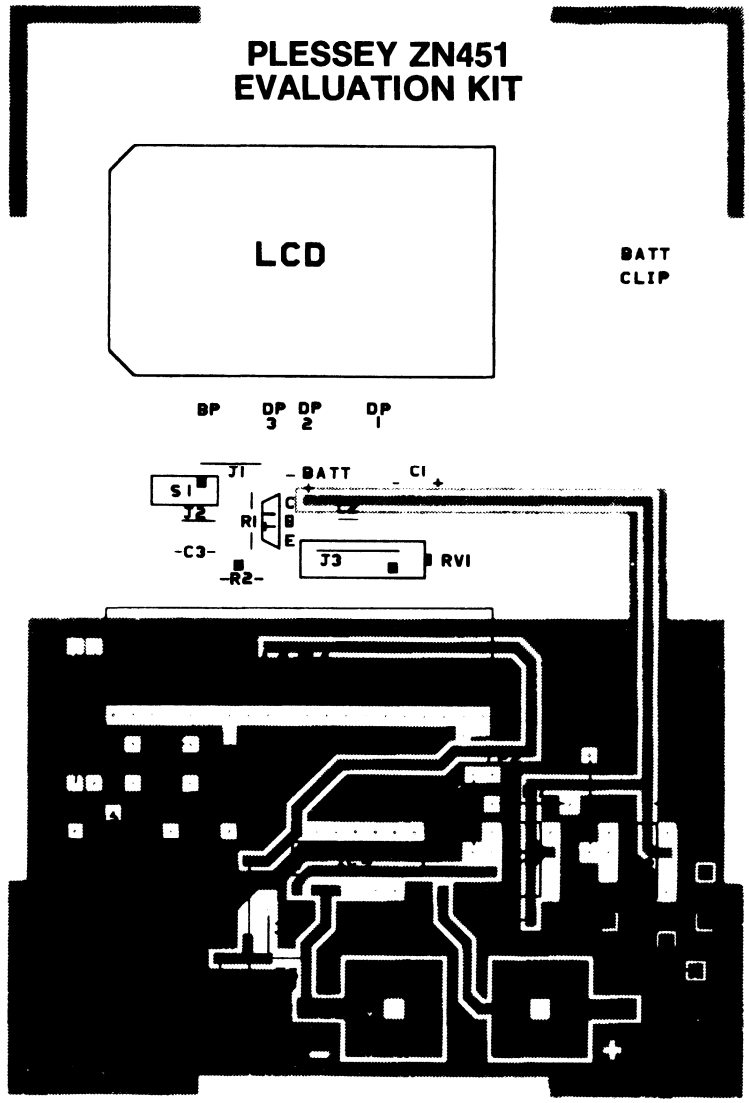


Fig. 3 Component layout (actual size)

Resistors

R1	=	15k	5%
R3	=	470k	2%
R4	=	10k	5%
R5	=	200k	2%
R6	=	22k	2%
R7	=	910R	2%
R8	=	22k	2%
R9	=	3k6	5%
R10	=	6k8	5%
R11	=	1k5	5%
RV2	=	100k	Multi-turn
RV3	=	100k	Multi-turn

Capacitors

C1	=	47μF	16V
C2	=	330pF	Ceramic
C3	=	470nF	MKH
C4	=	100nF	MKH
C5	=	10nF	MKH
C6-C8	=	100nF	MKH

Semiconductors

IC1	=	ZN451
IC2-3	=	TL091
IC4	=	CD4066
T1	=	ZTX108

Display

LUCID type 108 F111 or equivalent

Hardware

Printed circuit board, 40 pin I.C. socket,
14 pin I.C. socket, 2 x 8 pin I.C. socket,
red 4mm socket, black 4mm socket,
battery connector, battery clip,
2 x 8 B.A. nut, 2 x 8 B.A. bolt,
2 x test point terminals.

Optional components

R2	=	22k 5%
RV1	=	10k Multi-turn
S1	=	miniature p.c.b. slide switch

Table 1 ZN451 evaluation kit component list

CIRCUIT DESCRIPTION

The ZN451 I.C. operates with a nominal full-scale range of ± 100mV. It is preceded by a differential-input/differential-output amplifier comprising two FET op-amps IC2 and IC3. This has a nominal gain of 50 defined by:

$$A_V = 1 + \frac{R6 + R8}{R7}$$

which increases the full-scale sensitivity to ± 1.999mV.

The amplifier is preceded by a switch bridge comprising four CMOS analogue switches, which reverses the analogue input signal under control of the PH1 and PH2 outputs of the ZN451. A detailed description of the auto-zero operation is given on page of the ZN451 data sheet.

CONSTRUCTION

The circuit of the ZN451 evaluation kit is shown in Fig.1, whilst the printed circuit track pattern and component layout are given in Figs. 2 and 3 respectively. Before commencing construction of the DVM check all the components against the parts list given in Table 1. Please notify your supplier or Plessey Semiconductors in the event of any missing or damaged components. Note that some types of liquid crystal display are supplied with connectors designed for minimum insertion force, which should be fitted as shown in Fig.4. The display is mated to the connector at an angle of about 30° and is then pivoted to open the connector jaws before pushing fully home. Once this has been done the display and all other components can be fitted and soldered to the board, not forgetting jumper links J1, J2, J3 and J5.

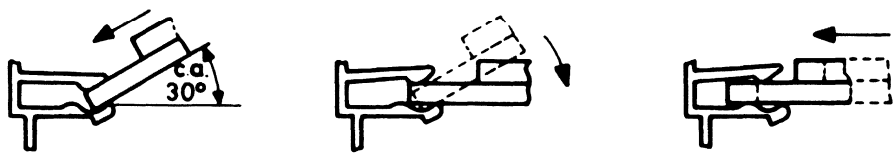


Fig. 4 Fitting the liquid crystal display connectors

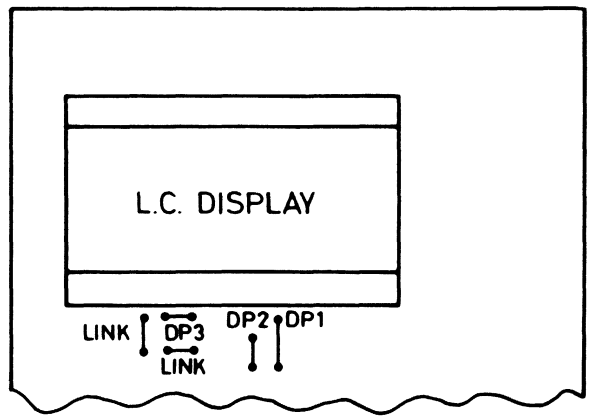


Fig. 5 Connecting unused decimal points to backplane

If any of the decimal points are not to be used they should be linked to the backplane as shown in Fig. 5. Decimal points which are used should be connected to a suitable drive circuit, examples of which are given in the ZN451 data sheet.

SETTING UP AND CALIBRATION

The ZN451 can null out zero errors of ± 150% of the full-scale output range, i.e. ± 3mV. However the worst-case input offset voltage of the TL091 is greater than this. A trimpot RV3 is therefore provided to set the quiescent output voltage of the differential amplifier to zero. Once this adjustment has been made it need not be altered again since the auto-zero system will take care of any long-term and temperature drift of the offset.

To set up the DVM connect the battery and short input + to input −. Connect a voltmeter between the test points TP1 and TP2 and adjust RV3 for a reading as near to zero as possible (typically less than 10mV can be achieved).

Disconnect the voltmeter and check that the DVM reads zero.

To calibrate the DVM connect a known input voltage near full-scale between input + and input −.

Adjust RV2 for a correct reading. Reverse the input leads and check that the roll-over error is less than ± 2 digits.

Using the DVM

When operating at such low signal levels thermal effects and noise can be a problem and the usual precautions should be observed. In particular the following should be noted.

1. To avoid thermal e.m.f's. the signal paths to each input should be identical and junctions of dissimilar metals should be avoided.

2. The temperature of the DVM circuit should not change during the measurement period or zero errors may result. For example, if the offset tempco of the differential amplifier is 10μV/°C a 0.1°C temperature change between phase 1 and phase 2 of the measurement can give a zero error of 1 count.

OPTIONS

1. Alternative full-scale input ranges

Full-scale inputs other than 1.999mV can be obtained by changing the feedback resistors of the differential amplifier. The full-scale input range is given by:

$$V_{FS} = \pm \frac{100mV}{A_V}$$

Only good quality metal film resistors should be used.

2. Display hold

To use the display hold facility add switch S1 and resistor R2. Remove jumper link J2.

3. Adjustable oscillator frequency

The oscillator frequency and hence the conversion rate of the ZN451 may be adjusted if J3 is replaced by potentiometer RV1.

4. Shunt regulator

To use the on-chip shunt regulator instead of the external series regulator omit T1 and link its B and E terminals on the P.C. board with a jumper. Change R1 to a suitable value as indicated in the data sheet.

5. Regulated + 5V supply

The ZN451 may be powered from a regulated + 5V supply such as a logic supply if R1 and T1 are omitted and supply + is connected to the E terminal of T1 on the P.C. board.

6. Underrange/overrange output

This output is available at pin 19 of the ZN451. A suitable decoding circuit is given in the data sheet.

7. Low battery indication

The LO BAT indicator (← on some types of display) is normally connected to the backplane. If this facility is to be used then break the thin track linking pin 38 of the display to the backplane and connect the low battery detector to pin 38. A suitable low battery detection circuit is given in the data sheet.

8. Single-ended input

The DVM can be contverted to a single-ended input by the following modifications.

a. Remove J5 and insert J4.

b. Replace R6 with a link.

c. Change the value of R8 to 47k if the same sensitivity is to be maintained.

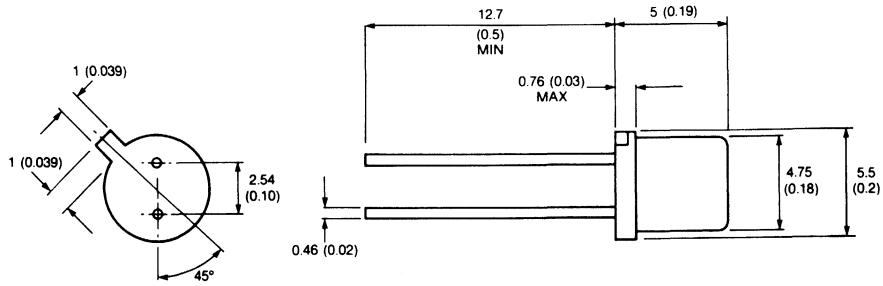
d. Remove IC3 and link pins 3 and 6 of the I.C. socket.

Package Outlines

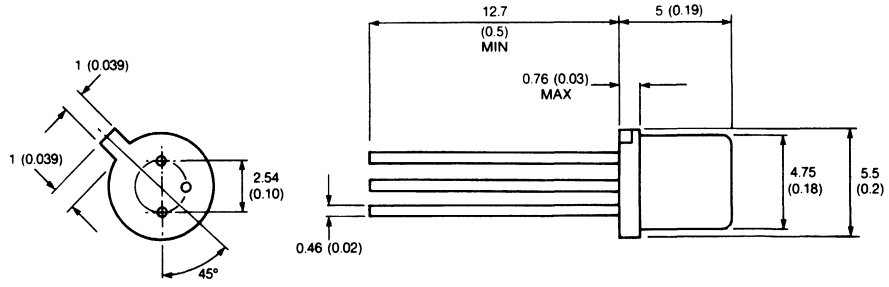
PACKAGE CODES

In 1987, Plessey Semiconductors acquired the semiconductor operation of Ferranti plc and has absorbed many Ferranti ICs into its product range. These can be identified in this Handbook by the prefixes ZN, SR or REF. The package codes for these devices differ from those (mostly Pro-Electron) adopted by Plessey Semiconductors, but will continue to be used with the device type numbers, for the foreseeable future. The table below lists the Plessey Semiconductors package codes shown on the Package Outline Drawings and their 'Ferranti' equivalents.

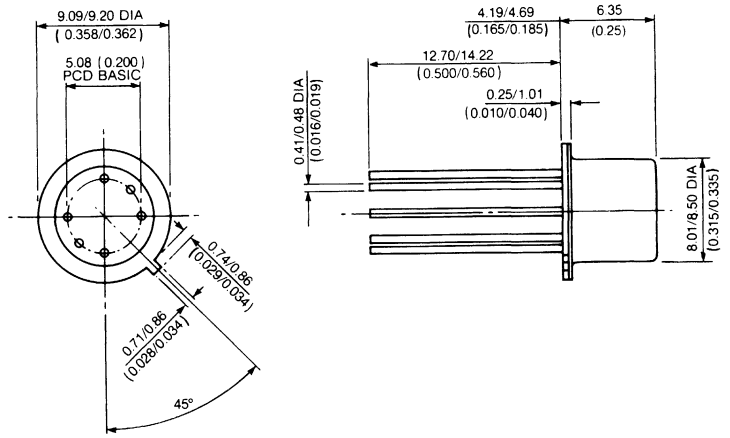
Package Description	Plessey Code	'Ferranti' Code
Ceramic DIL	DC or DG	J
Moulded plastic DIL	DP	E (also P)
Quad plastic J Lead (PLCC)	HP	Q
Leadless chip carrier	LC	AM
3-Lead miniature plastic (surface mount)	SOT-23	SOT-23
Miniature plastic DIL (surface mount)	MP	D
Miniature plastic DIL (wide body)	MP(W)	D
TO-92 (plastic)	TO-92	Z
Metal can (TO-18, TO-39)	CM	-



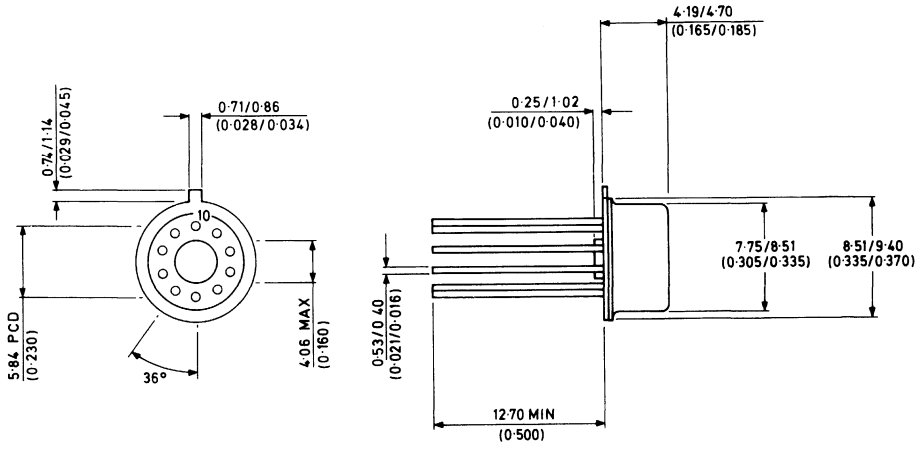
2-LEAD METAL CAN - CM2



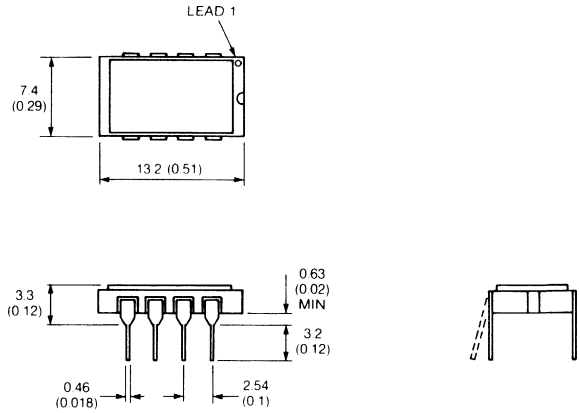
3-LEAD METAL CAN - CM3



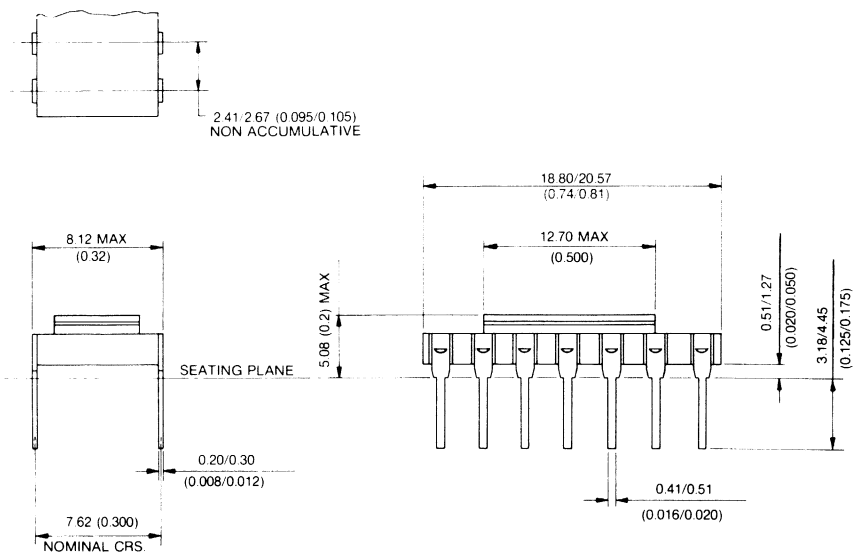
6-LEAD METAL CAN - CM6



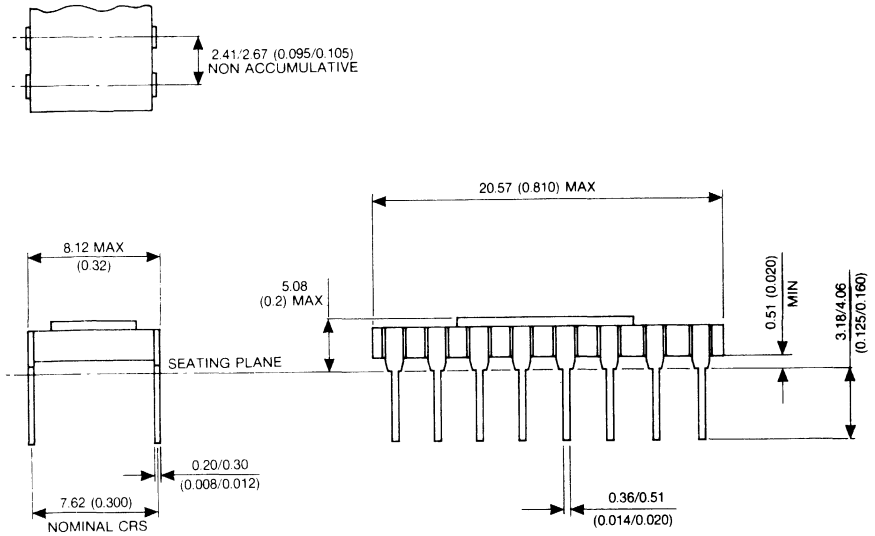
10-LEAD METAL/CERAMIC (5.84mm PCD)
WITH STANDOFF - CM10/S



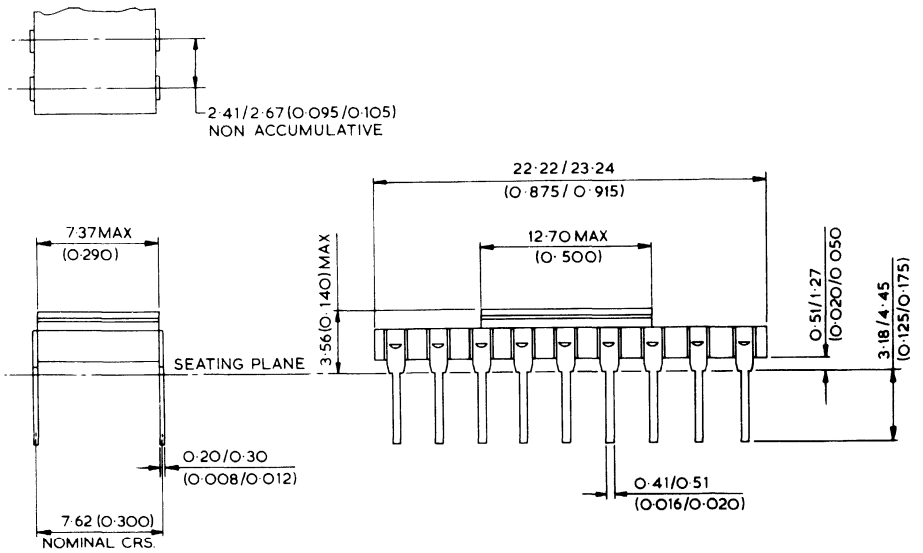
8-LEAD SIDEBRAZED CERAMIC DIL - DC8



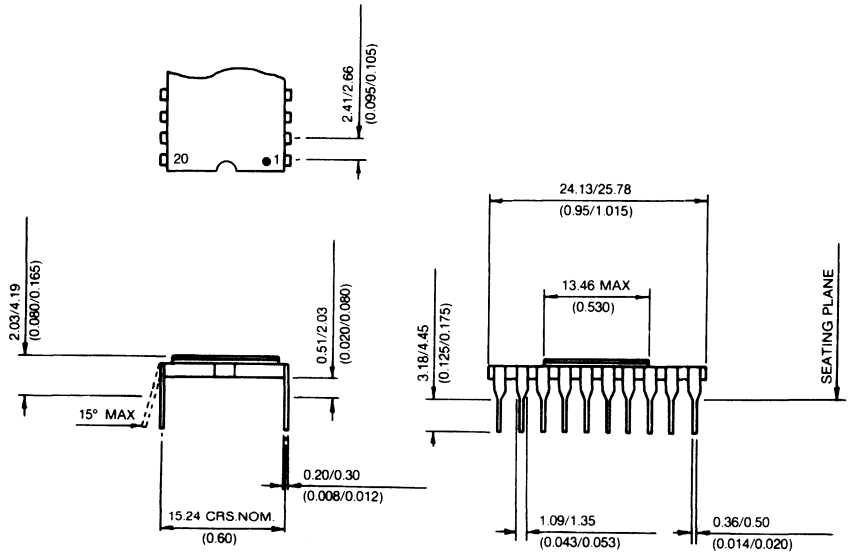
14-LEAD SIDEBRAZED CERAMIC DIL - DC14



16-LEAD SIDEBRAZED CERAMIC DIL - DC16



18-LEAD SIDEBRAZED CERAMIC DIL - DC18



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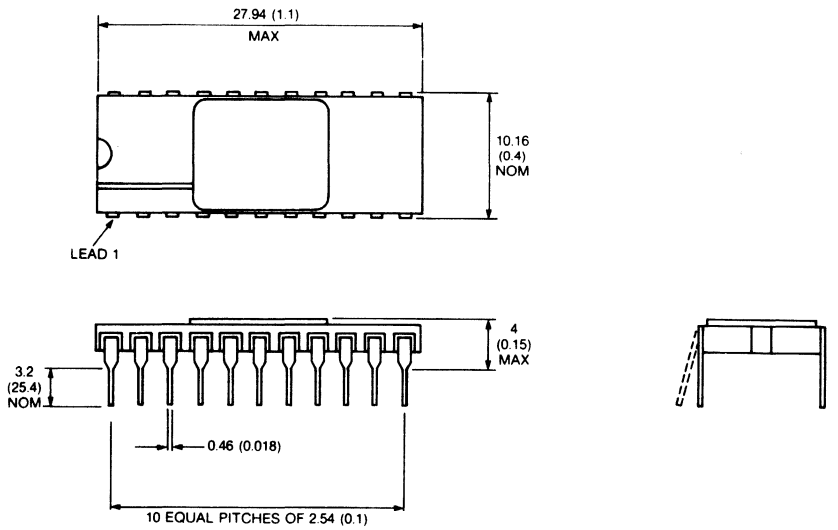
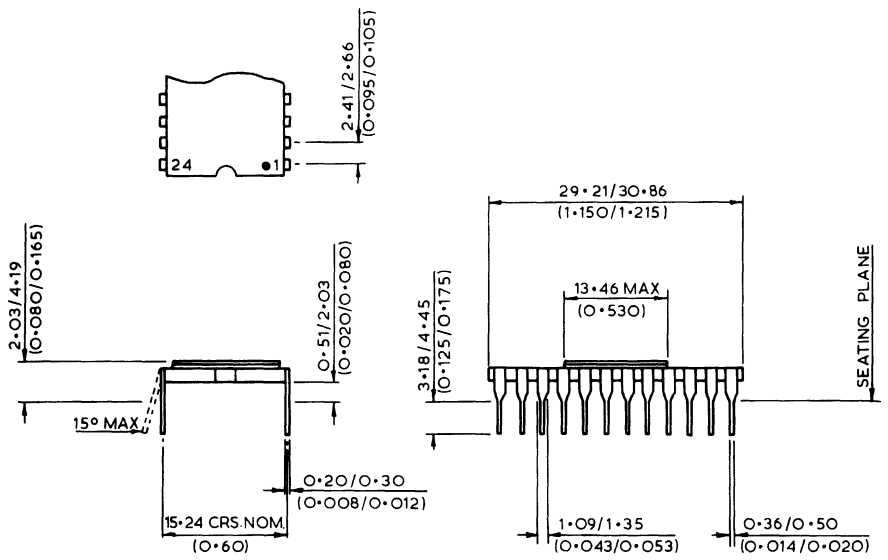
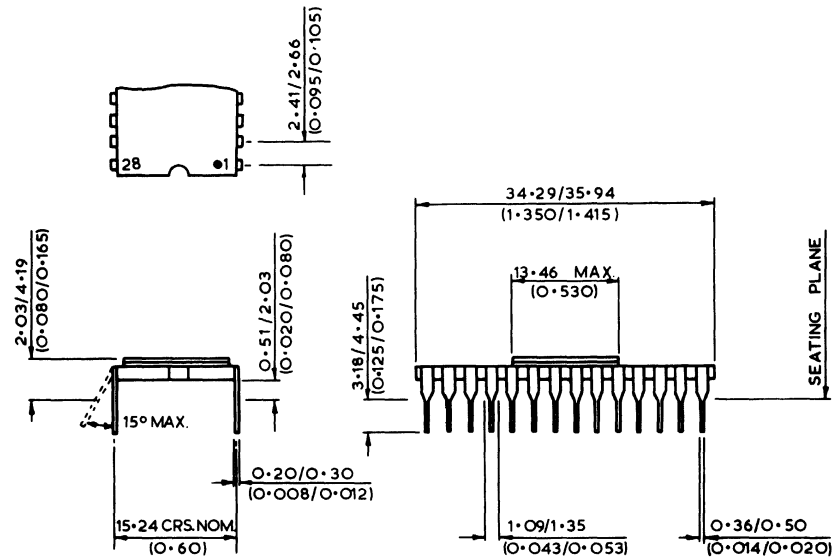


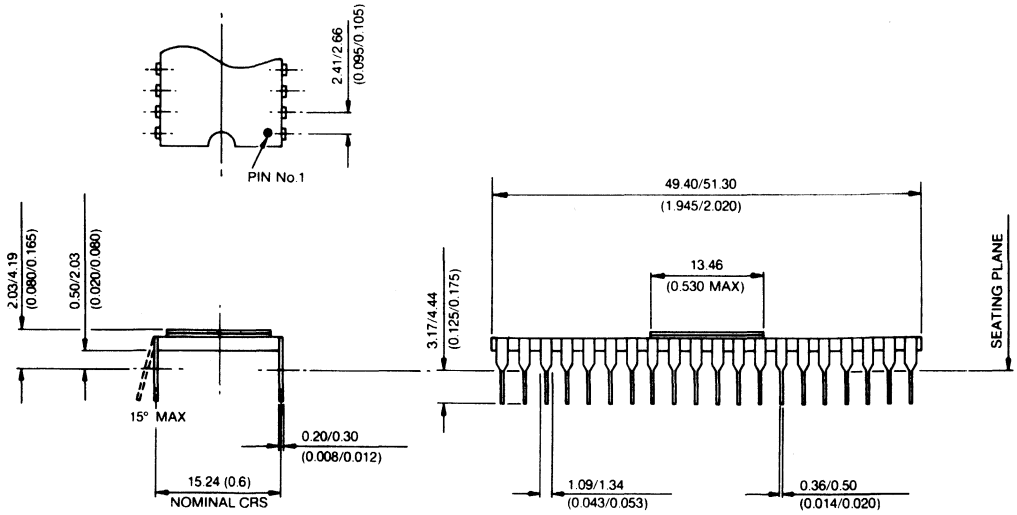
22-LEAD SIDEBRAZED CERAMIC DIL - DC22



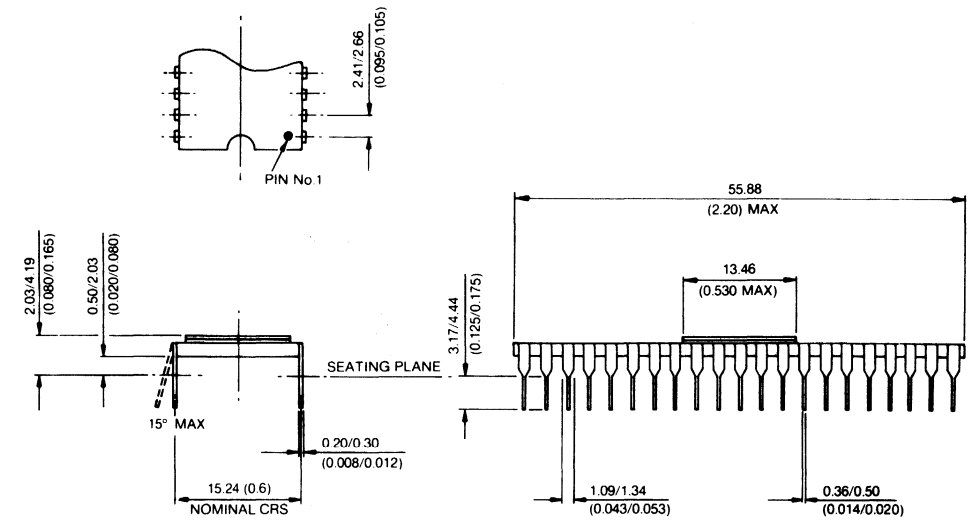
24-LEAD SIDEBRAZED CERAMIC DIL - DC24



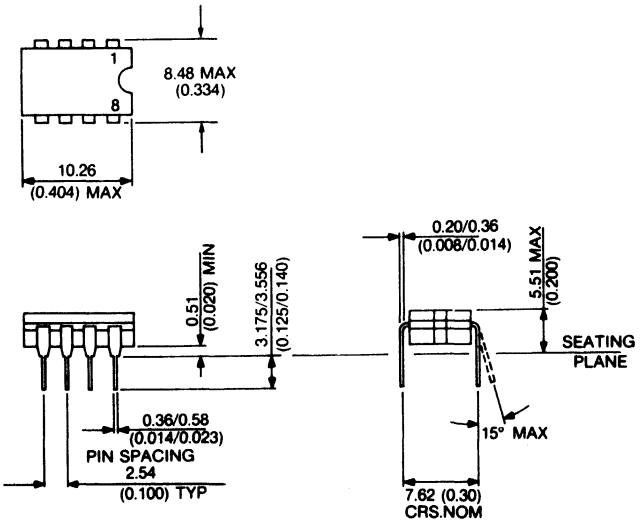
28-LEAD SIDEBRAZED CERAMIC DIL - DC28



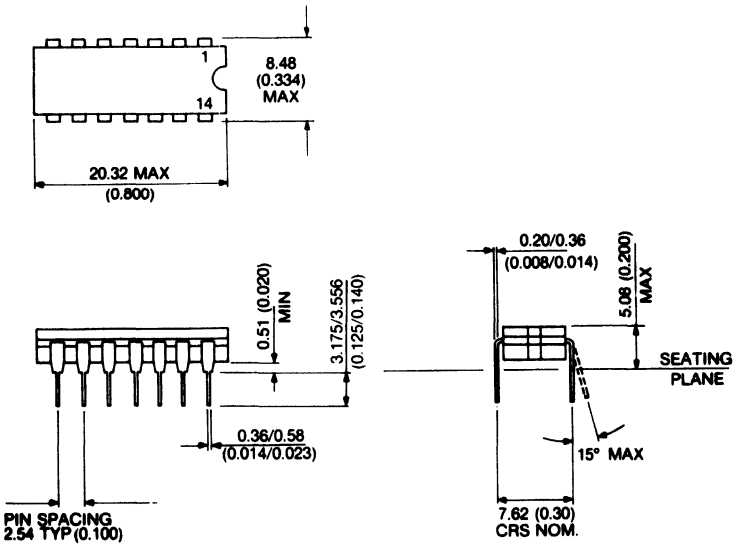
40-LEAD SIDEBRAZED CERAMIC DIL - DC40



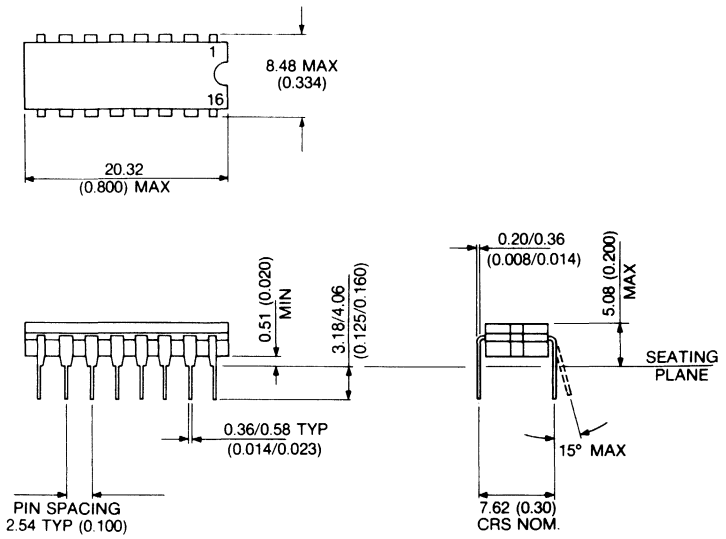
42-LEAD SIDEBRAZED CERAMIC DIL - DC42



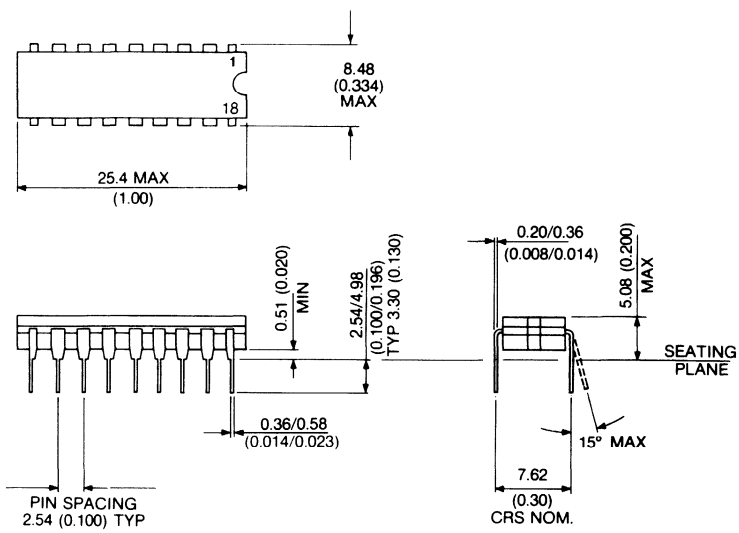
8-LEAD CERAMIC DIL - DG8



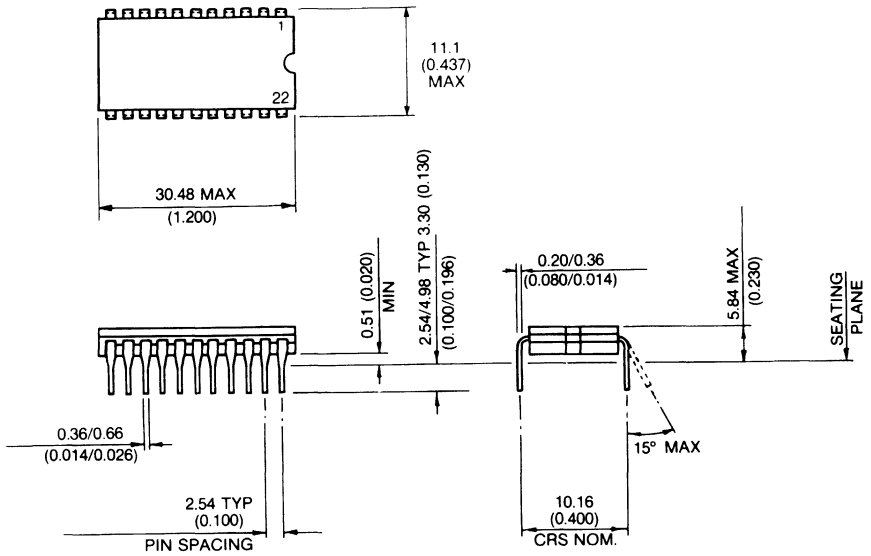
14-LEAD CERAMIC DIL - DG14



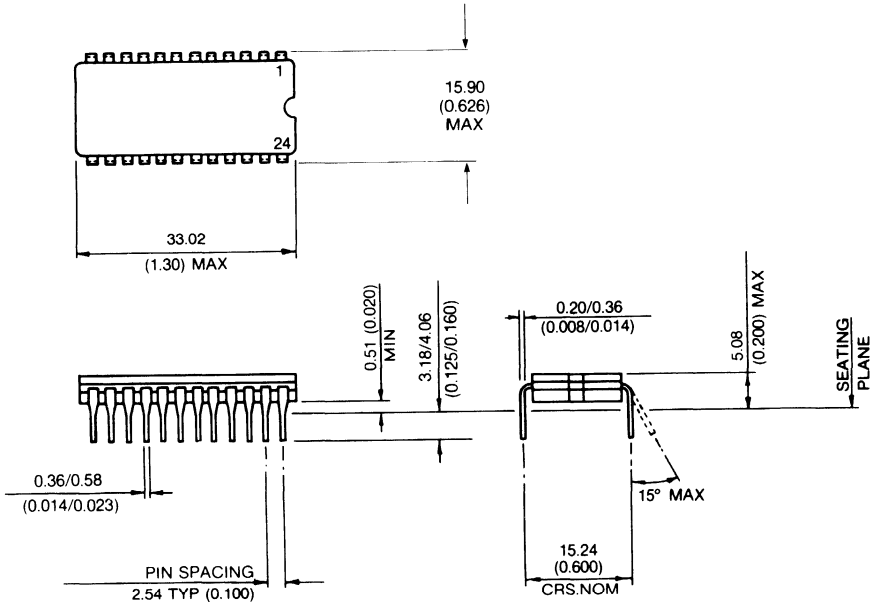
16-LEAD CERAMIC DIL - DG16



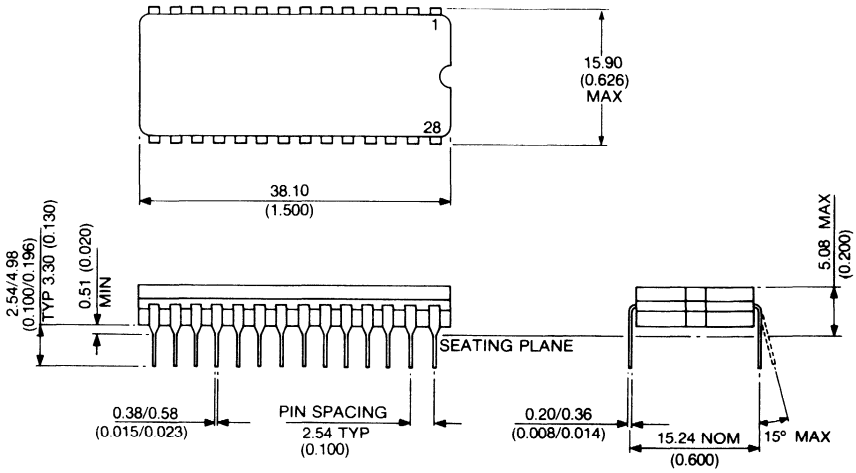
18-LEAD CERAMIC DIL - DG18



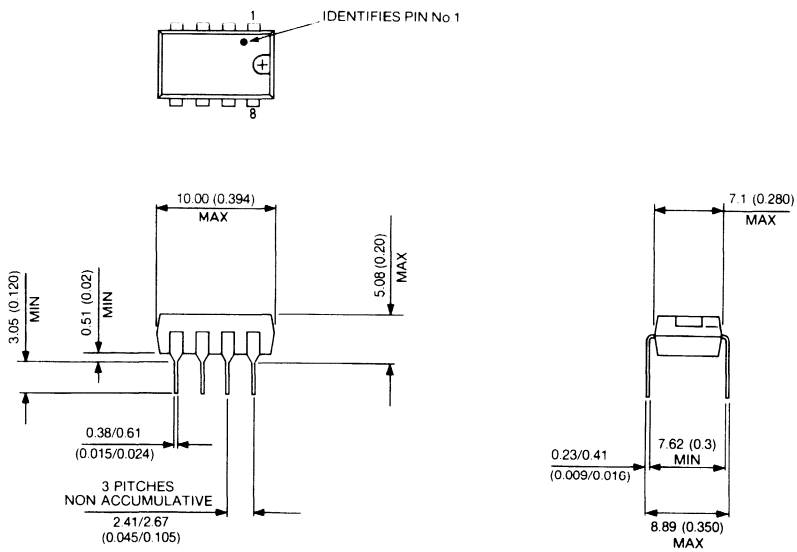
22-LEAD CERAMIC DIL CERDIP - DG22



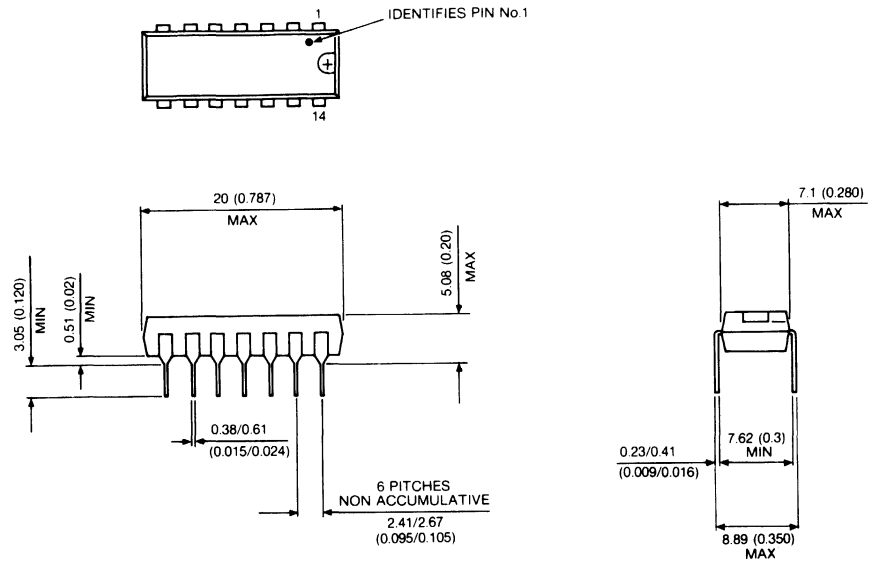
24 LEAD CERAMIC DIL CERDIP - DG24



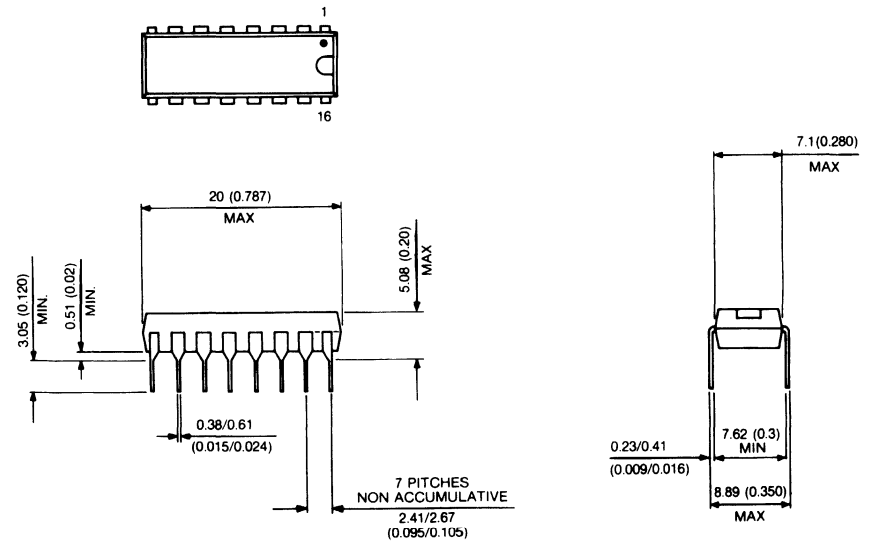
28-LEAD CERAMIC DIL - DG28



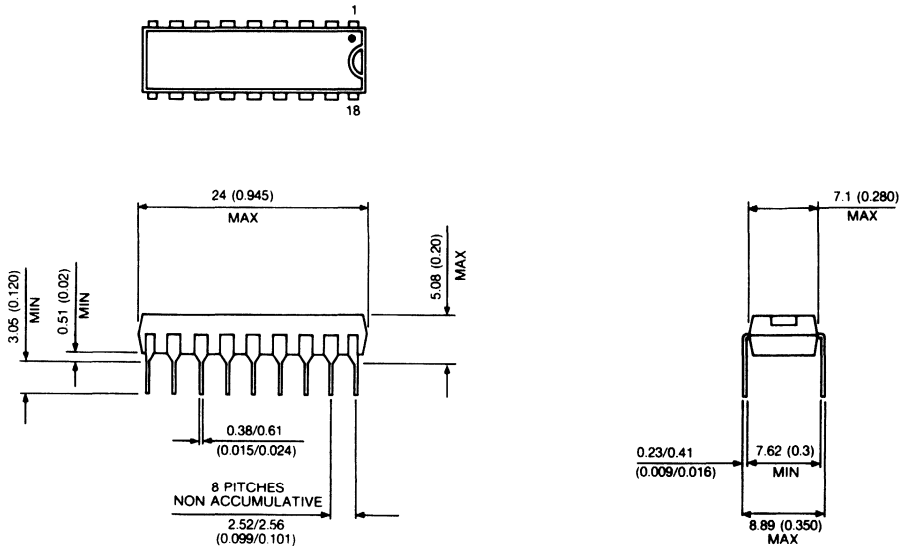
8-LEAD PLASTIC DIL - DP8



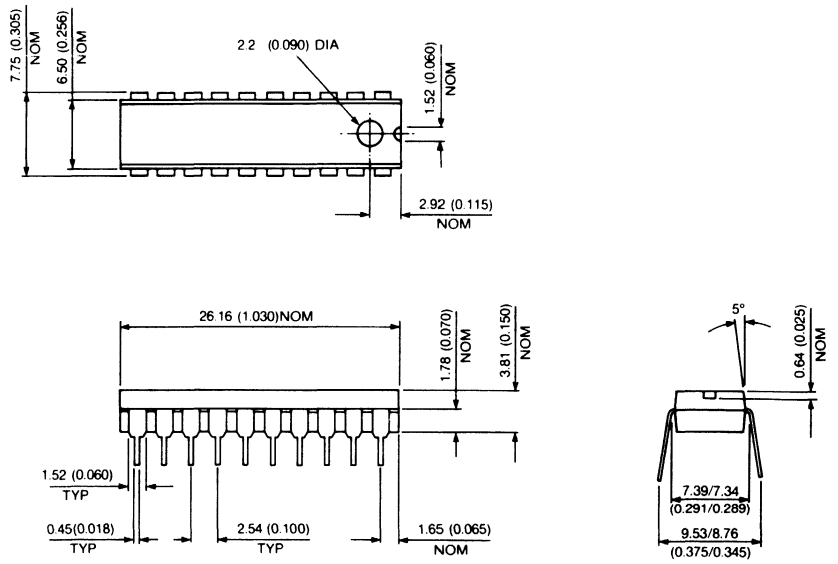
14-LEAD PLASTIC DIL - DP14



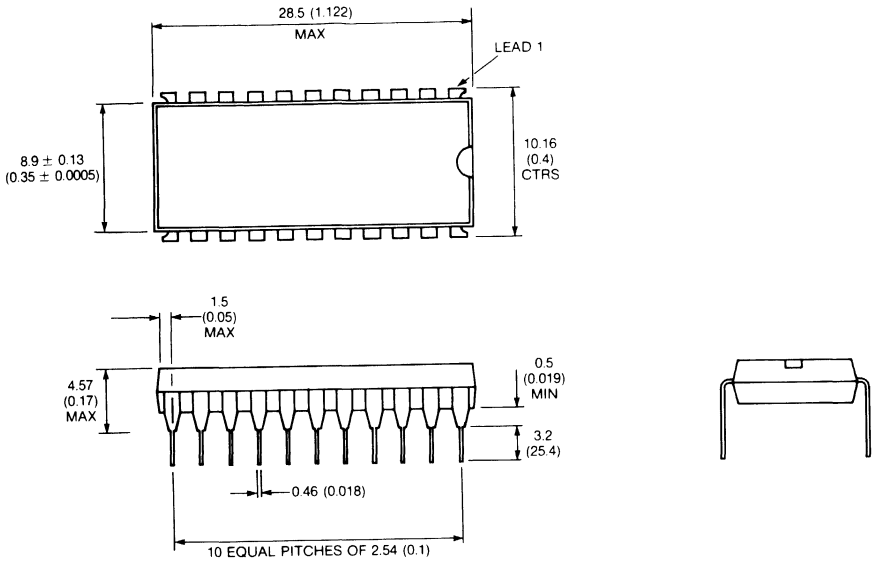
16-LEAD PLASTIC DIL - DP16



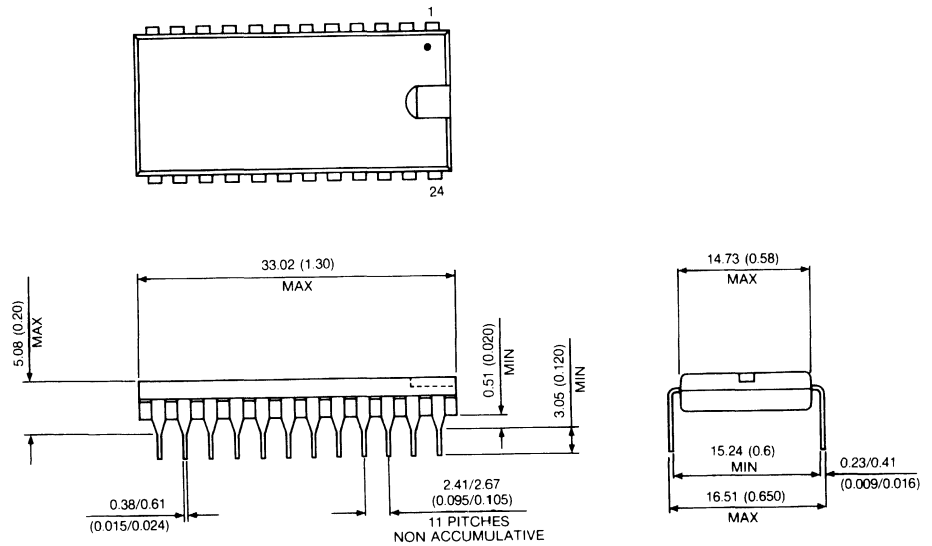
18-LEAD PLASTIC DIL - DP18



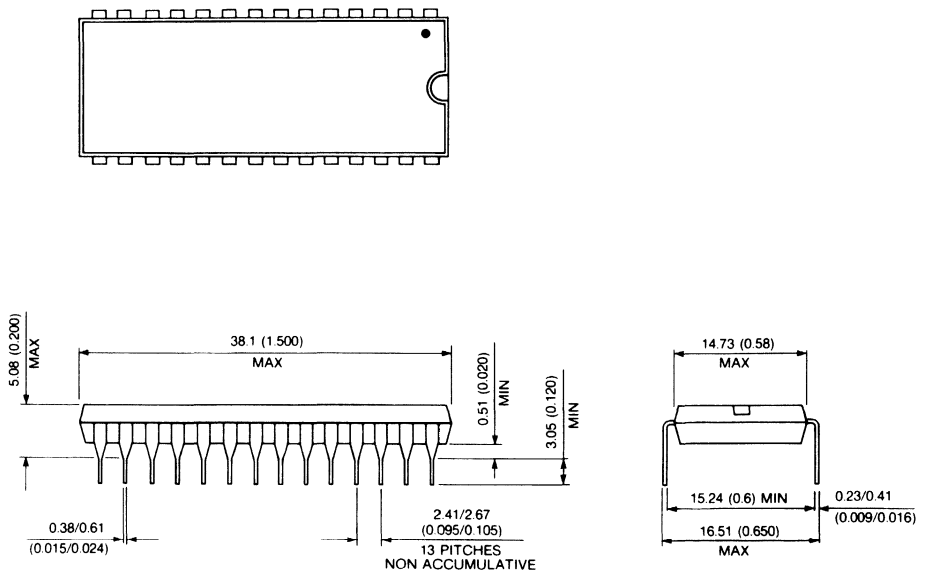
20 LEAD PLASTIC DIL – DP20



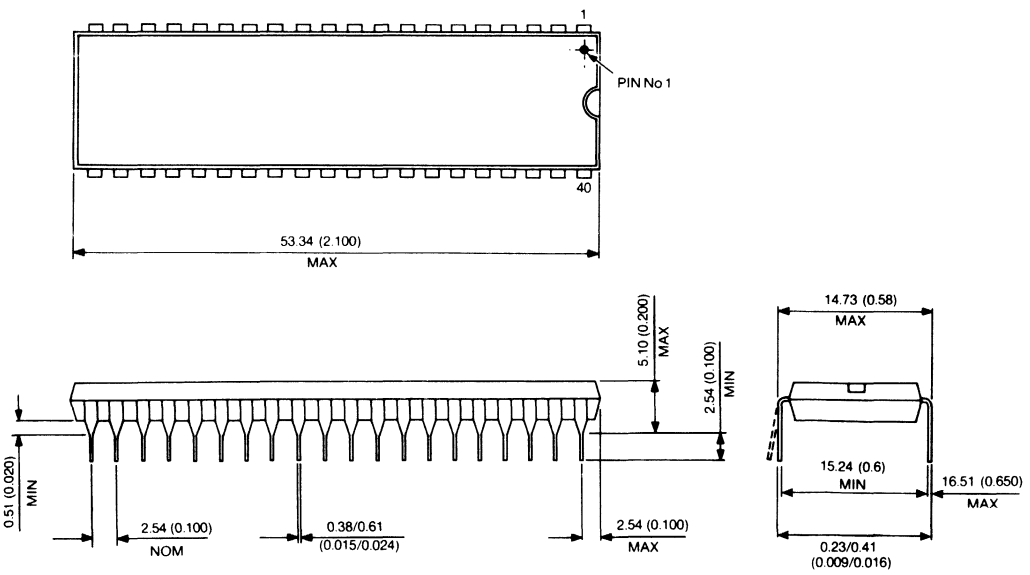
22-LEAD PLASTIC - DP22



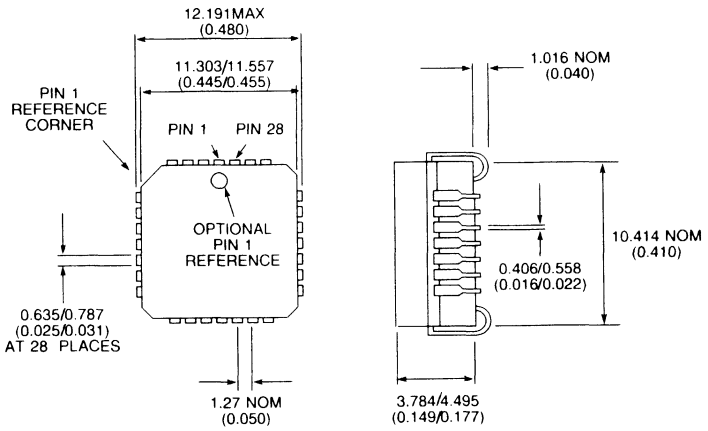
24-LEAD PLASTIC DIL - DP24



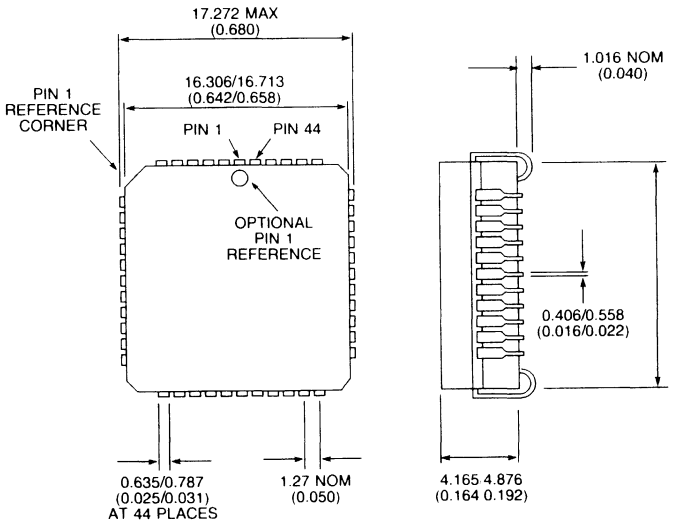
28-LEAD PLASTIC DIL - DP28



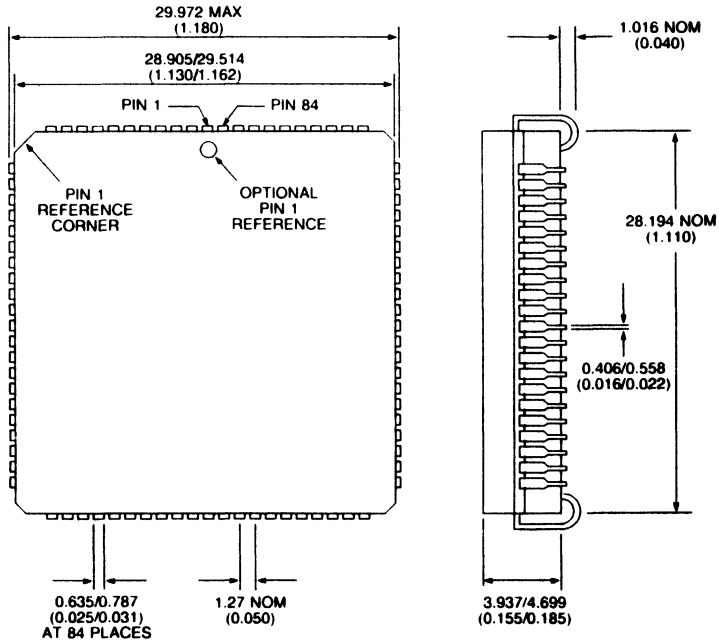
40 LEAD PLASTIC DIL - DP40



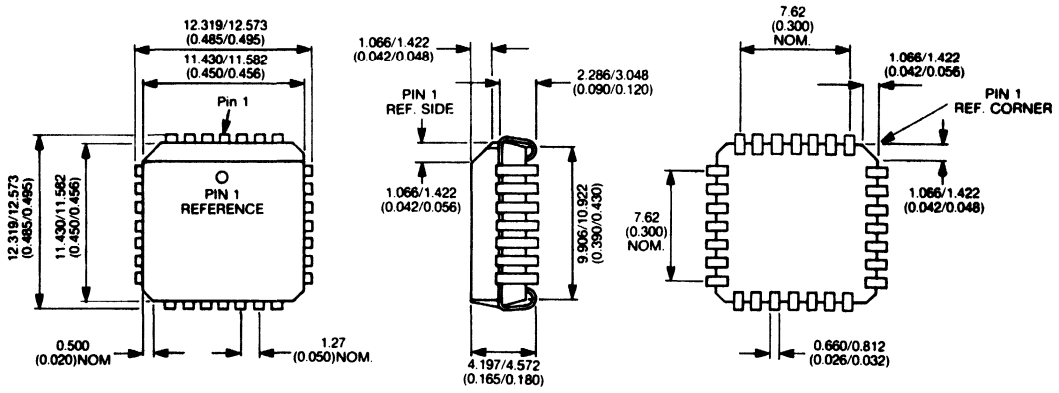
28-LEAD QUAD CERPAC CHIP CARRIER - HG28



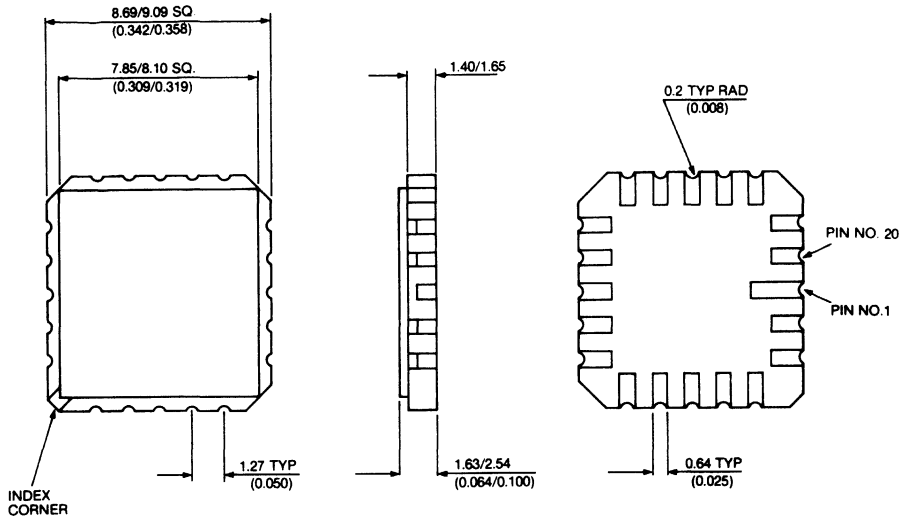
44-LEAD QUAD CERPAC CHIP CARRIER - HG44



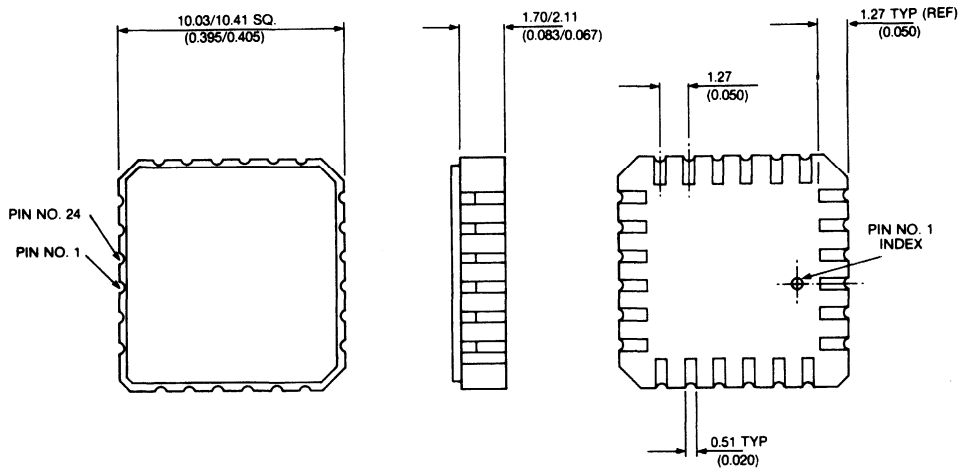
84-LEAD QUAD CERPAC CHIP CARRIER - HG84



28-LEAD QUAD PLASTIC J LEAD - HP28



20-PIN LEADLESS CHIP CARRIER - LC20
(HERMETIC)



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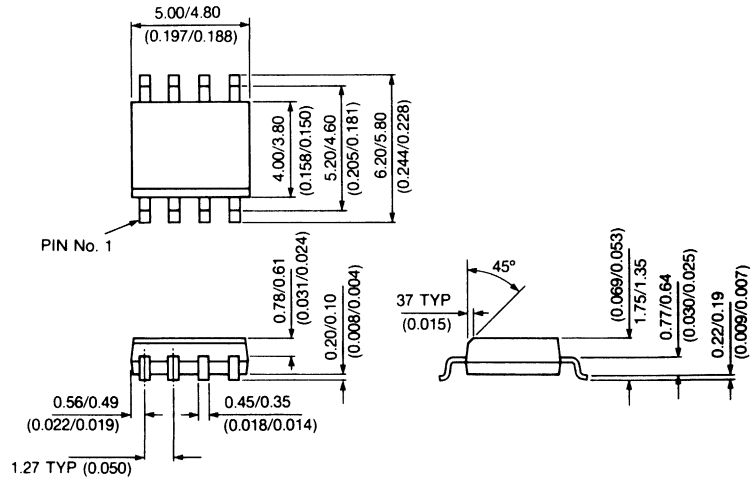
(HERMETIC)



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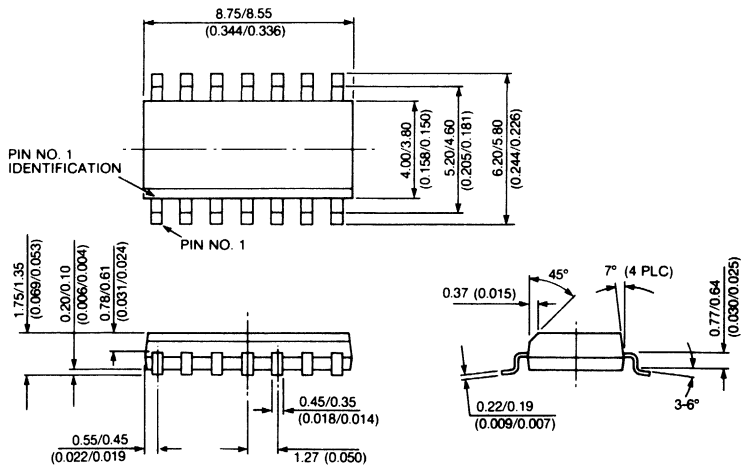

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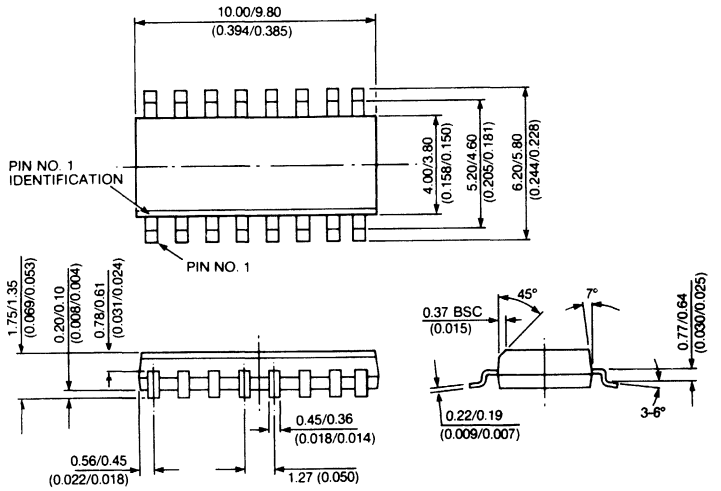

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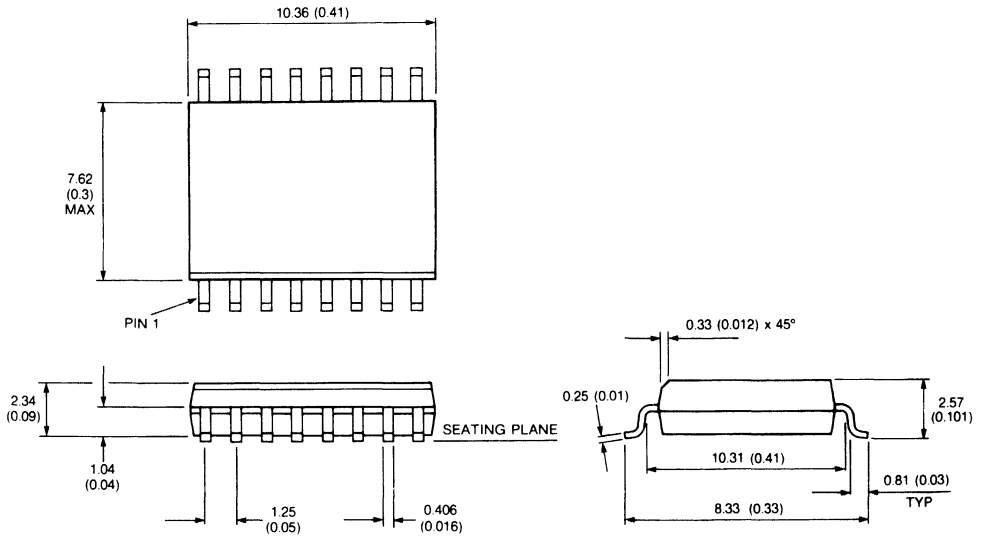

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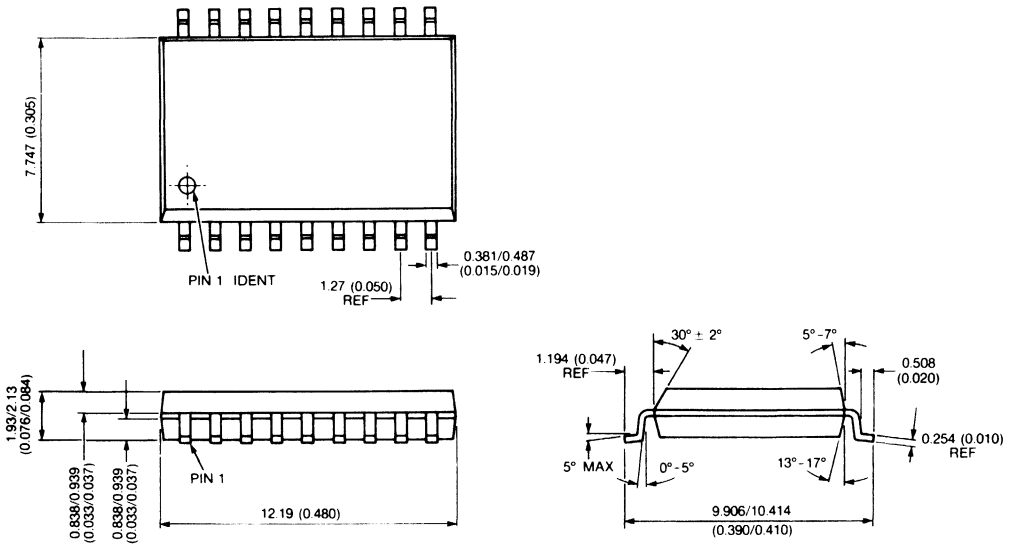

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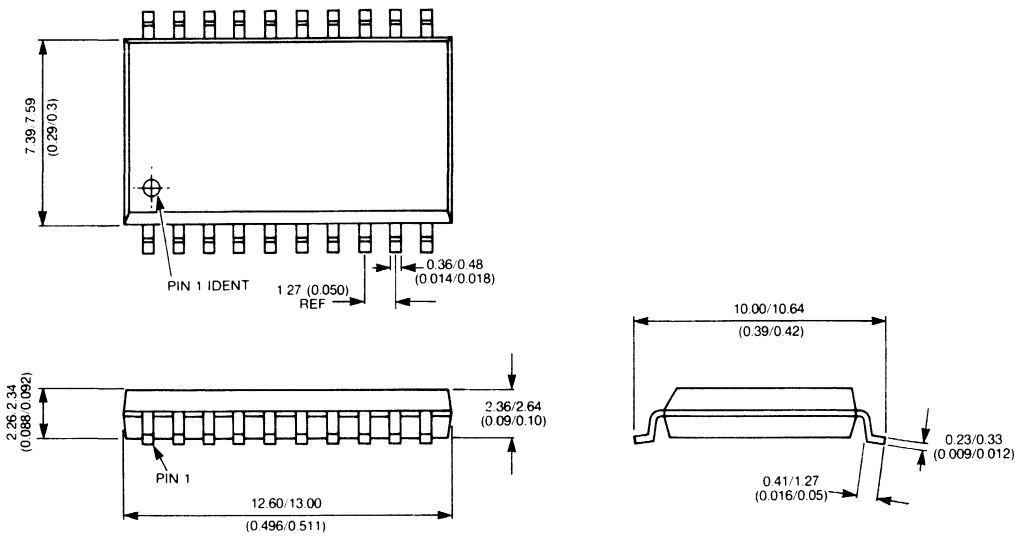

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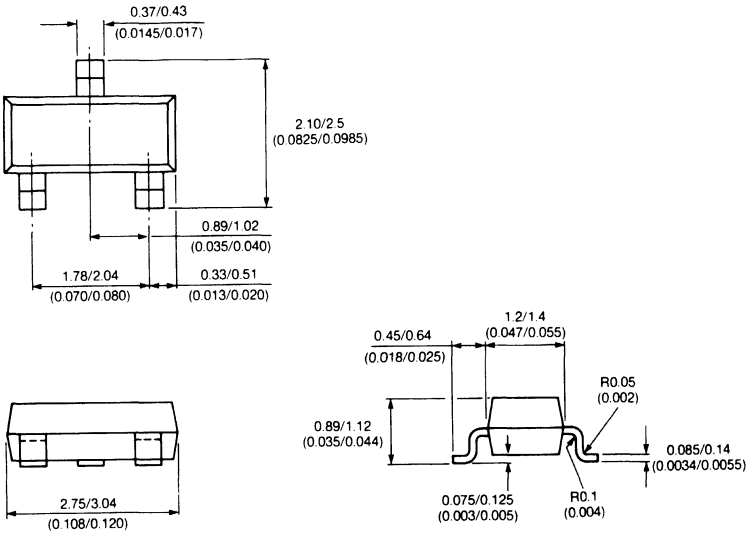

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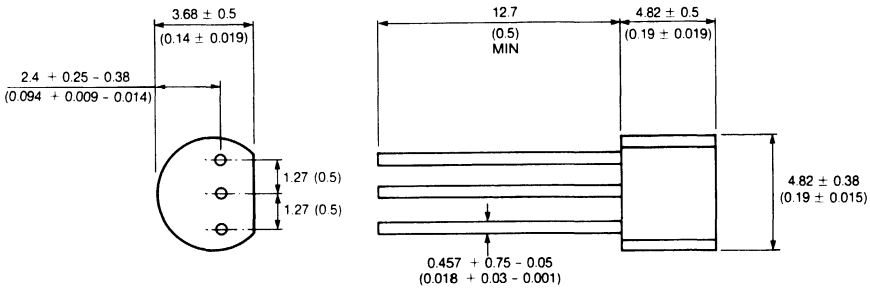

3-LEAD PLASTIC -TO-92

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